74LVX574

LOW VOLTAGE CMOS OCTAL D-TYPE FLIP-FLOP (3-STATE NON INV.) WITH 5V TOLERANT INPUTS

- HIGH SPEED:
  f_{MAX} = 125MHz (TYP.) at V_{CC} = 3.3V
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:
  V_{IL} = 0.8V, V_{IH} = 2V at V_{CC} = 3V
- LOW POWER DISSIPATION:
  I_{CC} = 4 µA (MAX.) at T_A=25°C
- LOW NOISE:
  V_{OLP} = 0.3V (TYP.) at V_{CC} =3.3V
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 4 mA (MIN) at V_{CC} =3V
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 2V to 3.6V (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 574
- IMPROVED LATCH-UP IMMUNITY

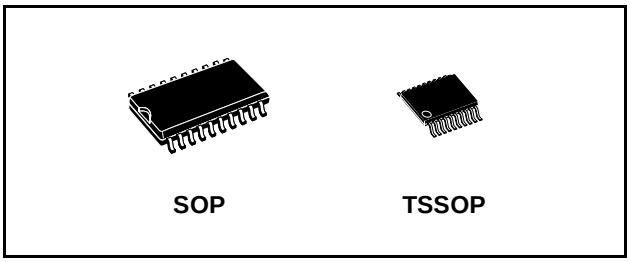


Table 1: Order Codes

PACKAGE	T & R
SOP	74LVX574MTR
TSSOP	74LVX574TTR

DESCRIPTION

The 74LVX574 is a low voltage CMOS OCTAL D-TYPE FLIP-FLOP with 3 STATE OUTPUT NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.

This 8 bit D-Type flip-flop is controlled by a clock input (CK) and an output enable input ($\overline{OE}$). On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs. While the ($\overline{OE}$) input is low, the 8 outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state. The output control does not affect the internal operation of flip flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

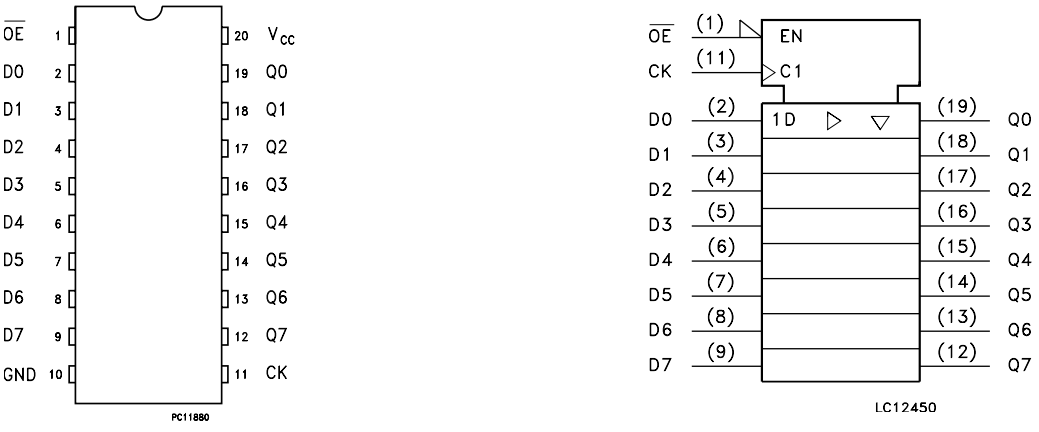


Figure 2: Input Equivalent Circuit

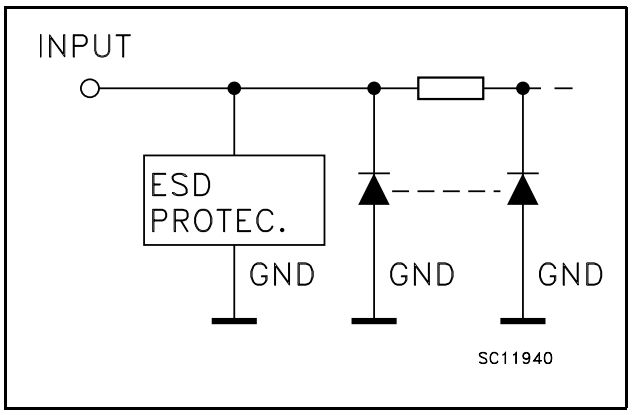


Table 2: Pin Description

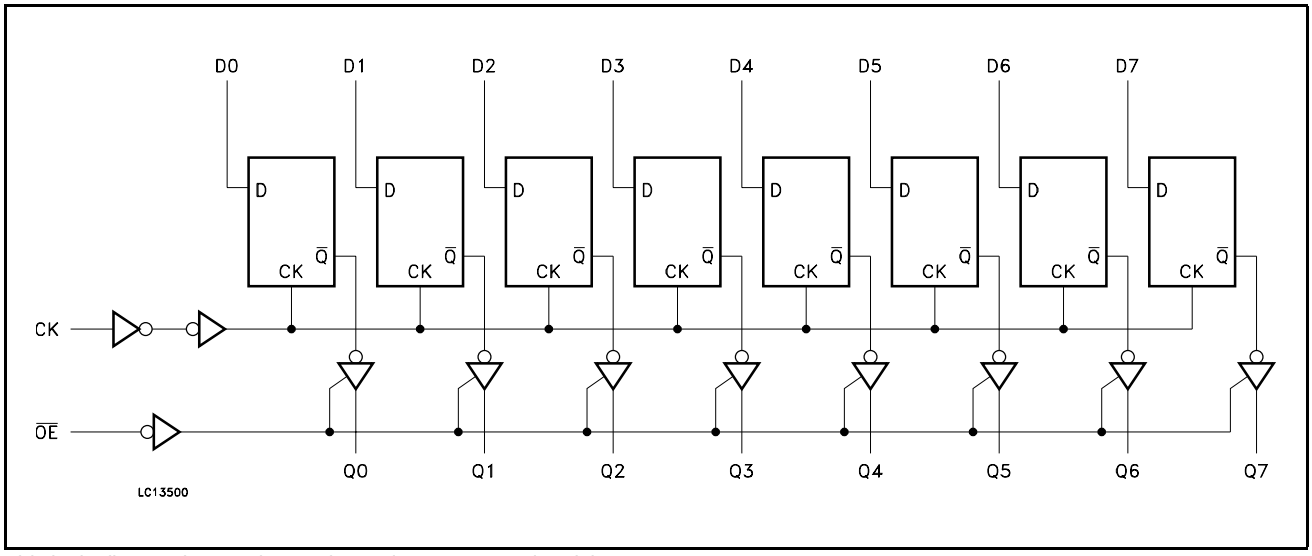
PIN N°	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-State Output Enable Input (Active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D0 to D7	Data Inputs
12, 13, 14, 15, 16, 17, 18, 19	Q0 to Q7	3-State Outputs
11	CK	Clock Input (LOW-to-HIGH Edge Triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	⌐	X	NO CHANGE
L	⌐	L	L
L	⌐	H	H

X : Don't Care
Z : High Impedance

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	2 to 3.6	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) (V_{CC} = 3V)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V
2) V_{IN} from 0.8V to 2.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-50 µA	1.9	2.0		1.9		1.9		V
		3.0	I_O=-50 µA	2.9	3.0		2.9		2.9		
		3.0	I_O=-4 mA	2.58			2.48		2.4		
V_{OL}	Low Level Output Voltage	2.0	I_O=50 µA		0.0	0.1		0.1		0.1	V
		3.0	I_O=50 µA		0.0	0.1		0.1		0.1	
		3.0	I_O=4 mA			0.36		0.44		0.55	
I_{OZ}	High Impedance Output Leakage Current	3.6	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			±0.25		± 2.5		± 2.5	µA
I_I	Input Leakage Current	3.6	V_I = 5V or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND			4		40		40	µA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C_L = 50 pF		0.3	0.8					V
V_{OLV}				-0.8	-0.3						
V_{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V_{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (Input $t_r = t_f$ = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q	2.7	15			9.2	14.5	1.0	17.5	1.0	17.5	ns
		2.7	50			11.5	18.0	1.0	21.0	1.0	21.0	
		3.3(*)	15			8.5	13.2	1.0	15.5	1.0	15.5	
		3.3(*)	50			11.0	16.7	1.0	19.0	1.0	19.0	
t_{PZL} t_{PZH}	Output Enable Time	2.7	15			9.8	15.0	1.0	18.5	1.0	18.5	ns
		2.7	50			11.4	18.5	1.0	22.0	1.0	22.0	
		3.3(*)	15			8.2	12.8	1.0	15.0	1.0	15.0	
		3.3(*)	50			10.7	16.3	1.0	18.5	1.0	18.5	
t_{PLZ} t_{PHZ}	Output Disable Time	2.7	50			12.1	19.1	1.0	22.0	1.0	22.0	ns
		3.3(*)	50			11.0	15.0	1.0	17.0	1.0	17.0	
t_W	CK pulse Width, HIGH	2.7	50			6.5			7.5		7.5	ns
		3.3(*)	50			5.0			5.0		5.0	
t_S	Setup Time D to CK HIGH or LOW	2.7	50			5.0			5.0		5.0	ns
		3.3(*)	50			3.5			3.5		3.5	
t_h	Hold Time D to CK HIGH or LOW	2.7	50			1.5			1.5		1.5	ns
		3.3(*)	50			1.5			1.5		1.5	
f_{MAX}	Maximum Clock Frequency	2.7	15		60	115		50		48		MHz
		2.7	50		45	60		40		40		
		3.3(*)	15		80	125		65		60		
		3.3(*)	50		50	75		45		40		
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1,2)	2.7	50			0.5	1.0		1.5		1.5	ns
		3.3(*)	50			0.5	1.0		1.5		1.5	

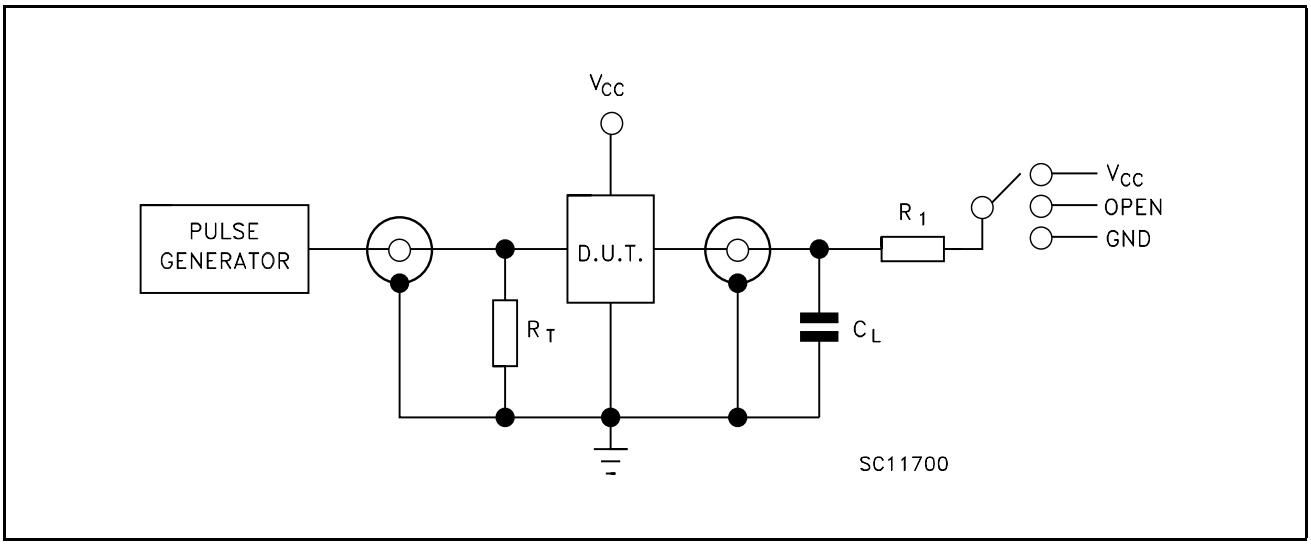
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW
2) Parameter guaranteed by design
(*) Voltage range is 3.3V ± 0.3V

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	3.3			4	10		10		10	pF
C_{OUT}	Output Capacitance	3.3			6						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3	f_{IN} = 10MHz		27						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/8$ (per circuit)

Figure 4: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L =15/50pF or equivalent (includes jig and probe capacitance)
R_L = R1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays Setup And Hold Times (f=1MHz; 50% duty cycle)

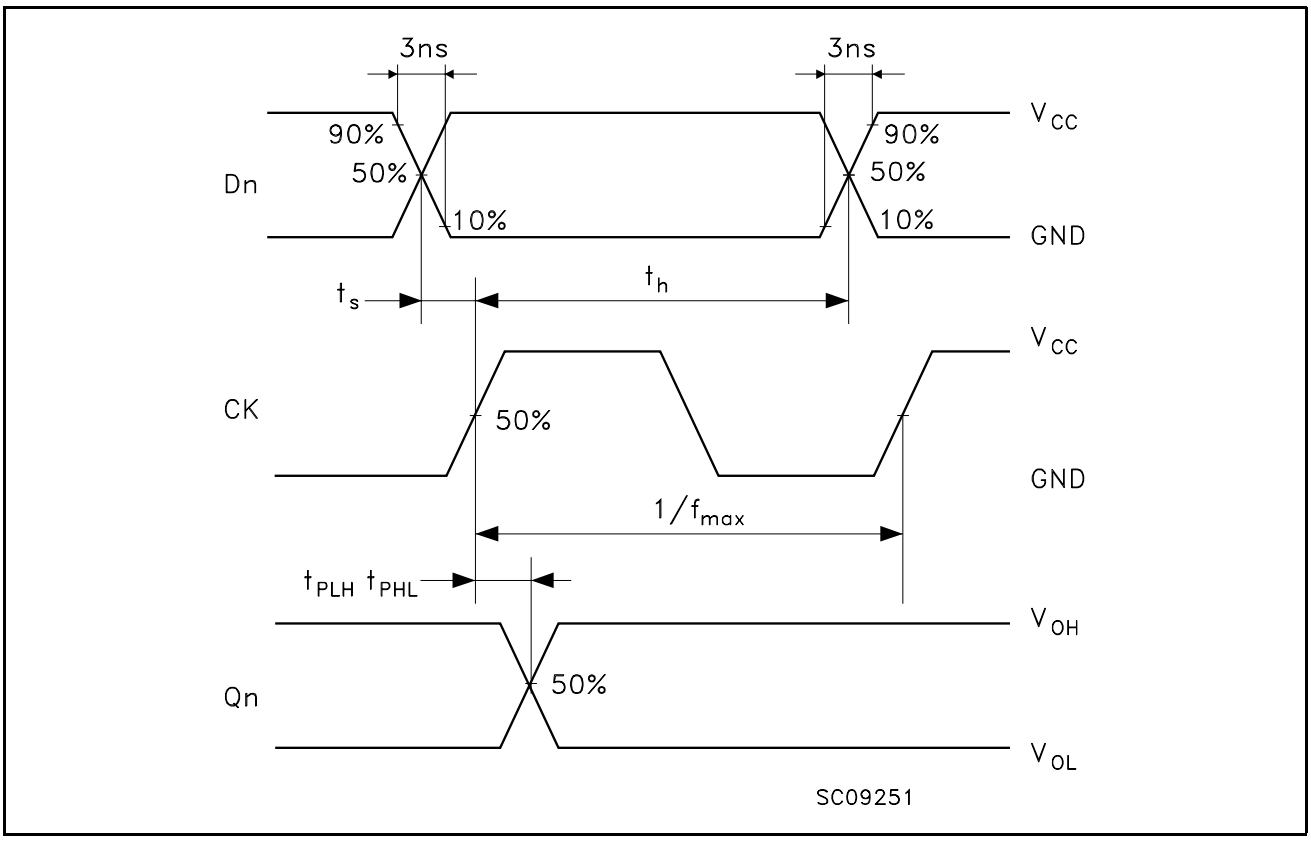


Figure 6: Waveform - Output Enable And Disable Times (f=1MHz; 50% duty cycle)

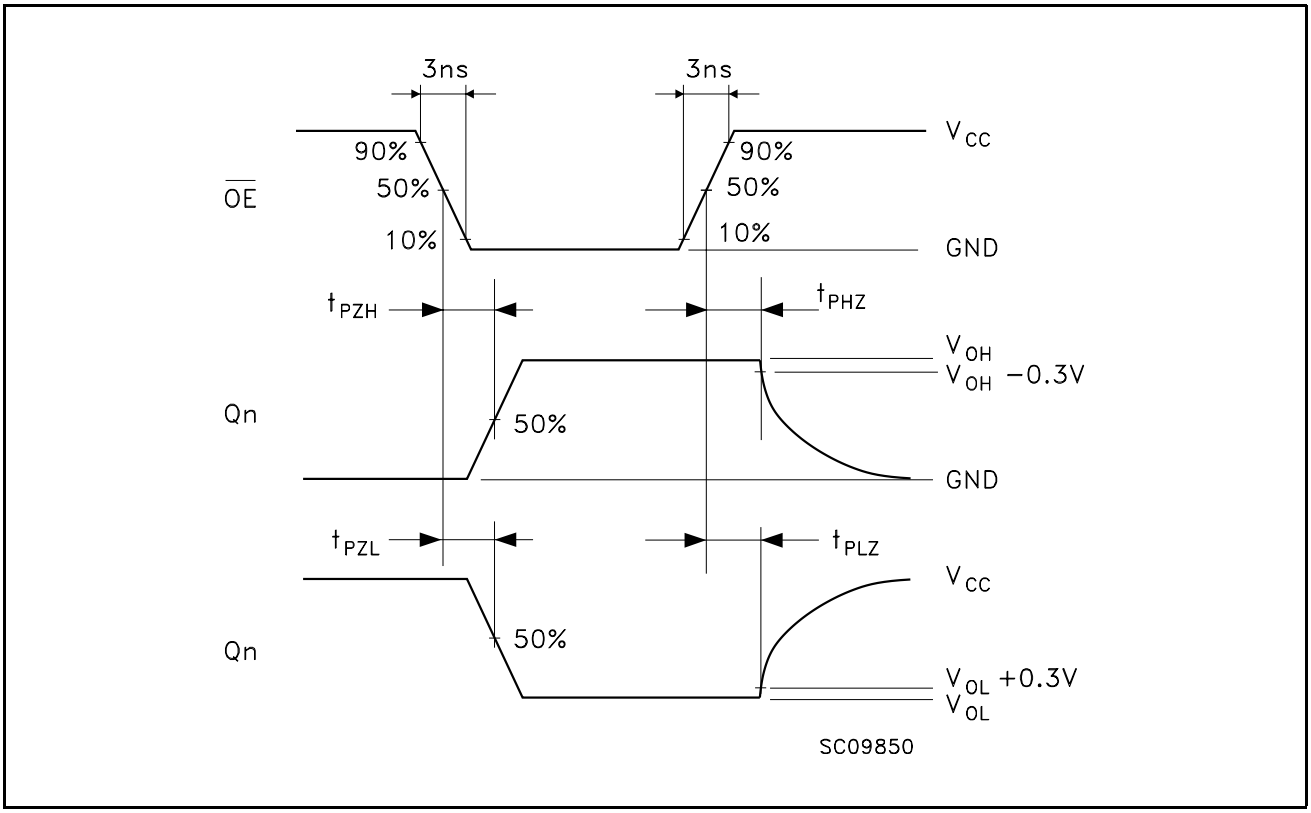
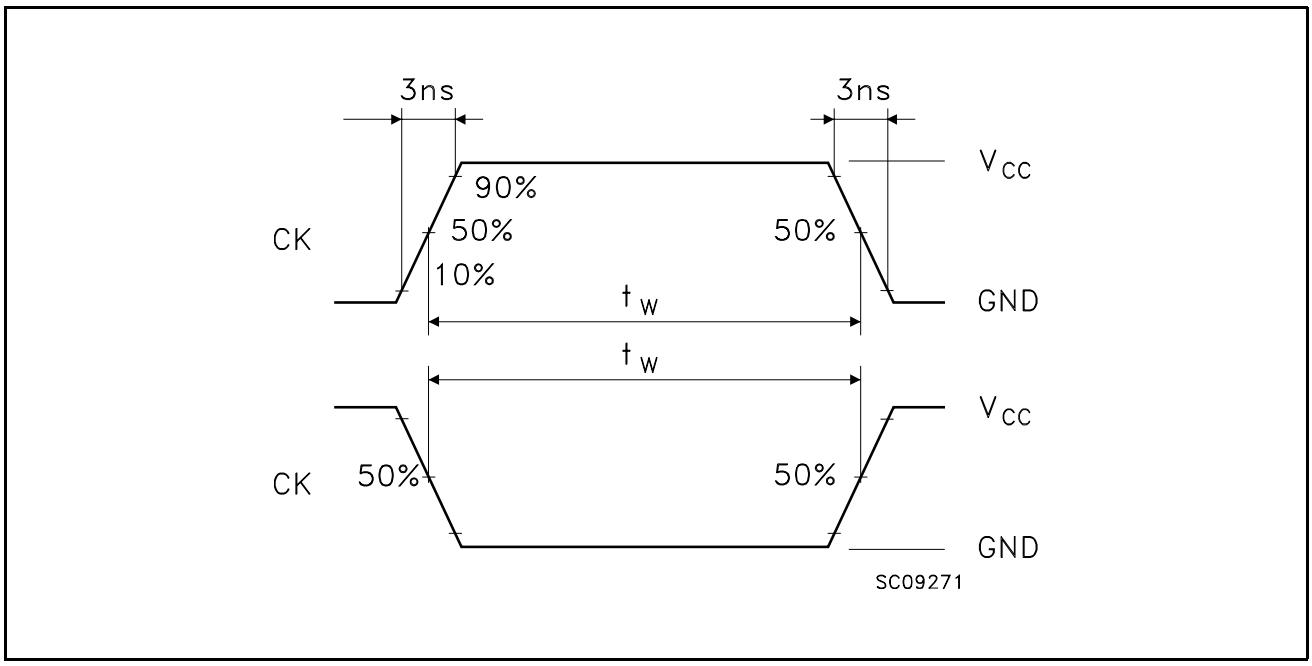
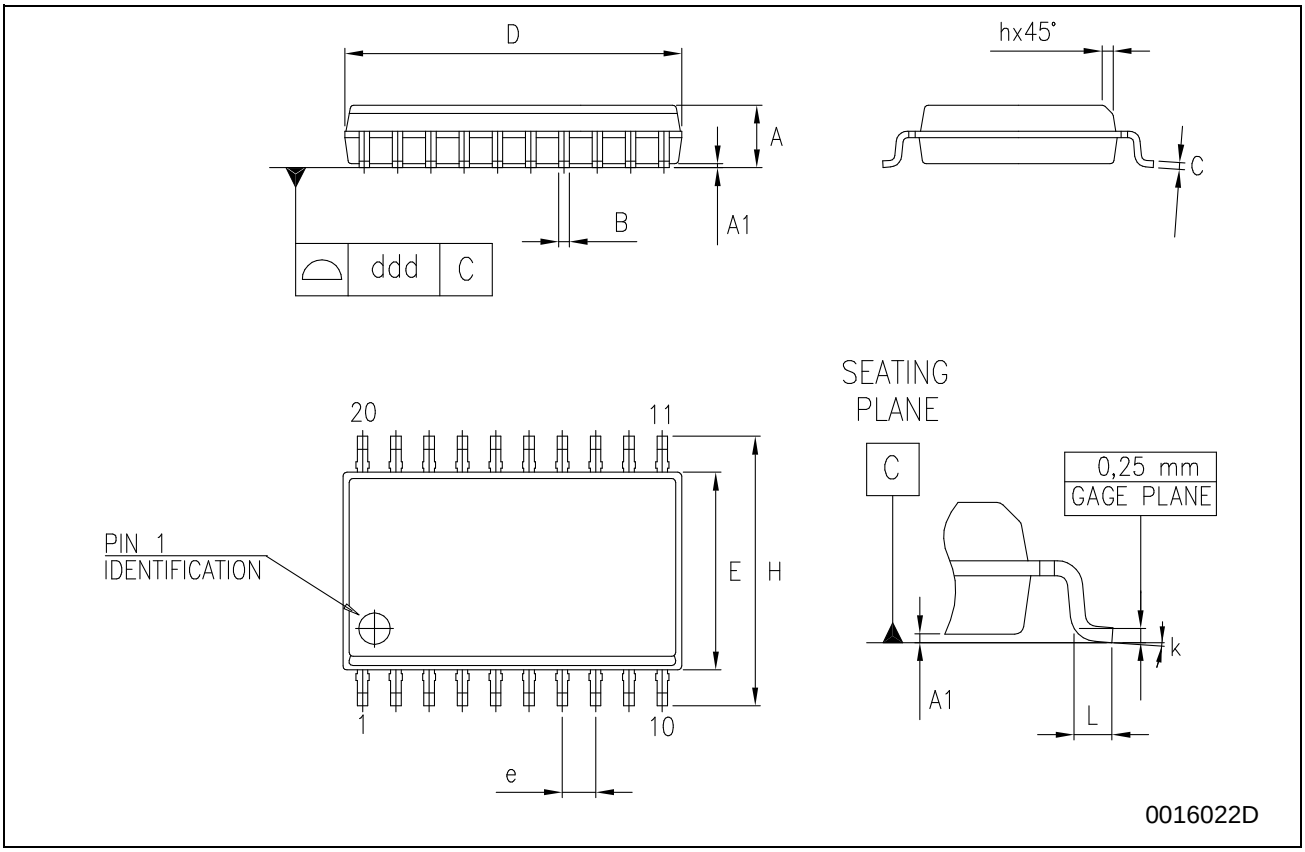


Figure 7: Waveform - CK Minimum Pulse Width (f=1MHz; 50% duty cycle)



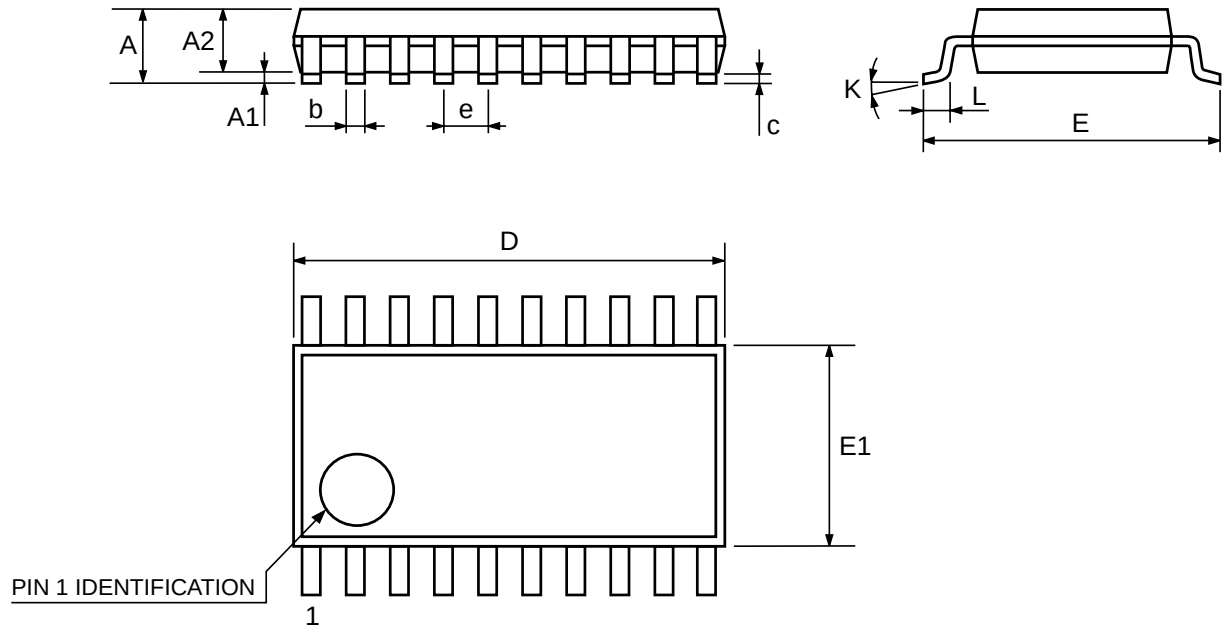
SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.30	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.60		13.00	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10.00		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



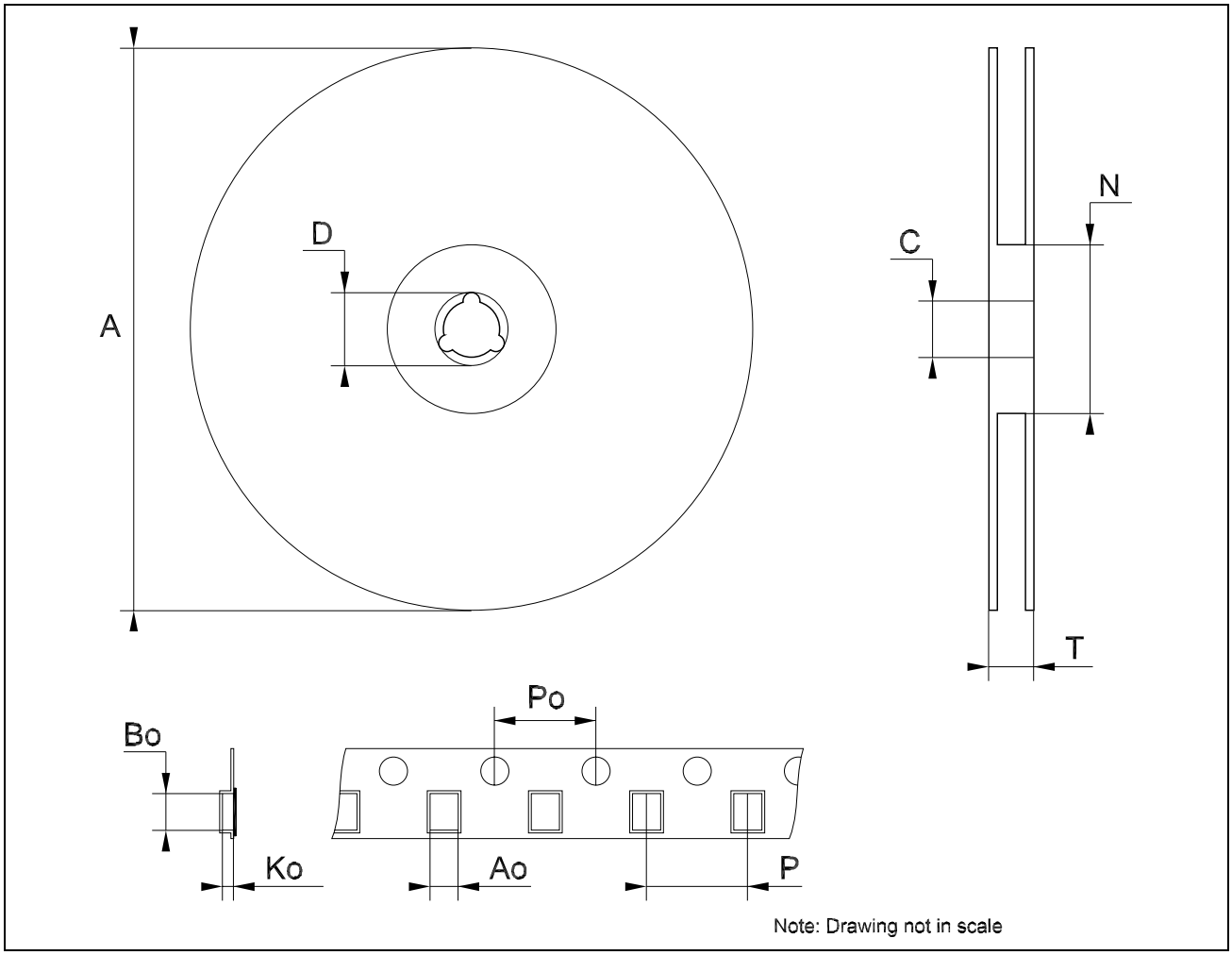
TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel SO-20 MECHANICAL DATA

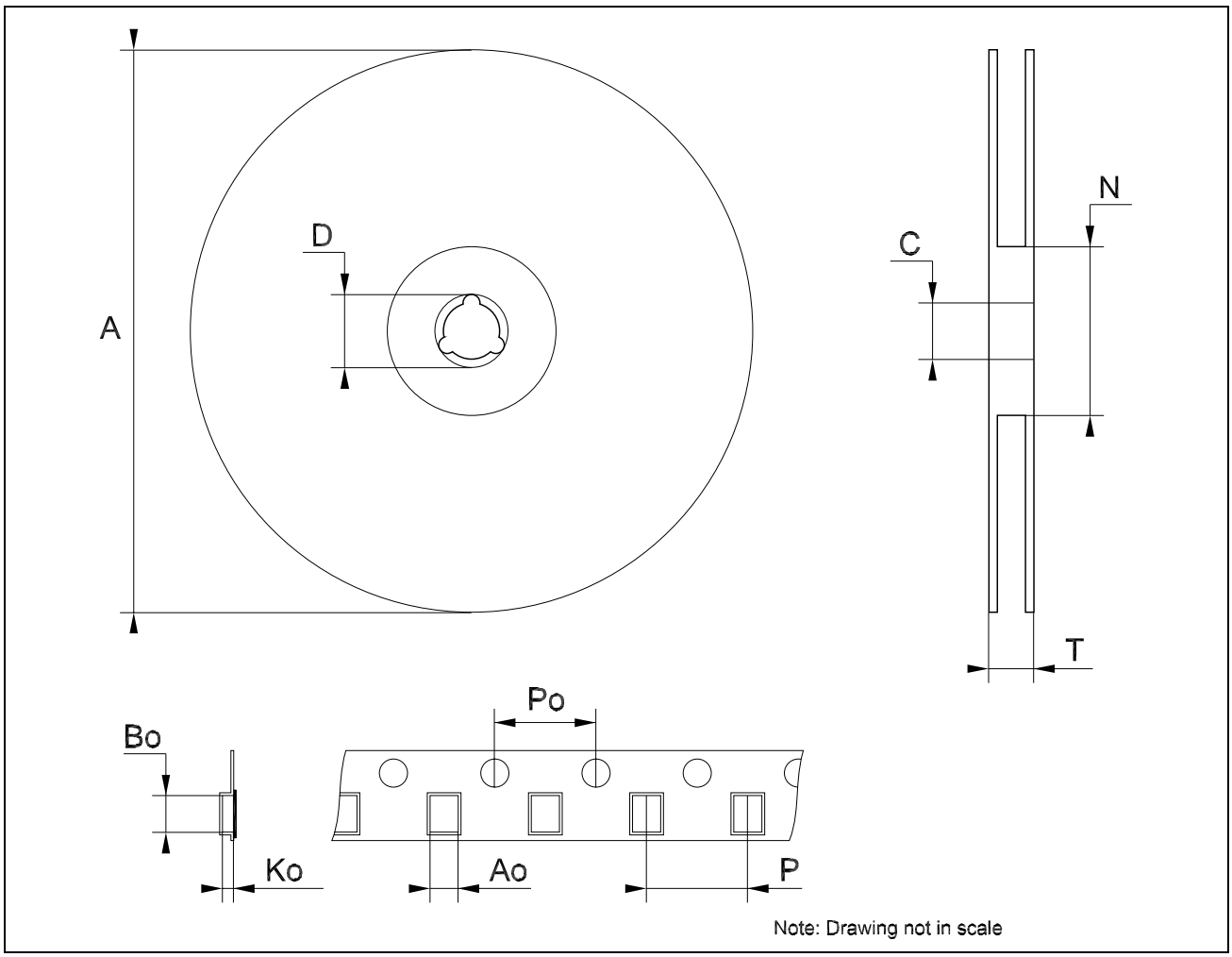
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11	0.425		0.433
Bo	13.2		13.4	0.520		0.528
Ko	3.1		3.3	0.122		0.130
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Table 10: Revision History

Date	Revision	Description of Changes
27-Aug-2004	3	Ordering Codes Revision - pag. 1.