FAIRCHILD SEMICONDUCTOR®

February 1993
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# 74LVX00
# Low Voltage Quad 2-Input NAND Gate

## General Description

The LVX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

## Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

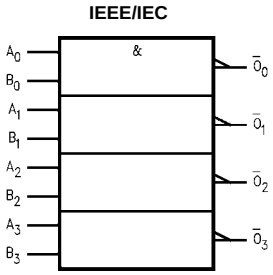
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74LVX00M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74LVX00MX_NL (Note 1) | M14A | Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74LVX00SJ | M14D | Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LVX00MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74LVX00MTCX_NL (Note 1) | MTC14 | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

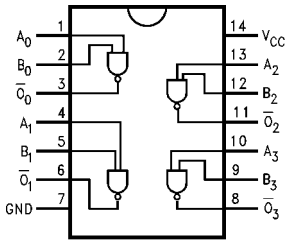
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

**Note 1:** "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

## Logic Symbol




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $A_n$, $B_n$ | Inputs |
| $\overline{O}_n$ | Outputs |

## Absolute Maximum Ratings (Note 2)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I$ = −0.5V | −20 mA |
| DC Input Voltage ($V_I$) | −0.5V to 7V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O$ = −0.5V | −20 mA |
| $V_O$ = $V_{CC}$ + 0.5V | +20 mA |
| DC Output Voltage ($V_O$) | −0.5V to $V_{CC}$ + 0.5V |
| DC Output Source | |
| or Sink Current ($I_O$) | ±25 mA |
| DC $V_{CC}$ or Ground Current | |
| ($I_{CC}$ or $I_{GND}$) | ±50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation | 180 mW |

## Recommended Operating Conditions (Note 3)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 2.0V to 3.6V |
| Input Voltage ($V_I$) | 0V to 5.5V |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Input Rise and Fall Time ($\Delta t/\Delta V$) | 0 ns/V to 100 ns/V |

**Note 2:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** Unused inputs must be held HIGH or LOW They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| $V_{IH}$ | HIGH Level Input Voltage | 2.0 | 1.5 | | | 1.5 | | V | | |
| | | 3.0 | 2.0 | | | 2.0 | | | | |
| | | 3.6 | 2.4 | | | 2.4 | | | | |
| $V_{IL}$ | LOW Level Input Voltage | 2.0 | | | 0.5 | | 0.5 | V | | |
| | | 3.0 | | | 0.8 | | 0.8 | | | |
| | | 3.6 | | | 0.8 | | 0.8 | | | |
| $V_{OH}$ | HIGH Level Output Voltage | 2.0 | 1.9 | 2.0 | | 1.9 | | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | $I_{OH}$ = −50 μA |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | $I_{OH}$ = −50 μA |
| | | 3.0 | 2.58 | | | 2.48 | | | | $I_{OH}$ = −4 mA |
| $V_{OL}$ | LOW Level Output Voltage | 2.0 | | 0.0 | 0.1 | | 0.1 | V | $V_{IN}$ = $V_{IL}$ or $V_{IH}$ | $I_{OL}$ = 50 μA |
| | | 3.0 | | 0.0 | 0.1 | | 0.1 | | | $I_{OL}$ = 50 μA |
| | | 3.0 | | | 0.36 | | 0.44 | | | $I_{OL}$ = 4 mA |
| $I_{IN}$ | Input Leakage Current | 3.6 | | | ±0.1 | | ±1.0 | μA | $V_{IN}$ = 5.5V or GND | |
| $I_{CC}$ | Quiescent Supply Current | 3.6 | | | 2.0 | | 20.0 | μA | $V_{IN}$ = $V_{CC}$ or GND | |

## Noise Characteristics (Note 4)

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = 25°C | | Units | $C_L$ (pF) |
|---|---|---|---|---|---|---|
| | | | Typ | Limit | | |
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 3.3 | 0.3 | 0.5 | V | 50 |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | 3.3 | −0.3 | −0.5 | V | 50 |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 3.3 | | 2.0 | V | 50 |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | 3.3 | | 0.8 | V | 50 |

**Note 4:** Input $t_r$ = $t_f$ = 3ns

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ | | | $T_A = -40°C$ to $+85°C$ | | Units | $C_L$ (pF) |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | |
| $t_{PLH}$ | Propagation Delay Time | 2.7 | | 5.4 | 10.1 | 1.0 | 12.5 | ns | 15 |
| $t_{PHL}$ | | | | 7.9 | 13.6 | 1.0 | 16.0 | | 50 |
| | | 3.3 ± 0.3 | | 4.1 | 6.2 | 1.0 | 7.5 | | 15 |
| | | | | 6.6 | 9.7 | 1.0 | 11.0 | | 50 |
| $t_{OSLH}$ | Output to Output Skew | 2.7 | | | 1.5 | | 1.5 | ns | 50 |
| $t_{OSHL}$ | (Note 5) | 3.3 | | | 1.5 | | 1.5 | | |

**Note 5:** Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$

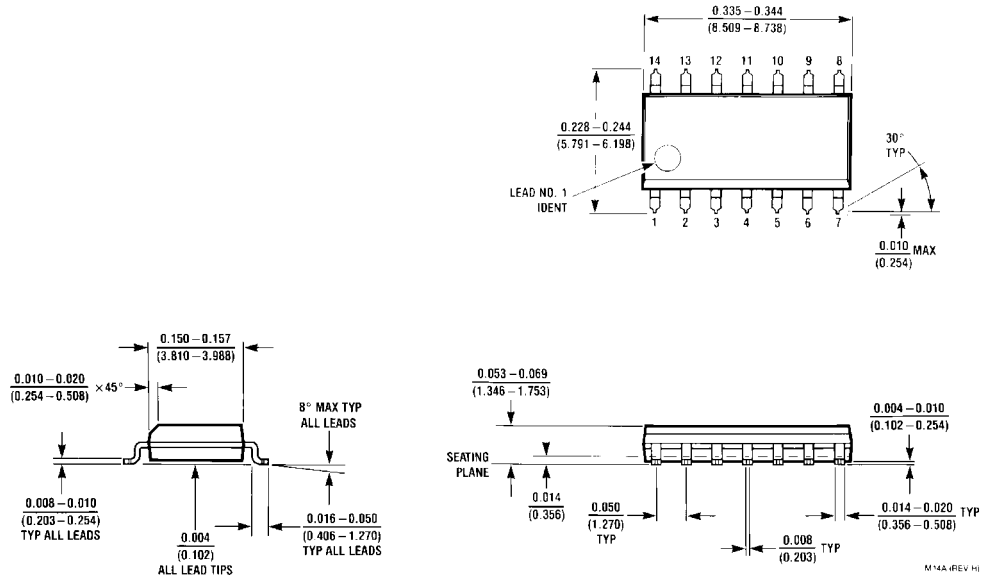
## Capacitance

| Symbol | Parameter | $T_A = +25°C$ | | | $T_A = -40°C$ to $+85°C$ | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $C_{IN}$ | Input Capacitance | | 4 | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (Note 6) | | 19 | | | | pF |

**Note 6:** $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

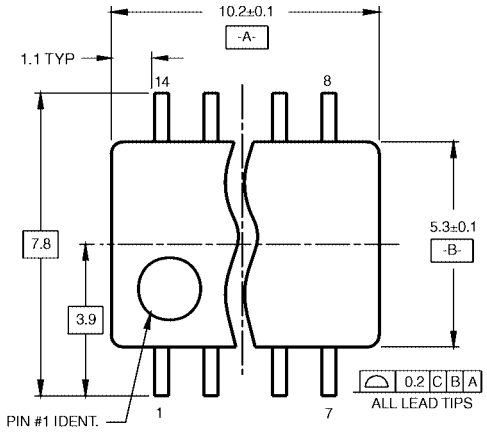
Average operating current can be obtained by the equation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$

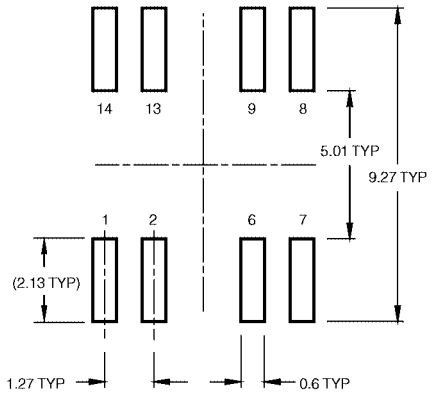
## Physical Dimensions inches (millimeters) unless otherwise noted



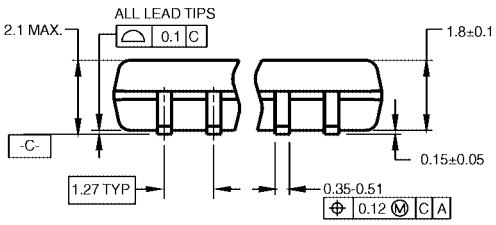

**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M14A**

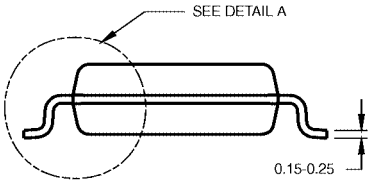
## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




LAND PATTERN RECOMMENDATION




DIMENSIONS ARE IN MILLIMETERS

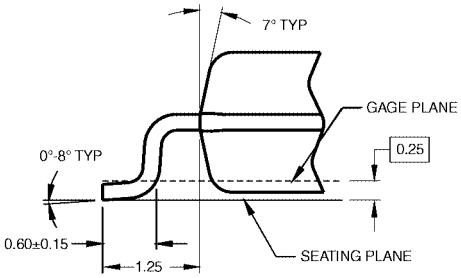
NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

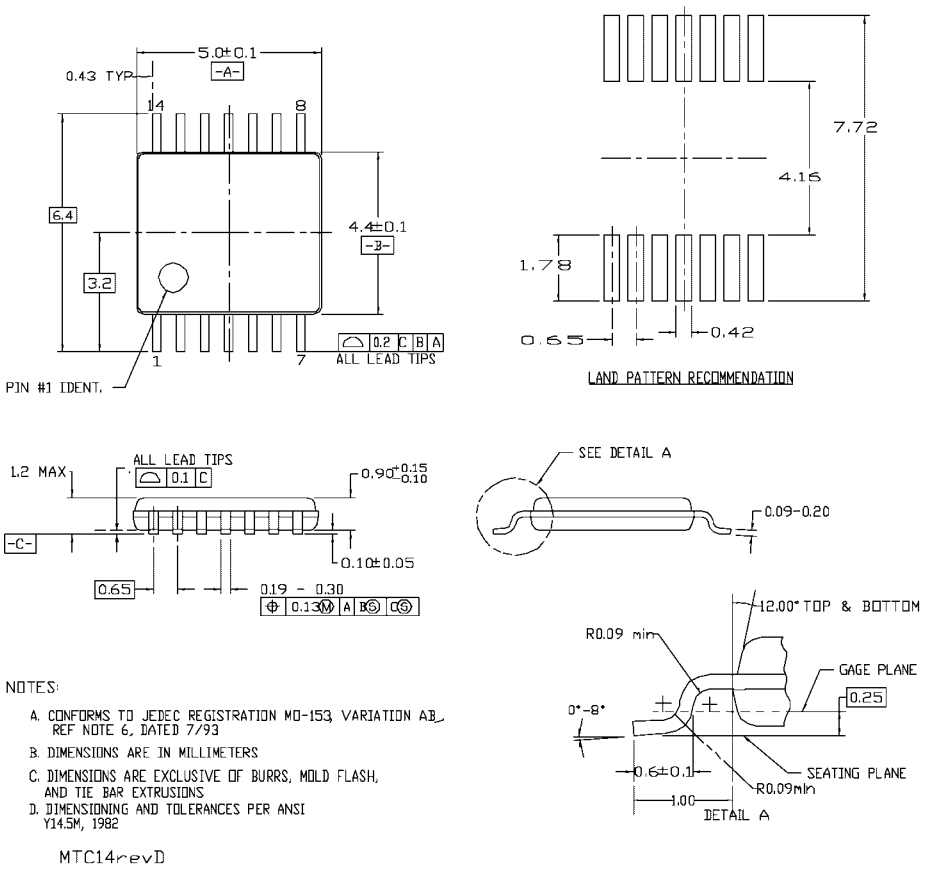
M14DRevB1




DETAIL A

**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC14**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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