DATA SHEET

74LVT623

3.3 V octal transceiver with dual enable, non-inverting (3-State)

Product specification
Supersedes data of 1999 Jul 09
File under Integrated Circuits, IC24 Handbook

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3.3 V octal transceiver with dual enable, non-inverting (3-State)

74LVT623

FEATURES

- Separate controls for data flow in each direction
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-State
- Power-up reset
- Latch-up protection exceeds 500 mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74LVT623 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The 74LVT623 is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

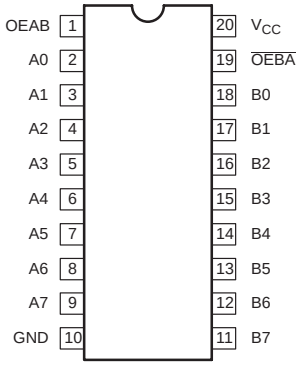
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 3.3 V	2.3 2.5	ns
C_{IN}	Input capacitance	V_I = 0 V or 3.0 V	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6 V	0.13	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
20-Pin Plastic SO	–40 °C to +85 °C	74LVT623D	SOT163-1
20-Pin Plastic SSOP Type II	–40 °C to +85 °C	74LVT623DB	SOT339-1
20-Pin Plastic TSSOP Type I	–40 °C to +85 °C	74LVT623PW	SOT360-1

PIN CONFIGURATION

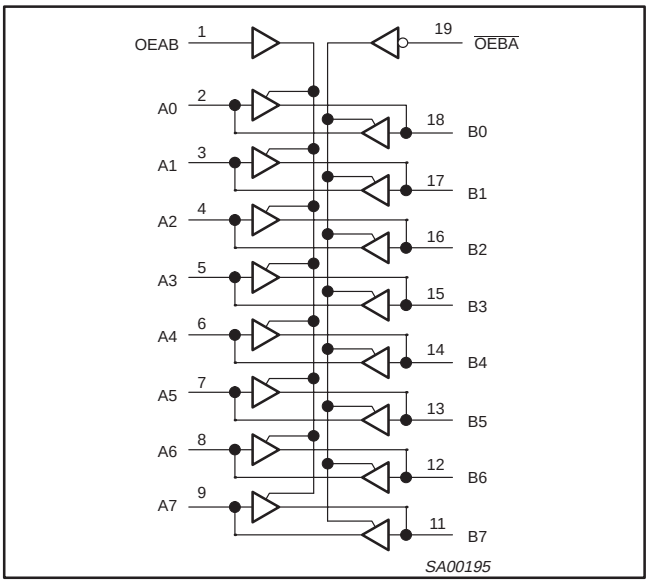


SA00189

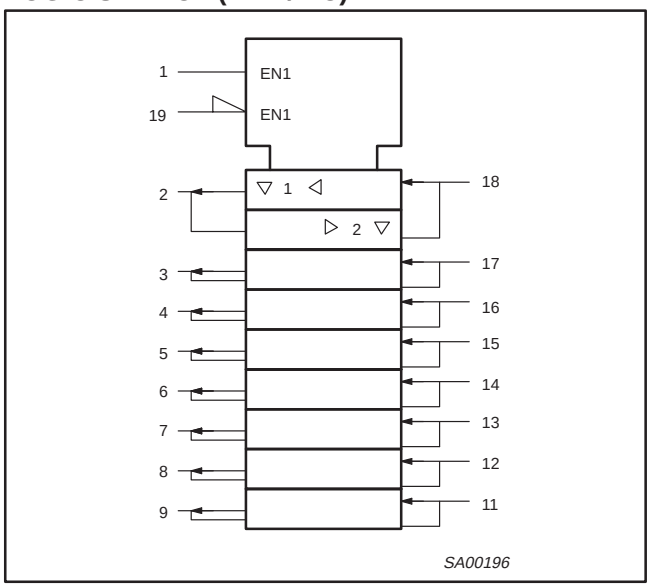
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output enable input, A side to B side (active-High)
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs/outputs (A side)
18, 17, 16, 15, 14, 13, 12, 11	B0 – B7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Output enable input, B side to A side (active-Low)
10	GND	Ground (0 V)
20	V_{CC}	Positive supply voltage

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	An	Bn
L	L	An = Bn	Inputs
H	H	Inputs	Bn = An
H	L	Z	Z
L	H	An = Bn	Bn = An

H = High voltage level
L = Low voltage level
Z = High impedance “off” state

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1 kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS Temp = –40 °C to +85 °C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA			–0.9	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6 V; I_{OH} = –100 µA		V_{CC}–0.2	V_{CC}–0.1		V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5		
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.2		
V_{OL}	Low-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA			0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA			0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 16 mA			0.25	0.4	
		V_{CC} = 3.0 V; I_{OL} = 32 mA			0.3	0.5	
		V_{CC} = 3.0 V; I_{OL} = 64 mA			0.4	0.55	
V_{RST}	Power-up output low voltage[5]	V_{CC} = 3.6 V; I_O = 1 mA; V_I = GND or V_{CC}			0.13	0.55	V
I_I	Input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	Control pins		±0.1	±1	µA
		V_{CC} = 0 or 3.6 V; V_I = 5.5 V			1	10	
		V_{CC} = 3.6 V; V_I = 5.5 V	I/O Data pins[4]		1	20	
		V_{CC} = 3.6 V; V_I = V_{CC}			0.1	1	
		V_{CC} = 3.6 V; V_I = 0			–1	–5	
I_{OFF}	Output off current	V_{CC} = 0 V; V_I or V_O = 0 to 4.5 V			1	±100	µA
I_{HOLD}	Bus Hold current A or B ports	V_{CC} = 3 V; V_I = 0.8 V		75	150		µA
		V_{CC} = 3 V; V_I = 2.0 V		–75	–150		
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	V_O = 5.5 V; V_{CC} = 3.0 V			60	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$/OE = Don't care			15	±100	µA
I_{CCH}	Quiescent supply current	V_{CC} = 3.6 V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}		V_{CC} = 3.6 V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			3	12	
I_{CCZ}		V_{CC} = 3.6 V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0			0.13	0.19	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3 V to 3.6 V; One input at V_{CC} –0.6 V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.

AC CHARACTERISTICS

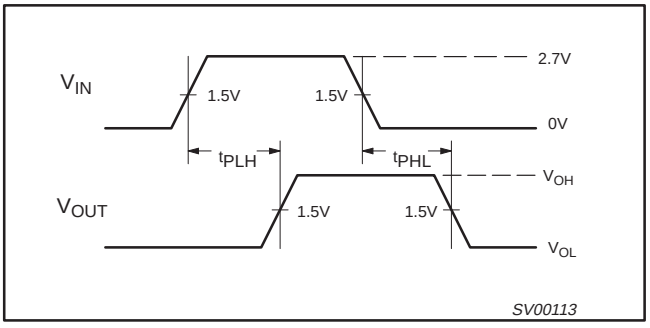
GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3 V ±0.3 V			V_{CC} = 2.7 V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	1	1.0 1.0	2.3 2.5	3.5 3.7	4.3 4.1	ns
t_{PZH} t_{PZL}	Output enable time $\overline{OEBA}$ to An	2 3	1.0 1.1	3.7 3.7	5.9 5.9	7.6 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time $\overline{OEBA}$ to An	2 3	1.8 1.8	3.6 3.2	5.0 4.5	5.5 4.6	ns
t_{PZH} t_{PZL}	Output enable time OEAB to Bn	2 3	1.0 1.4	4.2 4.3	6.3 6.2	7.8 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time OEAB to Bn	2 3	2.3 2.0	3.9 3.6	6.1 5.3	6.9 5.8	ns

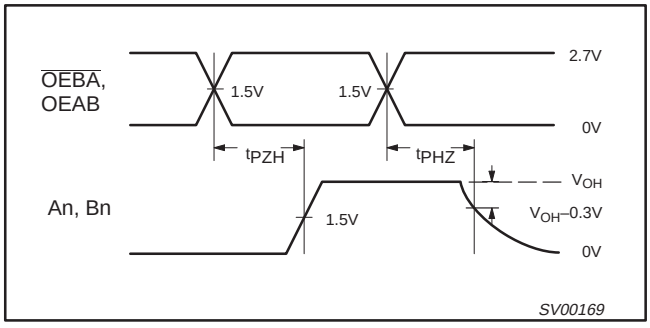
NOTE:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25°C.

AC WAVEFORMS

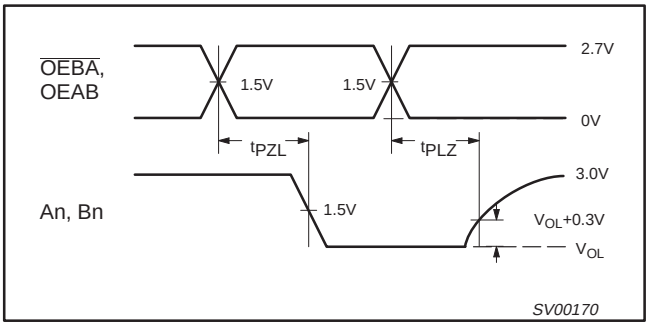
V_M = 1.5 V, V_{IN} = GND to 2.7 V



Waveform 1. Propagation Delay for Non-Inverting Output

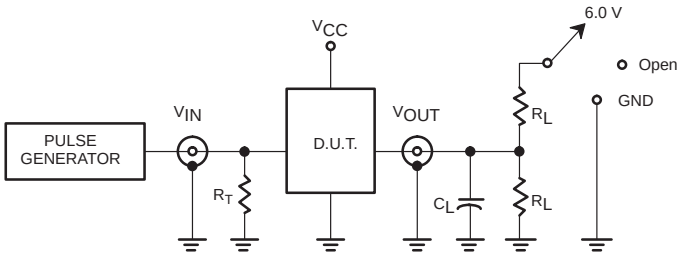


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level

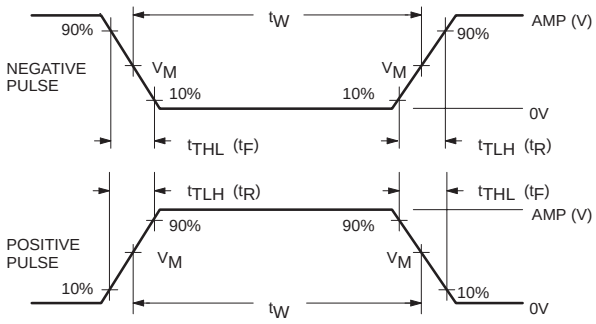


Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5 V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

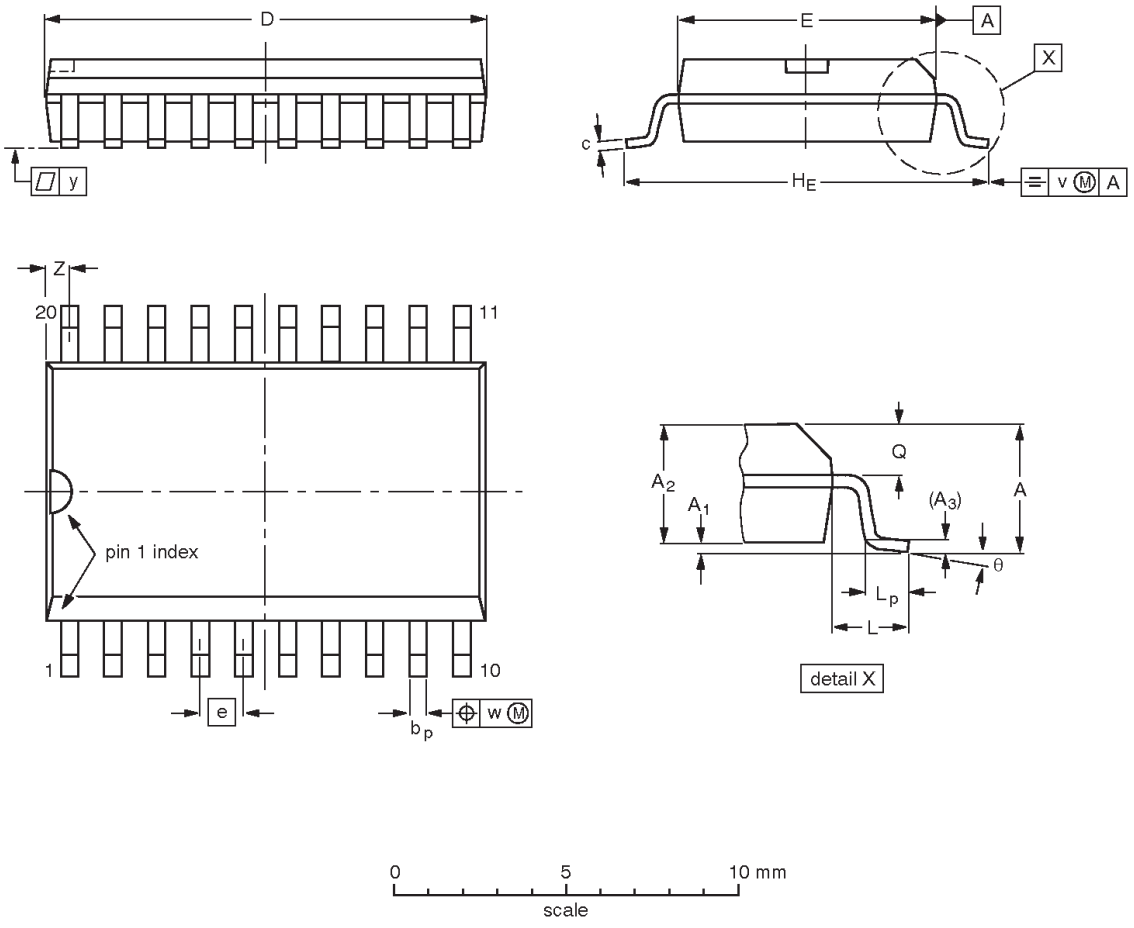
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

SV00092

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

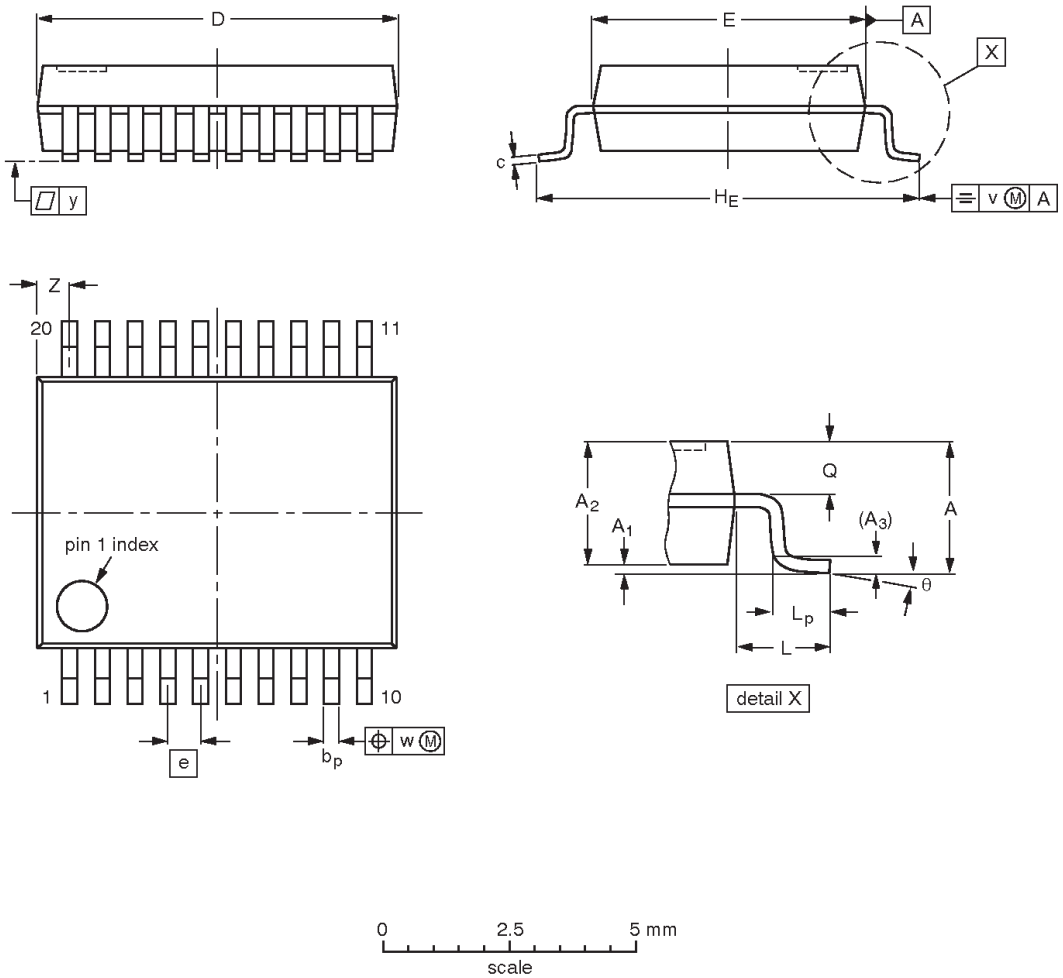
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013				~~97-05-22~~ 99-12-27

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

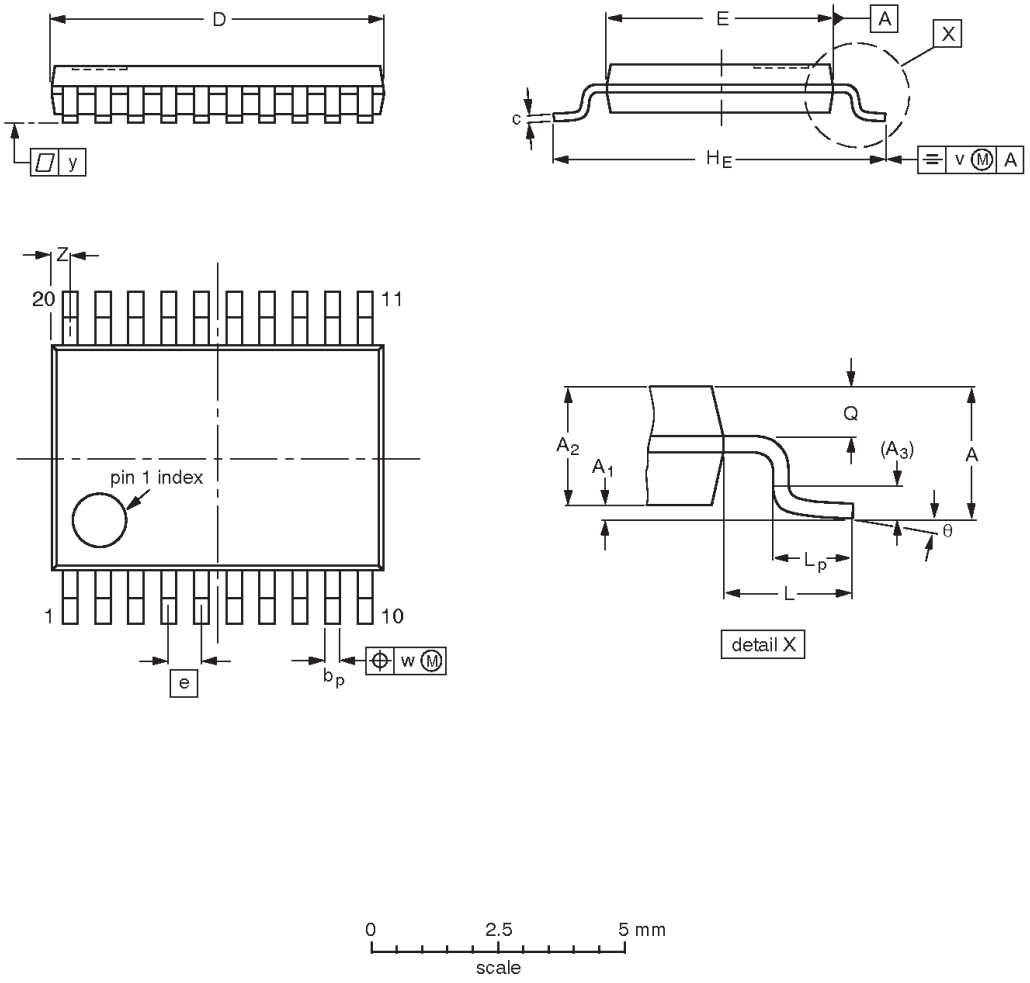
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150				~~95-02-04~~ 99-12-27

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153				~~95-02-04~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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