DATA SHEET

74LVT1403

3.3V combined 8-bit bus receiver and 4-bit bus driver

Product specification

1998 Nov 12

IC23 Data Handbook

Philips Semiconductors

PHILIPS

3.3V combined 8-bit bus receiver and 4-bit bus driver

74LVT1403

FEATURES

- 4-bit 74LVT125-like bus driver
- 8-bit 74LVT14-like Schmitt trigger
- Bus drive +64mA/–32mA
- 7 bus inputs with common inversion control pin
- 32-pin TSSOP footprint
- DE pin with resistive pull up and active LOW for easier live insertion
- DE pin includes Schmitt trigger with typical 0.6V hysteresis

DESCRIPTION

The 74LVT1403 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device combines the functionality of a 4-bit data path bus driver and 8-bit Schmitt trigger bus receiver, along with control logic in one 32-pin package.

The receiver inputs are Schmitt trigger type capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. The receiver outputs are 74LVT14 style with +32mA/–20mA drive capability. The receiver inputs include the bus hold feature.

The driver outputs feature power-up in 3-State/live insertion capability and are all controlled by the A/B, EN1, and EN2 control pins. The driver inputs include the bus hold feature.

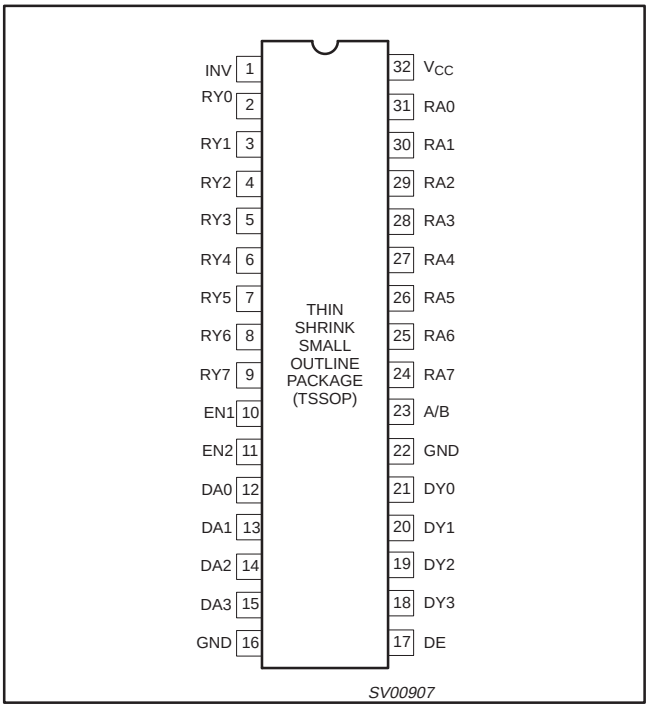
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	4.5	ns
t_{PHL}	Propagation delay An to Yn	C_L = 50pF; V_{CC} = 3.3V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
I_{CC}	Total supply current	Outputs low, V_{CC} = 3.6V	4	mA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
32-pin plastic TSSOP	–40°C to +85°C	74LVT1403 DR	74LVT1403 DR	SOT487-1

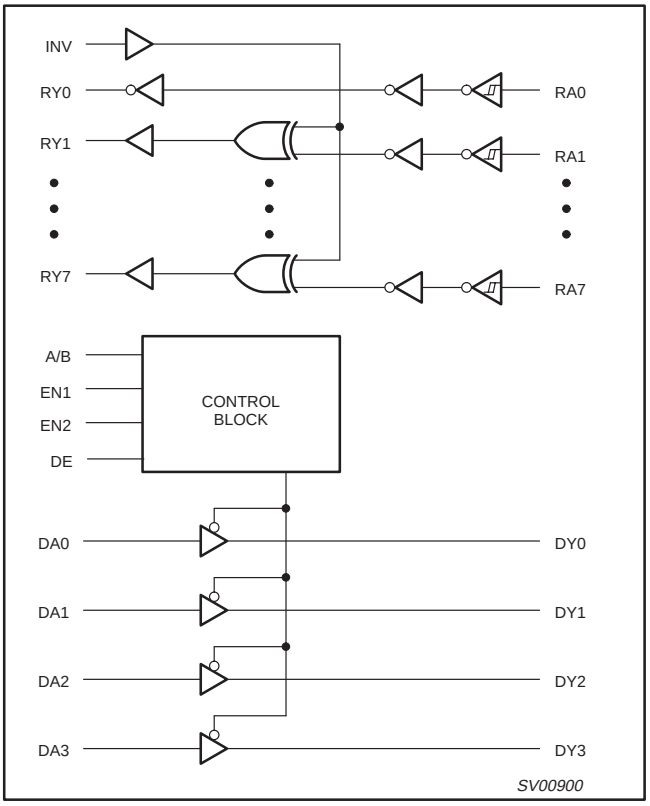
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
31, 30, 29, 28, 27, 26, 25, 24	RA0–RA7	Receive Data inputs
2, 3, 4, 5, 6, 7, 8, 9	RY0–RY7	Receive Data outputs
12, 13, 14, 15	DA0–DA3	Driver Data inputs
21, 20, 19, 18	DY0–DY3	Driver Data outputs
10, 11	EN1, EN2	Driver Output enables
23	A/B	Mode control for enables
1	INV	Inversion control
16, 22	GND	Ground (0V)
32	V_{CC}	Positive supply voltage
17	DE	Driver output enable active LOW with resistive pull up

LOGIC SYMBOL



FUNCTION TABLE – RECEIVER

INPUTS		OUTPUTS	
RA0–RA7	INV	RY0	RY1–RY7
L	X	H	—
H	X	L	—
L	L	—	L
H	L	—	H
L	H	—	H
H	H	—	L

H = High voltage level
L = Low voltage level
X = Don't care
— = Reported on different line

FUNCTION TABLE – DRIVER

CONTROL INPUTS				OUTPUT CONDITION
DE	A/B	EN1	EN2	DY Status
L	L	L	L	A
L	L	X	H	Z
L	L	H	X	Z
L	H	H	H	A
L	H	X	L	Z
L	H	L	X	Z
H	X	X	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state
A = Active

DATA PATH IN ACTIVE MODE

INPUT	OUTPUT
DAn	DYn
L	L
H	H

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_I	DC input voltage[3]		–0.5 to +7.0	V
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DYn DC output current	Output in Low state	128	mA
		Output in High state	–64	mA
	RYn DC output current	Output in Low state	–32	mA
		Output in High state	64	mA
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		2.7	3.6	V
V_I	Input voltage		0	5.5	V
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level Input voltage			0.8	V
I_{OH}	High-level output current	DYn		–32	mA
		RYn		–20	mA
I_{OL}	Low-level output current	DYn		32	mA
		RYn		32	mA
	Low-level output current; current duty cycle ≤ 50%, f ≥ 1kHz	DYn		64	mA
$\Delta t/\Delta V$	Input transition rise or fall rate; Outputs enabled			10	ns/V
T_{amb}	Operating free-air temperature range		–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER		TEST CONDITIONS		LIMITS Temp = -40°C to +85°C MIN	TYP[1]	MAX	UNIT
V_{T+}	Positive-going threshold	RAn	V_{CC} = 3.3V		1.5	1.7	2.0	V
V_{T-}	Negative-going threshold	RAn	V_{CC} = 3.3V		0.9	1.1	1.3	V
ΔV_T	Hysteresis	RAn	V_{CC} = 3.3V		0.4	0.6		V
V_{IK}	Input clamp voltage		V_{CC} = 2.7V; I_{IK} = –18mA				–1.2	V
V_{OH}	High-level output voltage	RYn	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2			V
			V_{CC} = 2.7V; I_{OH} = –6mA		2.4			V
			V_{CC} = 3.0V; I_{OH} = –20mA		2.0			V
		DYn	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}–0.2	V_{CC}–0.1		V
			V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		V
			V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.2		V
V_{OL}	Low-level output voltage	RYn	V_{CC} = 2.7V; I_{OL} = 100µA				0.2	V
			V_{CC} = 2.7V; I_{OL} = 24mA				0.5	V
			V_{CC} = 3.0V; I_{OL} = 32mA				0.5	V
		DYn	V_{CC} = 2.7V; I_{OL} = 100µA			0.1	0.2	V
			V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	V
			V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	V
			V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	V
			V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	V
I_I	Input leakage current		V_{CC} = 0 or 3.6V; V_I = 5.5V	All inputs		1	10	µA
			V_{CC} = 3.6V; V_I = V_{CC}	Control pins		±0.1	±1	
			V_{CC} = 3.6V; V_I = GND	INV, EN1, EN2, A/B		±0.1	±1	
				DE		–60	–100	
			V_{CC} = 3.6V; V_I = V_{CC}	Data port[4]		0.1	1	
			V_{CC} = 3.6V; V_I = GND			–1	–5	µA
I_{OFF}	Output off current		V_{CC} = 0V; V_I or V_O = 0 to 4.5V			1	±100	µA
I_{HOLD}	Bus hold current RA and DA inputs		V_{CC} = 3V; V_I = 0.8V		75	150		µA
			V_{CC} = 3V; V_I = 2.0V		–75	–150		µA
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$		V_O = 5.5V; V_{CC} = 3.0V			60	125	µA
$I_{PU/PD}$	Power-up/down 3-State output current[3]		$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; EN1, EN2, A/B, DE = Don't care			±1	±100	µA
I_{OZH}	3-State output high current		V_{CC} = 3.6V; V_O = 3.0V			1	5	µA
I_{OZL}	3-State output low current		V_{CC} = 3.6V; V_O = 0.5V			–1	–5	µA
I_{CCH}	Quiescent supply current		V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.13	0.19	mA
I_{CCL}			V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4	11	mA
I_{CCZ}			V_{CC} = 3.6V; Outputs Disabled, V_I = GND or V_{CC}, I_O = 0[5]			0.13	0.19	mA
ΔI_{CC}	Additional supply current per input pin[2]		V_{CC} = 3V to 3.6V; One input at V_{CC}–0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V, a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. All RYn outputs High. All DYn outputs pulled up to V_{CC} or pulled down to ground.

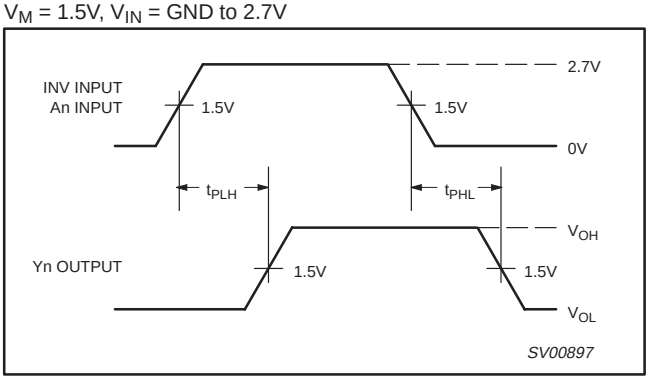
AC CHARACTERISTICS

RAn = Receive inputs; Ryn = Receive outputs
DAn = Driver inputs; Dyn = Driver outputs

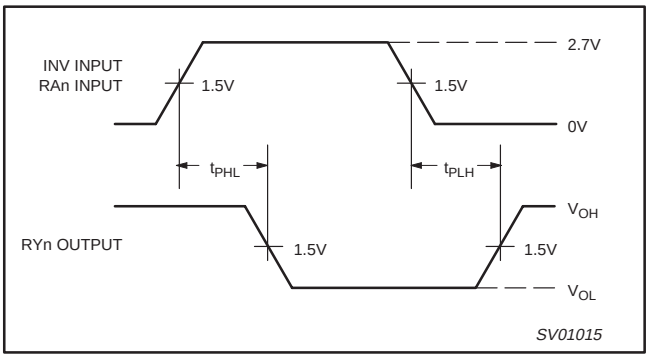
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ± 0.3V			V_{CC} = 2.7V	
			MIN	TYP	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay RA0 to RY0	2	1.0 1.0	3.8 3.2	5.7 4.4	6.9 4.3	ns
t_{PLH} t_{PHL}	Propagation delay RAn to RYn (n = 1 to 7)	1, 2	2.0 2.0	4.5 4.0	6.7 5.7	7.8 6.4	ns
t_{PLH} t_{PHL}	Propagation delay Invert to RYn	1, 2	2.0 2.0	4.0 3.6	6.3 5.5	7.1 7.4	ns
t_{PLH} t_{PHL}	Propagation delay DAn to DYn	1	1.0 1.0	3.1 2.0	4.2 3.0	4.7 3.5	ns
t_{PZH} t_{PZL}	Output enable time ENn to DYn with A/B = 0	3	2.0 2.0	4.8 4.3	7.1 6.7	9.6 7.4	ns
t_{PZH} t_{PZL}	Output enable time ENn to DYn with A/B = 1	4	2.0 2.0	4.3 4.0	6.5 6.1	7.8 6.6	ns
t_{PHZ} t_{PLZ}	Output disable time ENn to DYn with A/B =0	3	2.0 2.0	4.7 4.0	7.1 6.3	8.2 6.9	ns
t_{PHZ} t_{PLZ}	Output disable time ENn to DYn with A/B =1	4	2.0 2.0	4.2 4.0	6.8 6.2	8.3 6.5	ns
t_{PZH} t_{PZL}	Output enable time A/B to DYn	3, 4	2.0 2.0	5.0 4.2	8.6 6.5	9.5 7.2	ns
t_{PHZ} t_{PLZ}	Output disable time A/B to DYn	3, 4	2.0 2.0	5.1 4.3	7.5 6.2	7.7 6.6	ns
t_{PZH} t_{PZL}	Output enable time DE to DYn	3	2.0 2.0	5.1 4.7	7.6 6.8	9.1 7.5	ns
t_{PHZ} t_{PLZ}	Output disable time DE to DYn	3	2.0 2.0	5.9 4.9	9.3 7.2	9.7 7.7	ns

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 2.7V



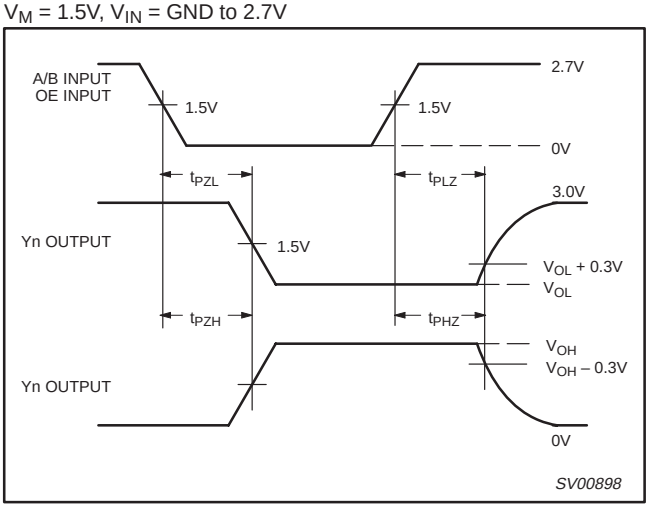
Waveform 1. Input (An) to Output (Yn) Propagation Delays



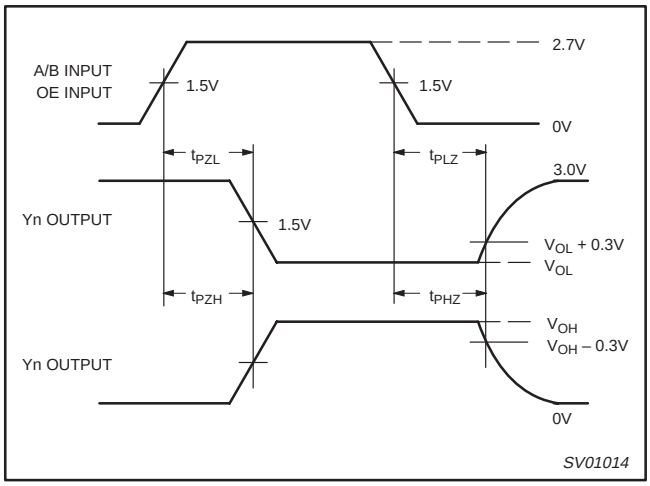
Waveform 2. Input (An) to Output (Yn) Propagation Delays

AC WAVEFORMS (Continued)

V_M = 1.5V, V_{IN} = GND to 2.7V

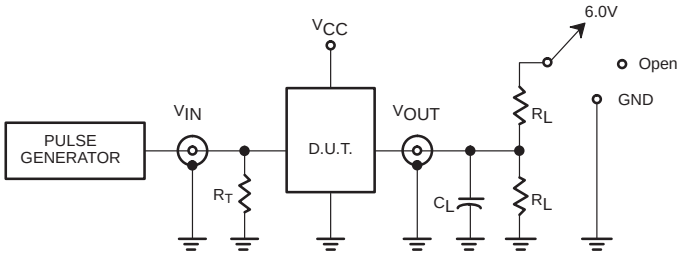


Waveform 3. 3-State Output Enable and Disable Times

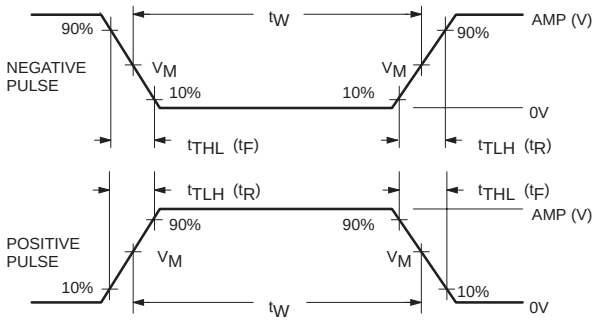


Waveform 4. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

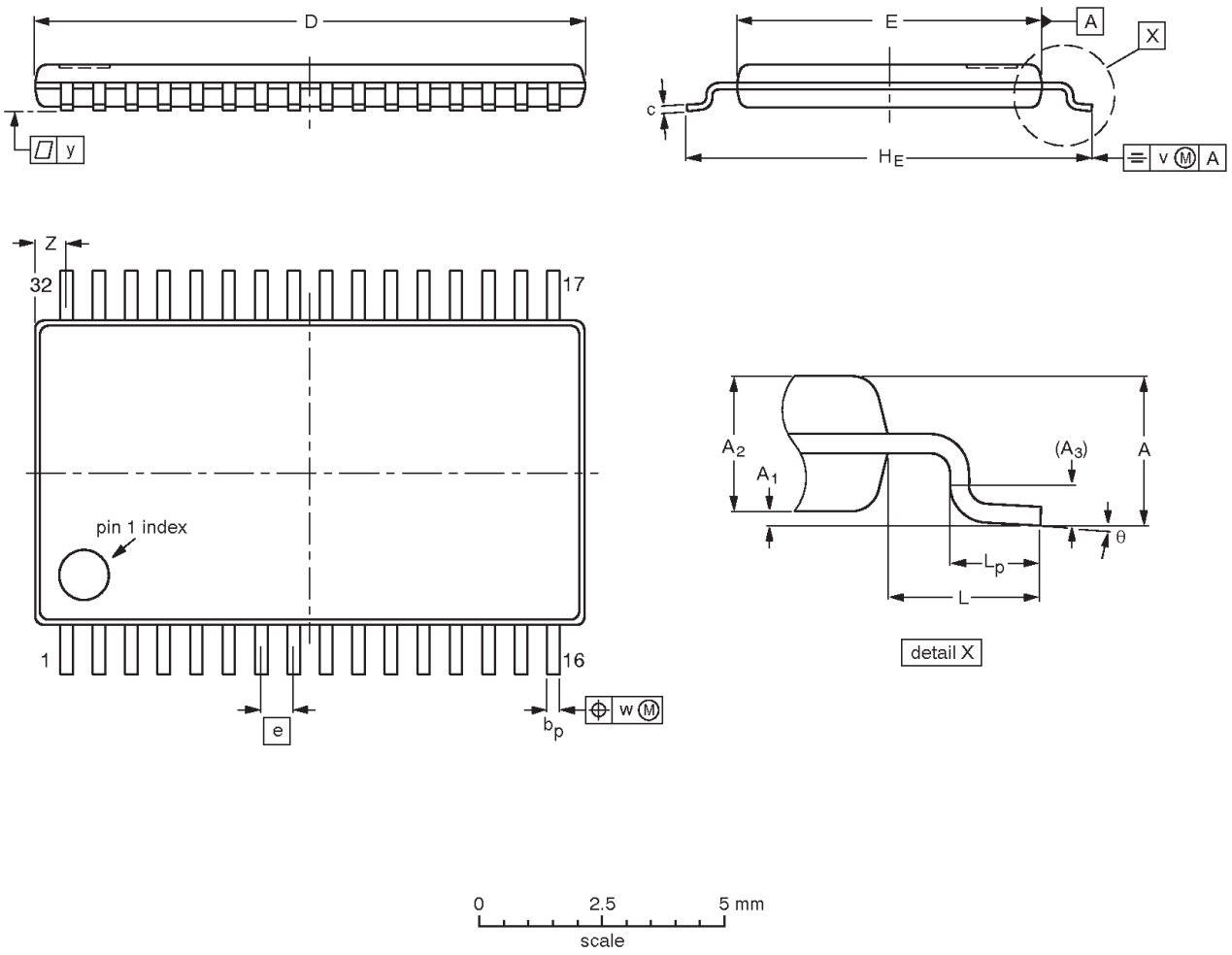
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SV00092

TSSOP32: plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm **SOT487-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.10 10.90	6.20 6.00	0.65	8.30 7.90	1.00	0.75 0.50	0.20	0.10	0.10	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT487-1		MO-153				97-06-11

NOTES

3.3V combined 8-bit bus receiver and 4-bit bus driver

74LVT1403

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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