

# 74LVT574; 74LVTH574

3.3 V octal D-type flip-flop; 3-state

Rev. 03 — 23 March 2006

Product data sheet

## 1. General description

The 74LVT574; 74LVTH574 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by the clock (pin CP) and output enable (pin  $\overline{OE}$ ) control gates. The state of each D input (one setup time before the LOW-to-HIGH clock transition) is transferred to the corresponding flip-flops Q output.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors.

The active LOW output enable (pin  $\overline{OE}$ ) controls all eight 3-state buffers independent of the clock operation.

When pin  $\overline{OE}$  is LOW, the stored data appears at the outputs. When pin  $\overline{OE}$  is HIGH, the outputs are in the high-impedance OFF-state, which means they will neither drive nor load the bus.

## 2. Features

- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- 3-state outputs for bus interfacing
- Common output enable control
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up reset
- Power-up 3-state
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883, method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$

**PHILIPS**

### 3. Quick reference data

**Table 1. Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PLH}$	LOW-to-HIGH propagation delay CP to Qn	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	-	3.6	-	ns
$t_{PHL}$	HIGH-to-LOW propagation delay CP to Qn	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	-	4.3	-	ns
$C_i$	input capacitance	$V_I = 0\text{ V}$ or $3.0\text{ V}$	-	4	-	pF
$C_o$	output capacitance	outputs disabled; $V_O = 0\text{ V}$ or $3.0\text{ V}$	-	8	-	pF
$I_{CC}$	quiescent supply current	outputs disabled; $V_{CC} = 3.6\text{ V}$	-	0.13	-	mA

### 4. Ordering information

**Table 2. Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74LVT574D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT574DB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT574PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH574D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH574DB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVTH574PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

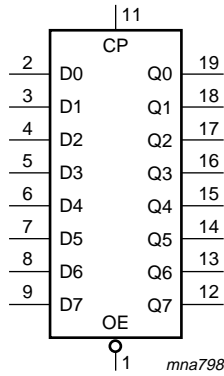


Fig 1. Logic symbol

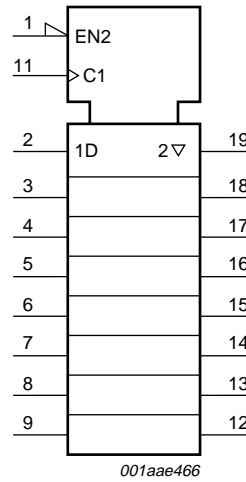


Fig 2. IEC logic symbol

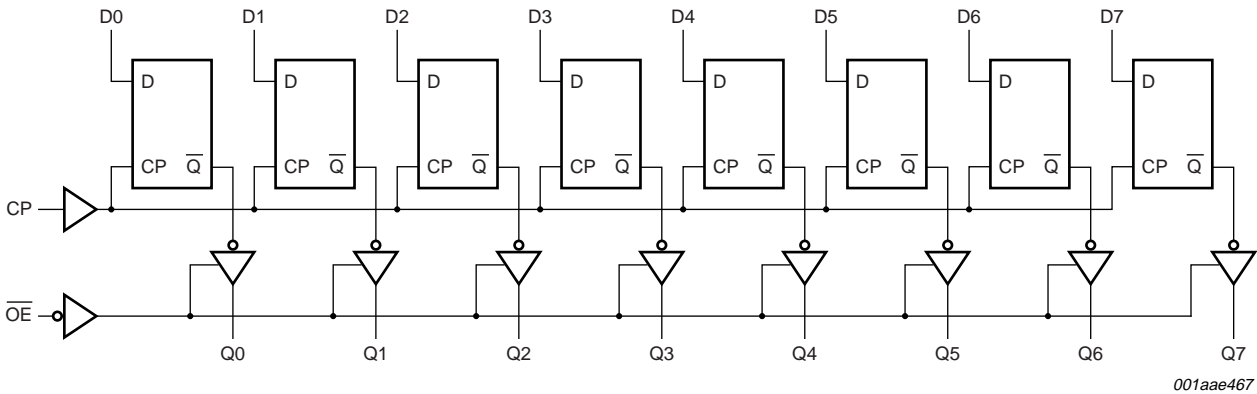
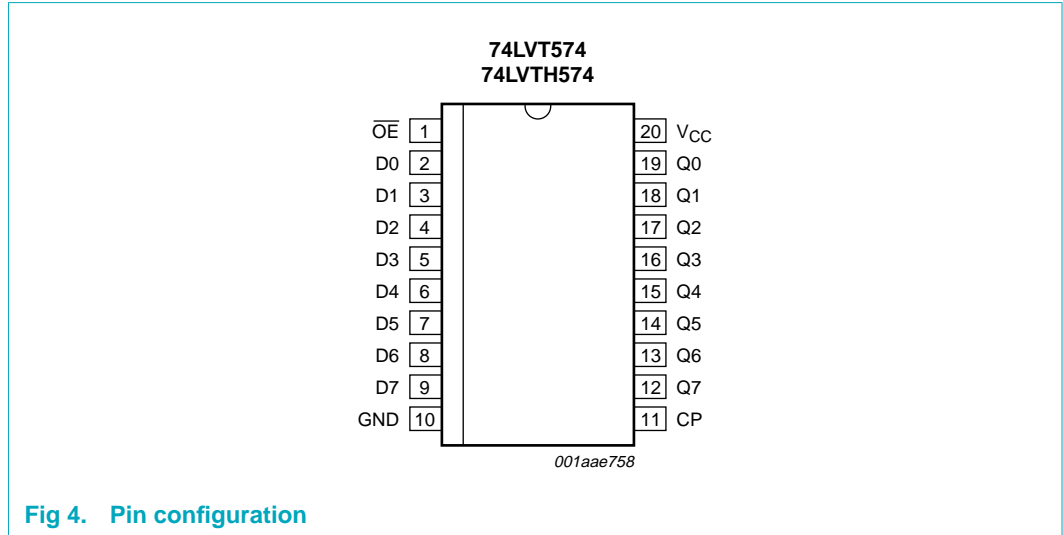


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$\overline{OE}$	1	output enable input (active LOW)
D0	2	data input D0
D1	3	data input D1
D2	4	data input D2
D3	5	data input D3
D4	6	data input D4
D5	7	data input D5
D6	8	data input D6
D7	9	data input D7
GND	10	ground (0 V)
CP	11	clock pulse input (active rising edge)
Q7	12	data output Q7
Q6	13	data output Q6
Q5	14	data output Q5
Q4	15	data output Q4
Q3	16	data output Q3
Q2	17	data output Q2
Q1	18	data output Q1
Q0	19	data output Q0
V <sub>CC</sub>	20	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4. Function table [1]

Operating mode	Control		Input	Internal register	Output
	OE	CP	Dn		Qn
Load and read register	L	↑	l	L	L
			h	H	H
Hold	L	NC	X	NC	NC
Disable outputs	H	X	X	NC	Z

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 ↑ = LOW-to-HIGH clock transition;  
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition;  
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition;  
 Z = high-impedance OFF-state;  
 NC = no change;  
 X = don't care.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-	-50	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-	-50	mA
$I_O$	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		[2] -	150	°C

- [1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$V_{IH}$	HIGH-state input voltage		2.0	-	-	V
$V_{IL}$	LOW-state input voltage		-	-	0.8	V
$I_{OH}$	HIGH-state output current		-	-	-32	mA
$I_{OL}$	LOW-state output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz	-	-	64	mA
$T_{amb}$	ambient temperature	in free air	-40	-	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ [1]							
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-	-0.9	-1.2	V	
$V_{OH}$	HIGH-state output voltage	$V_{CC} = 2.7\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$	$V_{CC} - 0.1$	-	V	
		$V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V	
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.2	-	V	
$V_{OL}$	LOW-state output voltage	$V_{CC} = 2.7\text{ V}$					
		$I_{OL} = 100\text{ }\mu\text{A}$	-	0.1	0.2	V	
		$I_{OL} = 24\text{ mA}$	-	0.3	0.5	V	
		$V_{CC} = 3.0\text{ V}$					
		$I_{OL} = 16\text{ mA}$	-	0.25	0.4	V	
		$I_{OL} = 32\text{ mA}$	-	0.3	0.5	V	
$V_{RST}$	power-up output low voltage	$V_{CC} = 3.6\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = \text{GND}$ or $V_{CC}$	[2]	0.13	0.55	V	
$I_{LI}$	input leakage current	all input pins	$V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	1	10	$\mu\text{A}$
		control pins	$V_{CC} = 3.6\text{ V}$ ; $V_{CC}$ or GND	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		data pins	$V_{CC} = 3.6\text{ V}$	[3]			
			$V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$
			$V_I = 0\text{ V}$	-	-1	-5	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$	-	1	$\pm 100$	$\mu\text{A}$	

**Table 7. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{\text{HOLD}}$	bus hold current data input	$V_{\text{CC}} = 3 \text{ V}$	[4]				
		$V_{\text{I}} = 0.8 \text{ V}$	75	150	-	$\mu\text{A}$	
		$V_{\text{I}} = 2.0 \text{ V}$	-75	-150	-	$\mu\text{A}$	
		$V_{\text{CC}} = 0 \text{ V to } 3.6 \text{ V}$	[4]				
$I_{\text{EX}}$	external current into output	$V_{\text{CC}} = 3.6 \text{ V}$	$\pm 500$	-	-	$\mu\text{A}$	
		output in HIGH-state when $V_{\text{O}} > V_{\text{CC}}$ ; $V_{\text{O}} = 5.5 \text{ V}$ and $V_{\text{CC}} = 3.0 \text{ V}$	-	60	125	$\mu\text{A}$	
$I_{\text{O(pu/pd)}}$	power-up/power-down output current	$V_{\text{CC}} \leq 1.2 \text{ V}$ ; $V_{\text{O}} = 0.5 \text{ V to } V_{\text{CC}}$ ; $V_{\text{I}} = \text{GND or } V_{\text{CC}}$ ; $\text{OE} = \text{don't care}$	[5]	1	$\pm 100$	$\mu\text{A}$	
$I_{\text{OZ}}$	OFF-state output current	$V_{\text{CC}} = 3.6 \text{ V}$ ; $V_{\text{I}} = V_{\text{IH}} \text{ or } V_{\text{IL}}$					
		output HIGH: $V_{\text{O}} = 3.0 \text{ V}$	-	1	5	$\mu\text{A}$	
		output LOW: $V_{\text{O}} = 0.5 \text{ V}$	-	1	-5	$\mu\text{A}$	
$I_{\text{CC}}$	quiescent supply current	$V_{\text{CC}} = 3.6 \text{ V}$ ; $V_{\text{I}} = \text{GND or } V_{\text{CC}}$ ; $I_{\text{O}} = 0 \text{ A}$					
		outputs HIGH	-	0.13	0.19	$\text{mA}$	
		outputs LOW	-	3	12	$\text{mA}$	
		outputs disabled	[6]	-	0.13	0.19	$\text{mA}$
$\Delta I_{\text{CC}}$	additional quiescent supply current	per input pin; $V_{\text{CC}} = 3 \text{ V to } 3.6 \text{ V}$ ; one input at $V_{\text{CC}} - 0.6 \text{ V}$ and other inputs at $V_{\text{CC}}$ or GND	[7]	-	0.1	0.2	$\text{mA}$
$C_{\text{i}}$	input capacitance	$V_{\text{I}} = 0 \text{ V or } 3.0 \text{ V}$	-	4	-	$\text{pF}$	
$C_{\text{o}}$	output capacitance	outputs disabled; $V_{\text{O}} = 0 \text{ V or } 3.0 \text{ V}$	-	8	-	$\text{pF}$	

[1] Typical values are measured at  $V_{\text{CC}} = 3.3 \text{ V}$  and  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ .

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at  $V_{\text{CC}}$  or GND.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This parameter is valid for any  $V_{\text{CC}}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{\text{CC}} = 1.2 \text{ V}$  to  $V_{\text{CC}} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$  only.[6]  $I_{\text{CC}}$  is measured with outputs pulled to  $V_{\text{CC}}$  or GND.[7] This is the increase in supply current for each input at the specified voltage level other than  $V_{\text{CC}}$  or GND.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**Voltages are referenced to ground (GND = 0 V); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{amb}} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ [1]						
$t_{\text{PLH}}$	LOW-to-HIGH propagation delay CP to Qn	see <a href="#">Figure 5</a>				
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	1.7	3.6	5.4	ns
		$V_{\text{CC}} = 2.7 \text{ V}$	-	-	6.2	ns

**Table 8. Dynamic characteristics ...continued**

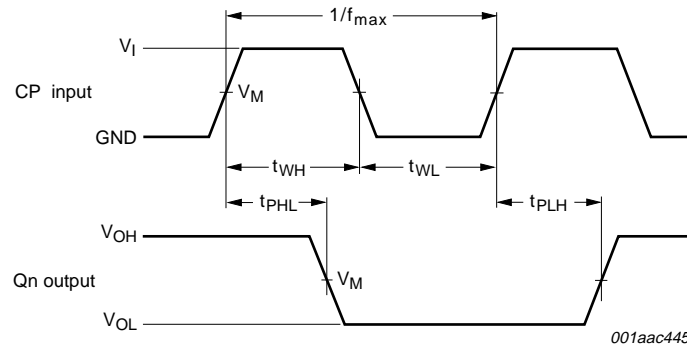
Voltages are referenced to ground ( $GND = 0\text{ V}$ ); for test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$	HIGH-to-LOW propagation delay CP to Qn	see <a href="#">Figure 5</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.4	4.3	5.9	ns
		$V_{CC} = 2.7\text{ V}$	-	-	6.6	ns
$t_{PZH}$	output enable time to HIGH-state	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.9	4.8	ns
		$V_{CC} = 2.7\text{ V}$	-	-	5.9	ns
$t_{PZL}$	output enable time to LOW-state	see <a href="#">Figure 7</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.3	3.4	5.1	ns
		$V_{CC} = 2.7\text{ V}$	-	-	6.2	ns
$t_{PHZ}$	output disable time from HIGH-state	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.9	4.0	5.5	ns
		$V_{CC} = 2.7\text{ V}$	-	-	5.9	ns
$t_{PLZ}$	output disable time from LOW-state	see <a href="#">Figure 7</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.7	3.2	4.5	ns
		$V_{CC} = 2.7\text{ V}$	-	-	4.5	ns
$t_{su(H)}$	setup time Dn to CP HIGH	see <a href="#">Figure 8</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	ns
		$V_{CC} = 2.7\text{ V}$	2.4	-	-	ns
$t_{su(L)}$	setup time Dn to CP LOW	see <a href="#">Figure 8</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.0	-	-	ns
		$V_{CC} = 2.7\text{ V}$	2.4	-	-	ns
$t_{h(H)}$	hold time Dn to CP HIGH	see <a href="#">Figure 8</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.3	-	-	ns
		$V_{CC} = 2.7\text{ V}$	0	-	-	ns
$t_{h(L)}$	hold time Dn to CP LOW	see <a href="#">Figure 8</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.3	-	-	ns
		$V_{CC} = 2.7\text{ V}$	0	-	-	ns
$t_{WH}$	pulse width CP HIGH	see <a href="#">Figure 5</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.3	-	-	ns
		$V_{CC} = 2.7\text{ V}$	3.3	-	-	ns
$t_{WL}$	pulse width CP LOW	see <a href="#">Figure 5</a>				
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.3	-	-	ns
		$V_{CC} = 2.7\text{ V}$	3.3	-	-	ns
$f_{max}$	maximum input clock frequency	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ; see <a href="#">Figure 5</a>	150	-	-	MHz

[1] Typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .



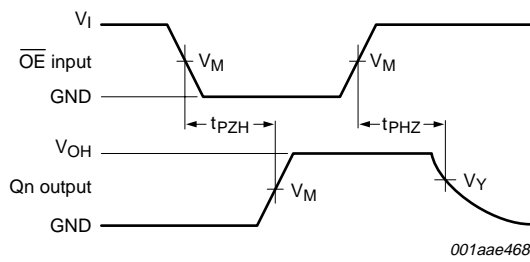
12. Waveforms



Measurement points are given in [Table 9](#)

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

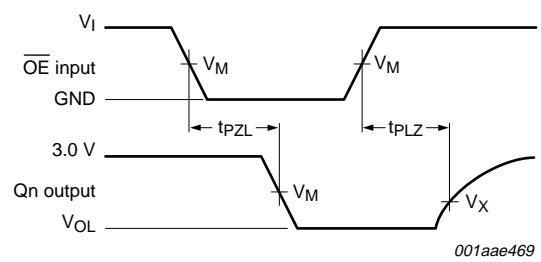
**Fig 5. Propagation delay clock input (CP) to output (Qn), pulse width clock (CP) and maximum clock frequency**



Measurement points are given in [Table 9](#)

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

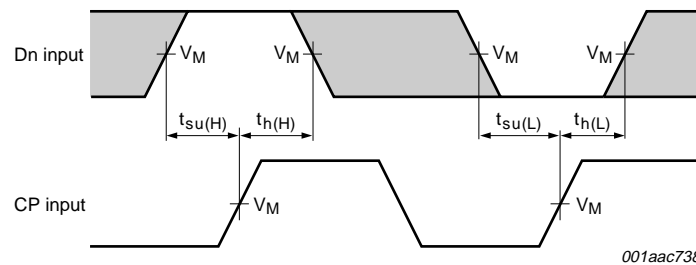
**Fig 6. Output enable time to HIGH-state and output disable time from HIGH-state**



Measurement points are given in [Table 9](#)

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

**Fig 7. Output enable time to LOW-state and output disable time from LOW-state**



Measurement points are given in [Table 9](#)

**Remark:** The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 8. Data setup and hold times**

Table 9. Measurement points

Input	Output		
$V_M$	$V_M$	$V_X$	$V_Y$
1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$

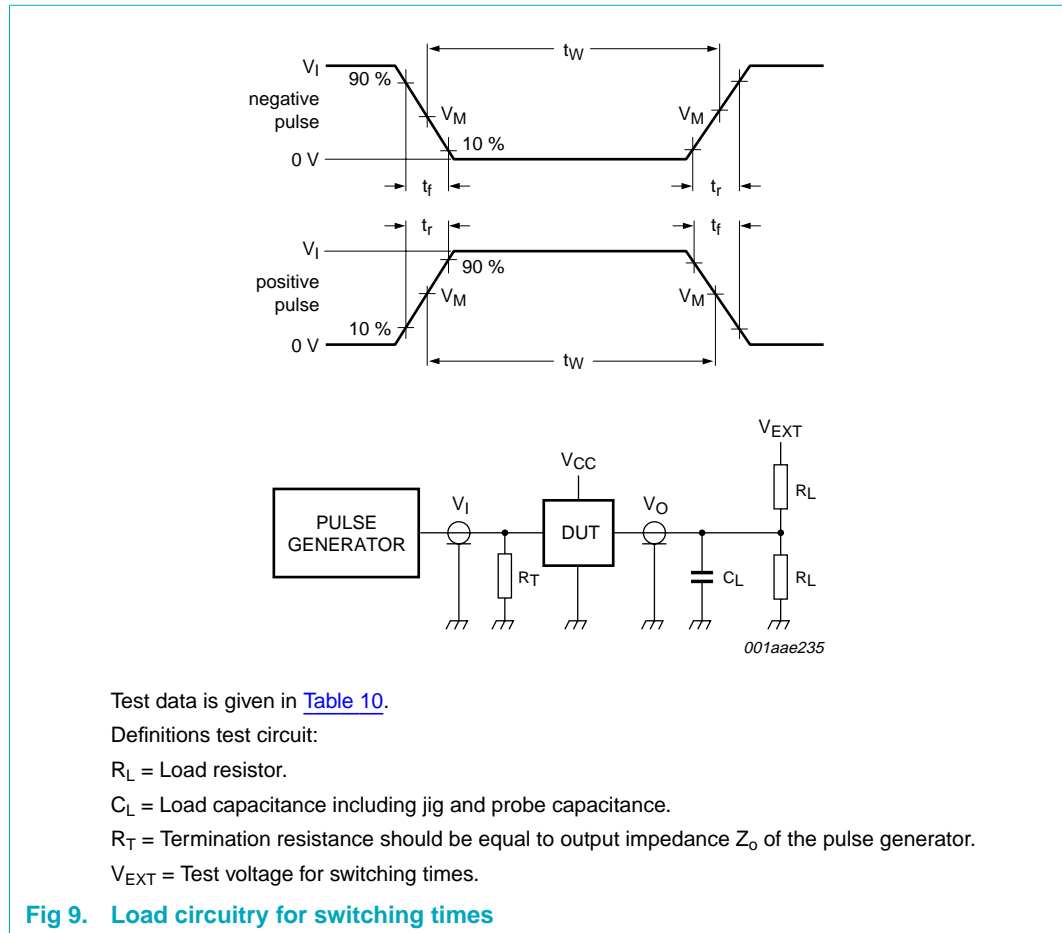


Table 10. Test data

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open

13. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

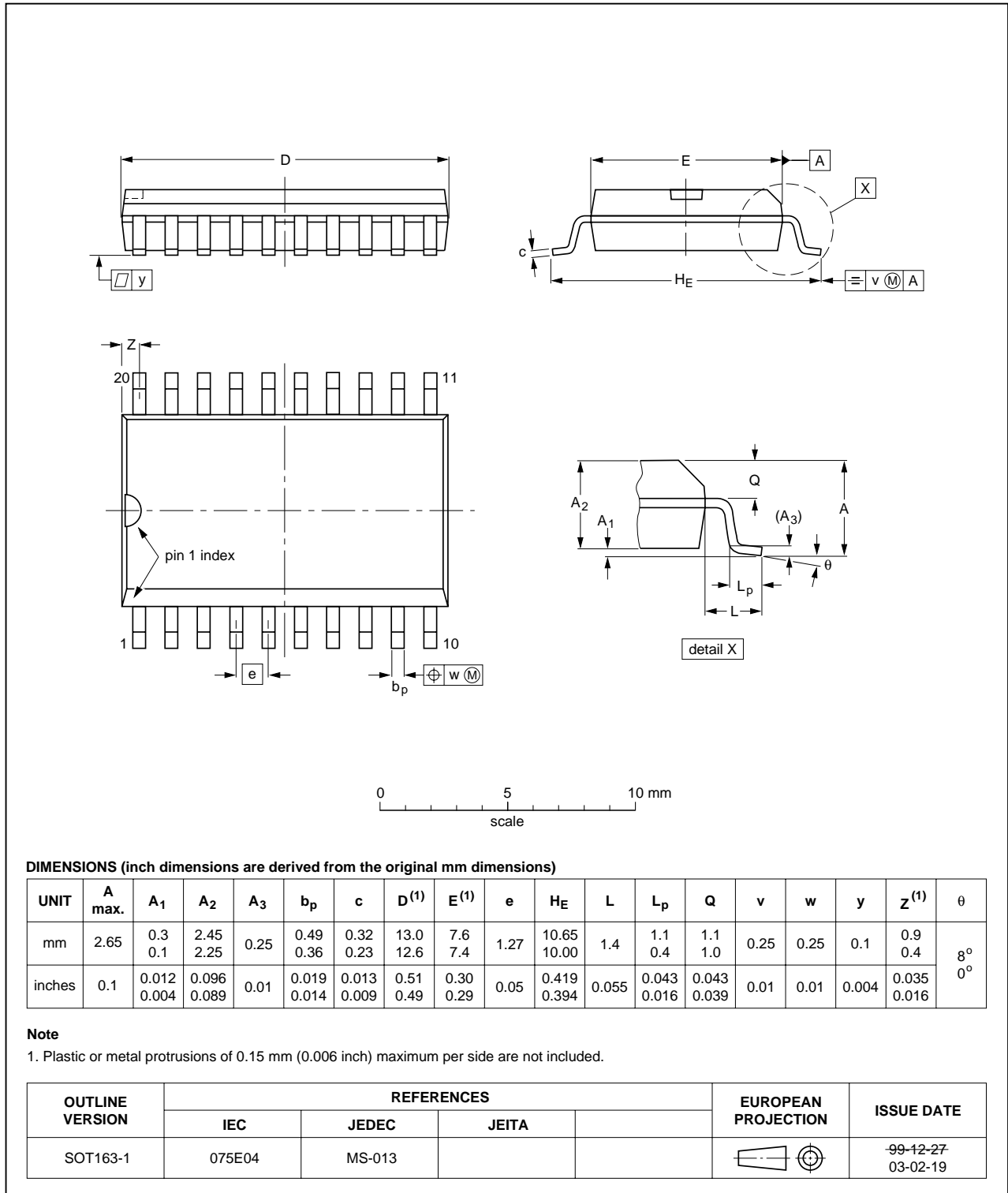


Fig 10. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

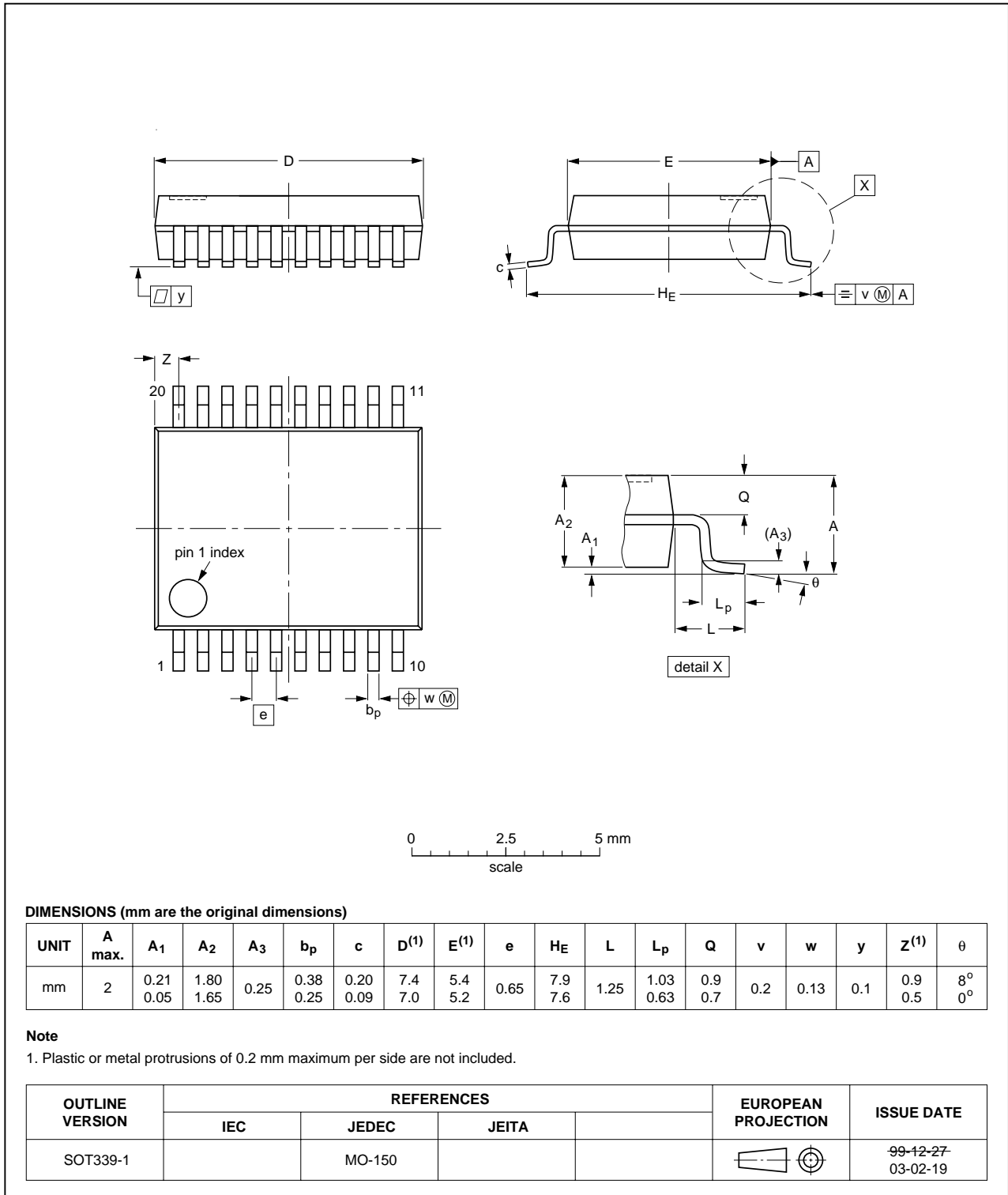


Fig 11. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

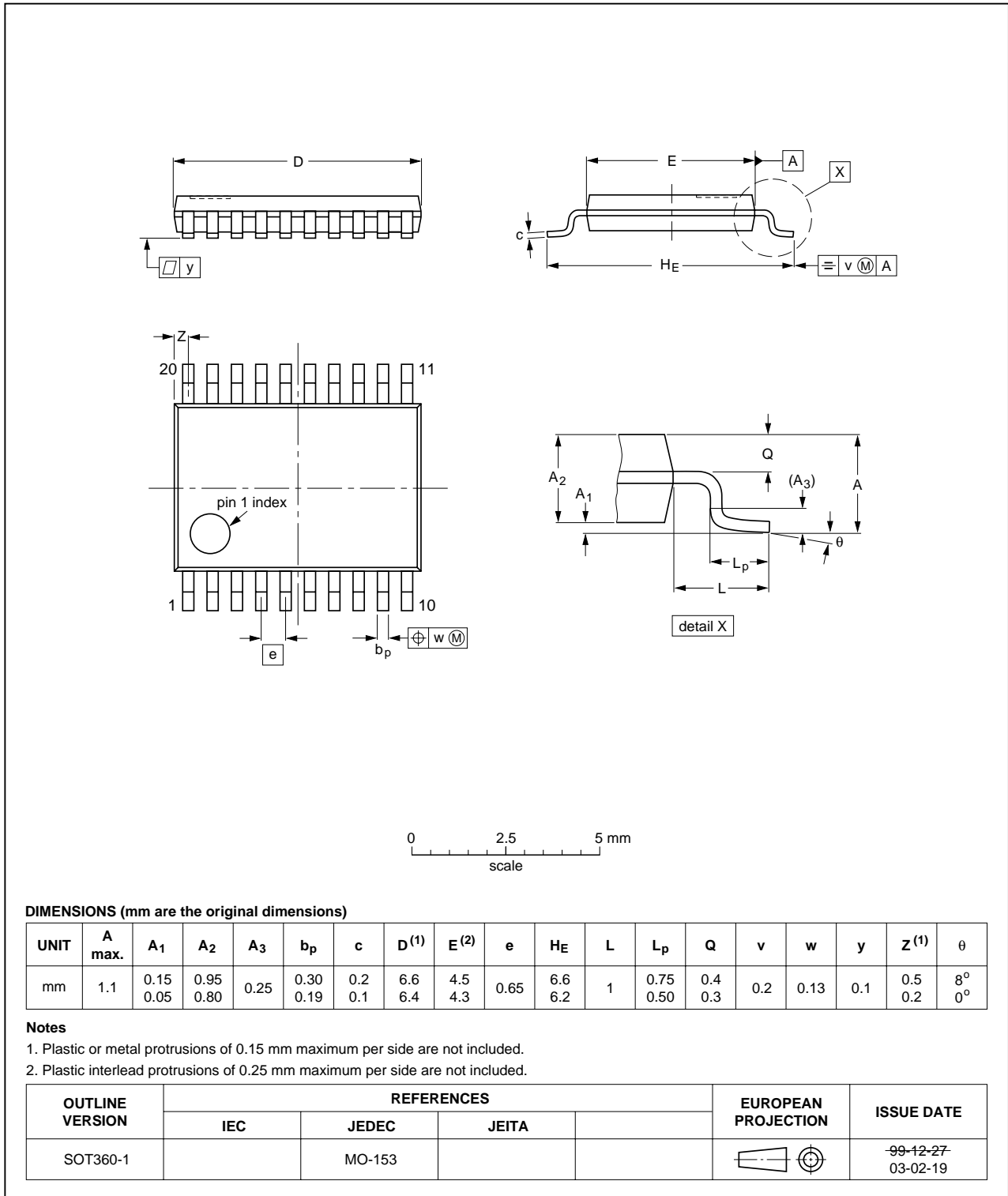


Fig 12. Package outline SOT360-1 (TSSOP20)

## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH574_3	20060323	Product data sheet	-	74LVT574_2 (9397 750 03542)
Modifications:		<ul style="list-style-type: none"> <li>The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 2 "Features"</a>: Changed JEDEC Std. 17 into JESD78</li> <li><a href="#">Table 2 "Ordering information"</a>: added type numbers 74LVTH574D, 74LVTH574DB and 74LVTH574PW.</li> </ul>		
74LVT574_2 (9397 750 03542)	19980219	product specification	-	74LVT574_1
74LVT574_1	19951114	product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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