FAIRCHILD SEMICONDUCTOR™

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74LVTH322374
Low Voltage 32-Bit D-Type Flip-Flop with 3-STATE Outputs and 25Ω Series Resistors in the Outputs (Preliminary)

General Description

The LVTH322374 contains thirty-two non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 32-bit operation.

The LVTH322374 is designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH322374 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These flip-flops are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH322374 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

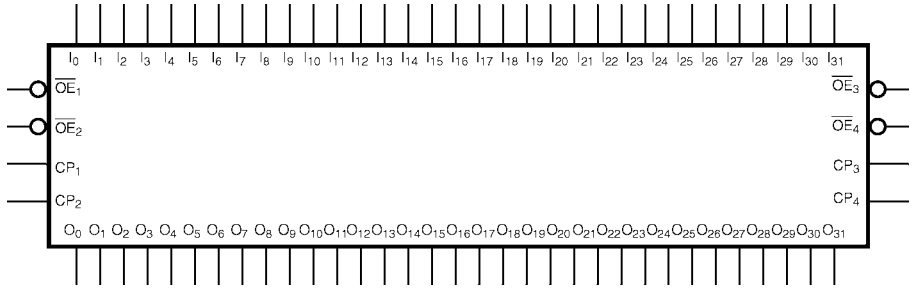
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Power Down high impedance provides glitch-free bus loading
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

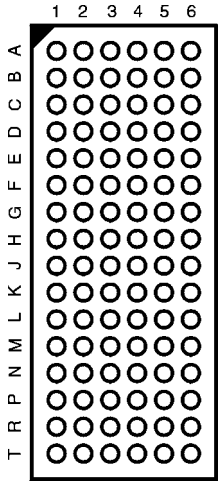
Order Number	Package Number	Package Description
74LVTH322374GX (Note 1)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]

Note 1: BGA package available in Tape and Reel only.

Logic Symbol



Connection Diagram



(Top Thru View)

Pin Descriptions for FBGA

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
CP_n	Clock Pulse Input
I_0–I_{31}	Inputs
O_0–O_{31}	3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	O_1	O_0	$\overline{OE}_1$	CP_1	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC1}	V_{CC1}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC1}	V_{CC1}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	$\overline{OE}_2$	CP_2	I_{15}	I_{14}
J	O_{17}	O_{16}	$\overline{OE}_3$	CP_3	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC2}	V_{CC2}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC2}	V_{CC2}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	$\overline{OE}_4$	CP_4	I_{31}	I_{30}

Truth Tables

Inputs			Outputs
CP_1	$\overline{OE}_1$	I_0–I_7	O_0–O_7
↗	L	H	H
↗	L	L	L
L	L	X	O_o
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	I_8–I_{15}	O_8–O_{15}
↗	L	H	H
↗	L	L	L
L	L	X	O_o
X	H	X	Z

Inputs			Outputs
CP_3	$\overline{OE}_3$	I_{16}–I_{23}	O_{16}–O_{23}
↗	L	H	H
↗	L	L	L
L	L	X	O_o
X	H	X	Z

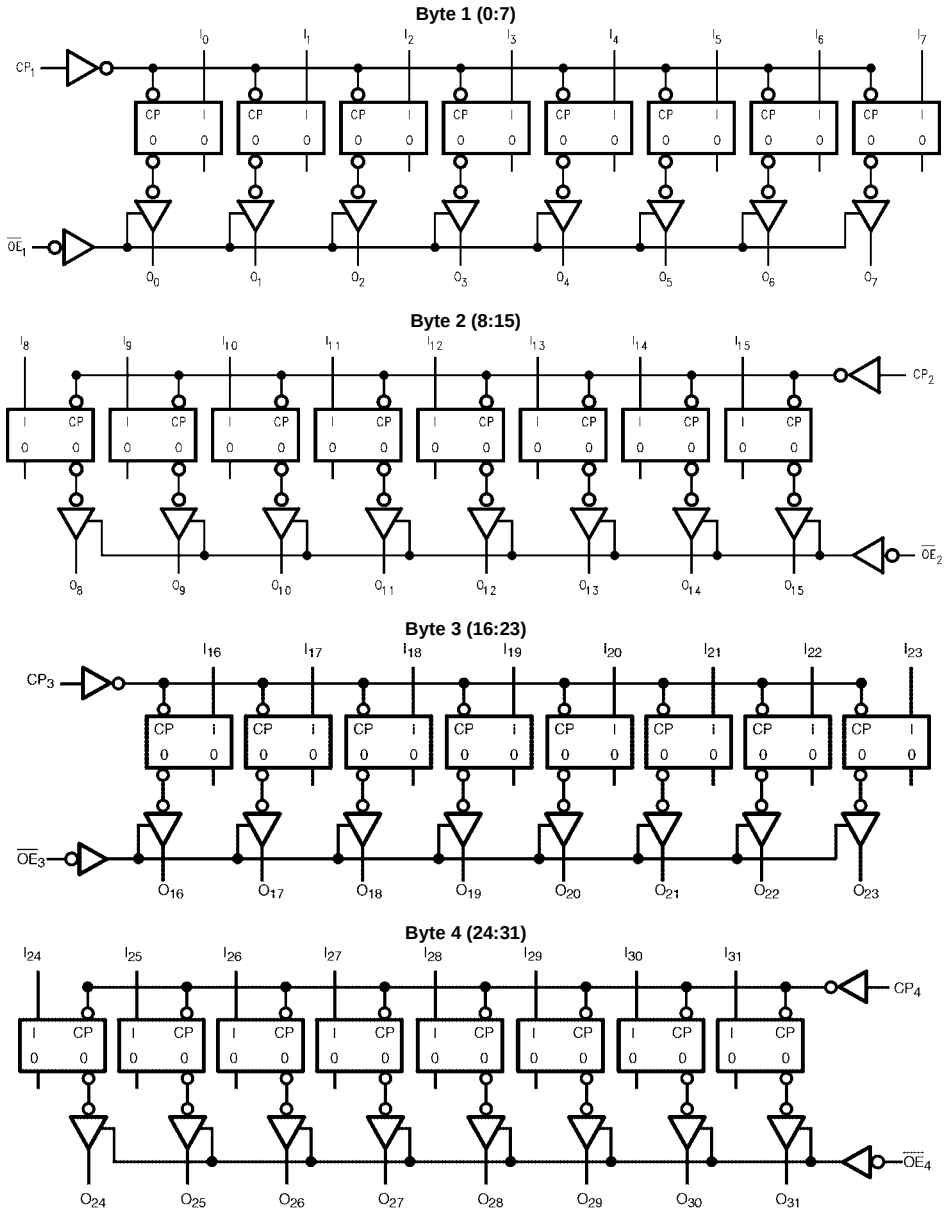
Inputs			Outputs
CP_4	$\overline{OE}_4$	I_{24}–I_{31}	O_{24}–O_{31}
↗	L	H	H
↗	L	L	L
L	L	X	O_o
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance
O_o = Previous O_o before HIGH-to-LOW of CP

Functional Description

The LVTH322374 consists of thirty-two edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}_n$ input does not affect the state of the flip-flops.

Logic Diagrams



V_{CC1} is associated with Bytes 1 and 2.

V_{CC2} is associated with Bytes 3 and 4.

Note: Please note that these diagrams are provided for the understanding of logic operation and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	–0.5 to +4.6		V
V_I	DC Input Voltage	–0.5 to +7.0		V
V_O	DC Output Voltage	–0.5 to +7.0	Output in 3-STATE	V
		–0.5 to +7.0	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	–65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		–32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = –40°C to +85°C Min	T_A = –40°C to +85°C Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		–1.2	V	I_I = –18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le$ 0.1V or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	$V_O \ge V_{CC}$ – 0.1V
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC} – 0.2		V	I_{OH} = –100 µA
			3.0	2.0			I_{OH} = –12 mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	I_{OL} = 100 µA
			3.0		0.8		I_{OL} = 12 mA
$I_{I(HOLD)}$	Bushold Input Minimum Drive		3.0	75		µA	V_I = 0.8V
				–75			V_I = 2.0V
$I_{I(OD)}$	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 4)
				–500			(Note 5)
I_I	Input Current		3.6		10	µA	V_I = 5.5V
		Control Pins	3.6		±1		V_I = 0V or V_{CC}
		Data Pins	3.6		–5		V_I = 0V
					1		V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0		±100	µA	0V ≤ V_I or $V_O \le$ 5.5V
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current		0–1.5V		±100	µA	V_O = 0.5V to 3.0V, V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		–5	µA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	V_O = 3.0V
I_{OZH+}	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le$ 5.5V
I_{CCH}	Power Supply Current	(V_{CC1} or V_{CC2})	3.6		0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current	(V_{CC1} or V_{CC2})	3.6		5	mA	Outputs LOW
I_{CCZ}	Power Supply Current	(V_{CC1} or V_{CC2})	3.6		0.19	mA	Outputs Disabled

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Max		
I_{CCZ}+	Power Supply Current (V_{CC1} or V_{CC2})	3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (V_{CC1} or V_{CC2}) (Note 6)	3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 8)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		–0.8		V	(Note 8)

Note 7: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

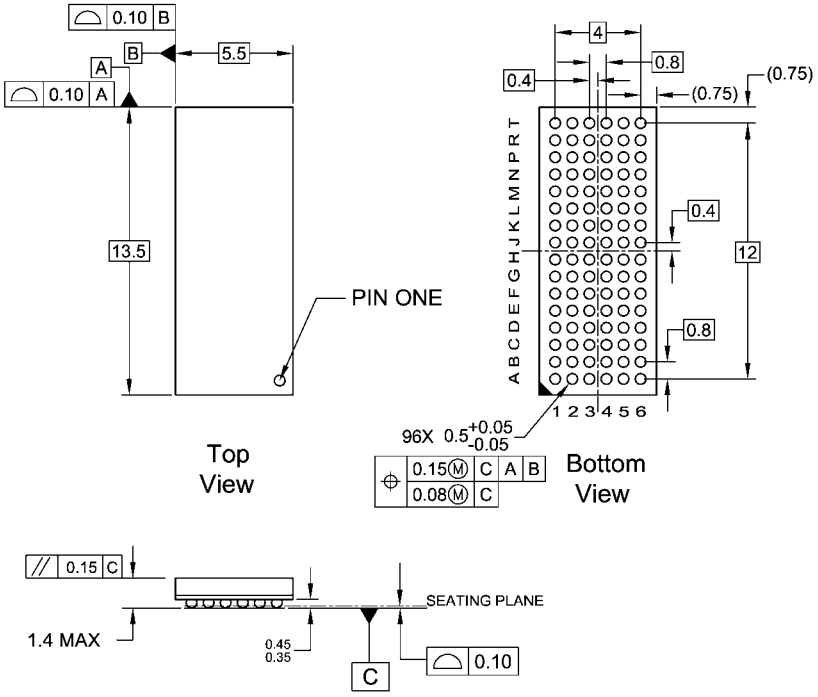
Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	160		160		MHz
t_{PHL}	Propagation Delay	2.2	4.9	2.2	5.1	ns
t_{PLH}	CP to O_n	2.0	5.3	2.0	6.2	
t_{PZL}	Output Enable Time	1.8	4.9	1.8	6.0	ns
t_{PZH}		1.8	5.6	1.8	6.9	
t_{PLZ}	Output Disable Time	2.0	5.0	2.0	5.1	ns
t_{PHZ}		2.4	5.4	2.4	5.7	
t_S	Setup Time	1.8		2.0		ns
t_H	Hold Time	0.8		0.1		ns
t_W	Pulse Width	3.0		3.0		ns

Capacitance (Note 9)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN, V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.0V, V_O = 0V or V_{CC}	8	pF

Note 9: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A
Preliminary

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