FAIRCHILD SEMICONDUCTOR™

January 2001
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74LVT32244 • 74LVTH32244
Low Voltage 32-Bit Buffer/Line Driver with 3-STATE Outputs (Preliminary)

General Description

The LVT32244 and LVTH32244 contain thirty-two non-inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit, 16-bit, or 32-bit operation.

The LVTH32244 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT32244 and LVTH32244 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation

Features

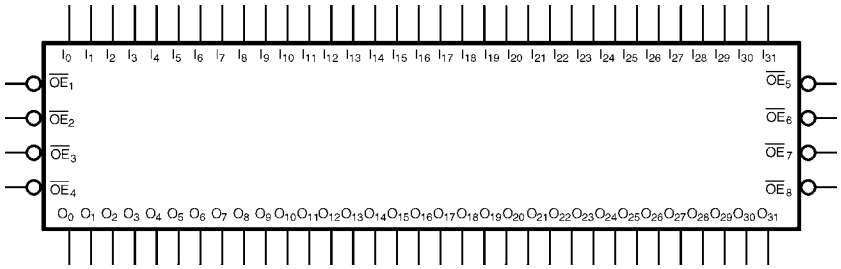
- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH32244), also available without bushold feature (74LVT32244).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink −32 mA/+64 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA) (Preliminary)

Ordering Code:

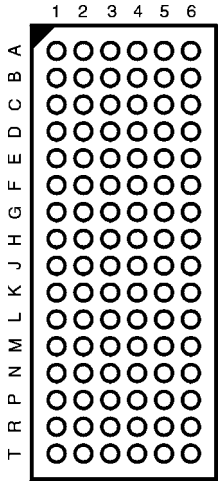
Order Number	Package Number	Package Description
74LVT32244GX (Note 1)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]
74LVTH32244GX (Note 1)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide [Tape and Reel]

Note 1: BGA package available in Tape and Reel only.

Logic Symbol



Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0–I_{31}	Inputs
O_0–O_{31}	Outputs

Pin Assignments for FBGA

	1	2	3	4	5	6
A	O_1	O_0	$\overline{OE}_1$	$\overline{OE}_2$	I_0	I_1
B	O_3	O_2	GND	GND	I_2	I_3
C	O_5	O_4	V_{CC1}	V_{CC1}	I_4	I_5
D	O_7	O_6	GND	GND	I_6	I_7
E	O_9	O_8	GND	GND	I_8	I_9
F	O_{11}	O_{10}	V_{CC1}	V_{CC1}	I_{10}	I_{11}
G	O_{13}	O_{12}	GND	GND	I_{12}	I_{13}
H	O_{14}	O_{15}	$\overline{OE}_4$	$\overline{OE}_3$	I_{15}	I_{14}
J	O_{17}	O_{16}	$\overline{OE}_5$	$\overline{OE}_6$	I_{16}	I_{17}
K	O_{19}	O_{18}	GND	GND	I_{18}	I_{19}
L	O_{21}	O_{20}	V_{CC2}	V_{CC2}	I_{20}	I_{21}
M	O_{23}	O_{22}	GND	GND	I_{22}	I_{23}
N	O_{25}	O_{24}	GND	GND	I_{24}	I_{25}
P	O_{27}	O_{26}	V_{CC2}	V_{CC2}	I_{26}	I_{27}
R	O_{29}	O_{28}	GND	GND	I_{28}	I_{29}
T	O_{30}	O_{31}	$\overline{OE}_8$	$\overline{OE}_7$	I_{31}	I_{30}

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0-I_3	O_0-O_3
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4-I_7	O_4-O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8-I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}-I_{15}	O_{12}-O_{15}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_5$	I_{16}-I_{19}	O_{16}-O_{19}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_6$	I_{20}-I_{23}	O_{20}-O_{23}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_7$	I_{24}-I_{27}	O_{24}-O_{27}
L	L	L
L	H	H
H	X	Z

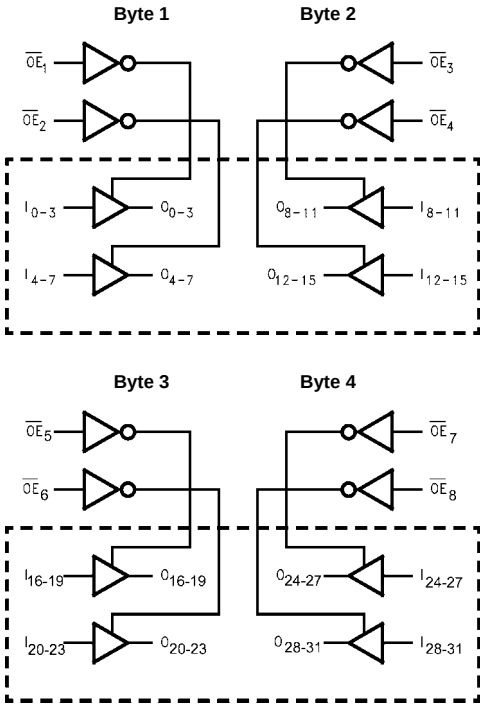
Inputs		Outputs
$\overline{OE}_8$	I_{28}-I_{31}	O_{28}-O_{31}
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74LVT32244 and 74LVTH32244 contain thirty-two non-inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 32-bit operation. The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagrams



V_{CC1} is associated with Bytes 1 and 2.

V_{CC2} is associated with Bytes 3 and 4.

Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +4.6		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to +7.0	Output in High or Low State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	High-Level Output Current		−32	mA
I_{OL}	Low-Level Output Current		64	mA
T_A	Free Air Operating Temperature	−40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 2: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 3: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40°C to +85°C Min	T_A = −40°C to +85°C Max	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		2.7		−1.2	V	I_I = −18 mA
V_{IH}	Input HIGH Voltage		2.7–3.6	2.0		V	$V_O \le 0.1V$ or
V_{IL}	Input LOW Voltage		2.7–3.6		0.8	V	$V_O \ge V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage		2.7–3.6	V_{CC} − 0.2		V	I_{OH} = −100 µA
			2.7	2.4			I_{OH} = −8 mA
			3.0	2.0			I_{OH} = −32 mA
V_{OL}	Output LOW Voltage		2.7		0.2	V	I_{OL} = 100 µA
			2.7		0.5		I_{OL} = 24 mA
			3.0		0.4		I_{OL} = 16 mA
			3.0		0.5		I_{OL} = 32 mA
			3.0		0.55		I_{OL} = 64 mA
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive		3.0	75		µA	V_I = 0.8V
				−75			V_I = 2.0V
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State		3.0	500		µA	(Note 5)
				−500			(Note 6)
I_I	Input Current		3.6		10	µA	V_I = 5.5V
		Control Pins	3.6		±1		V_I = 0V or V_{CC}
		Data Pins	3.6		−5		V_I = 0V
					1		V_I = V_{CC}
I_{OFF}	Power Off Leakage Current		0		±100	µA	$0V \le V_I$ or $V_O \le 5.5V$
$I_{PU/PD}$	Power Up/Down 3-STATE Current		0 – 1.5V		±100	µA	V_O = 0.5V to 3.0V, V_I = GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current		3.6		−5	µA	V_O = 0.5V
I_{OZH}	3-STATE Output Leakage Current		3.6		5	µA	V_O = 3.0V
I_{OZH+}	3-STATE Output Leakage Current		3.6		10	µA	$V_{CC} < V_O \le 5.5V$

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Conditions
				Min	Max		
I_{CCH}	Power Supply Current	V_{CC1} or V_{CC2}	3.6		0.19	mA	Outputs High
I_{CCL}	Power Supply Current	V_{CC1} or V_{CC2}	3.6		5.0	mA	Outputs Low
I_{CCZ}	Power Supply Current	V_{CC1} or V_{CC2}	3.6		0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current	V_{CC1} or V_{CC2}	3.6		0.19	mA	$V_{CC} \le V_O \le 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)	V_{CC1} or V_{CC2}	3.6		0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 4: Applies to bushold versions only (LVTH32244).

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF, $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		–0.8		V	(Note 9)

Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n–1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

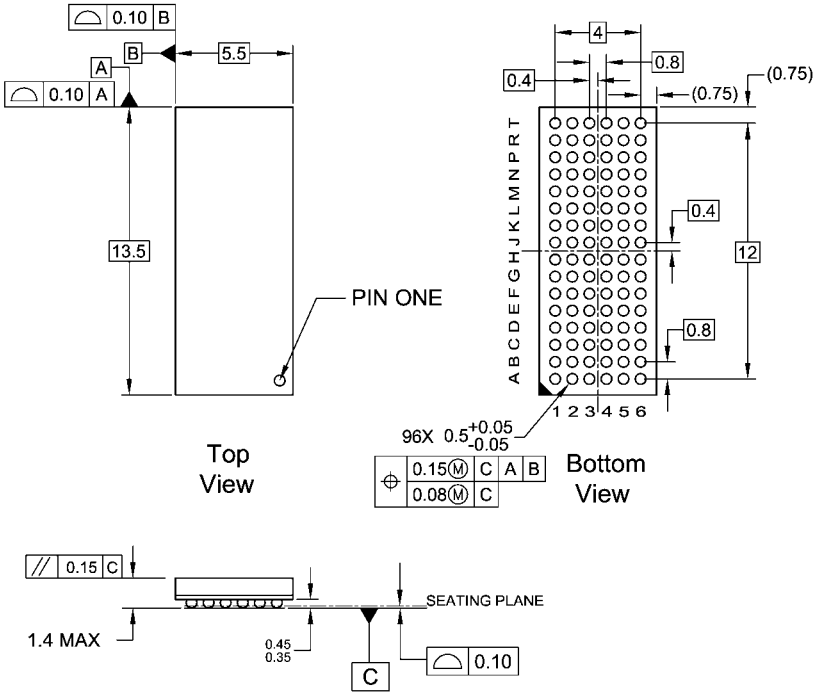
Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $R_L = 500\Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Output	1.2	3.5	1.2	3.9	ns
t_{PHL}		1.2	3.5	1.2	3.9	
t_{PZH}	Output Enable Time	1.2	4.0	1.2	5.0	ns
t_{PZL}		1.2	5.0	1.2	6.5	
t_{PHZ}	Output Disable Time	2.0	4.7	2.0	5.2	ns
t_{PLZ}		1.5	4.2	1.5	4.4	

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 0V$, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A
Preliminary

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