

# 74LVT244A; 74LVTH244A

3.3 V octal buffer/line driver; 3-state

Rev. 04 — 3 September 2008

Product data sheet

## 1. General description

The 74LVT244A; 74LVTH244A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ( $1\overline{OE}$ ,  $2\overline{OE}$ ), each controlling four of the 3-state outputs.

## 2. Features

- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
  - ◆ JESD78 Class II exceeds 500 mA
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V

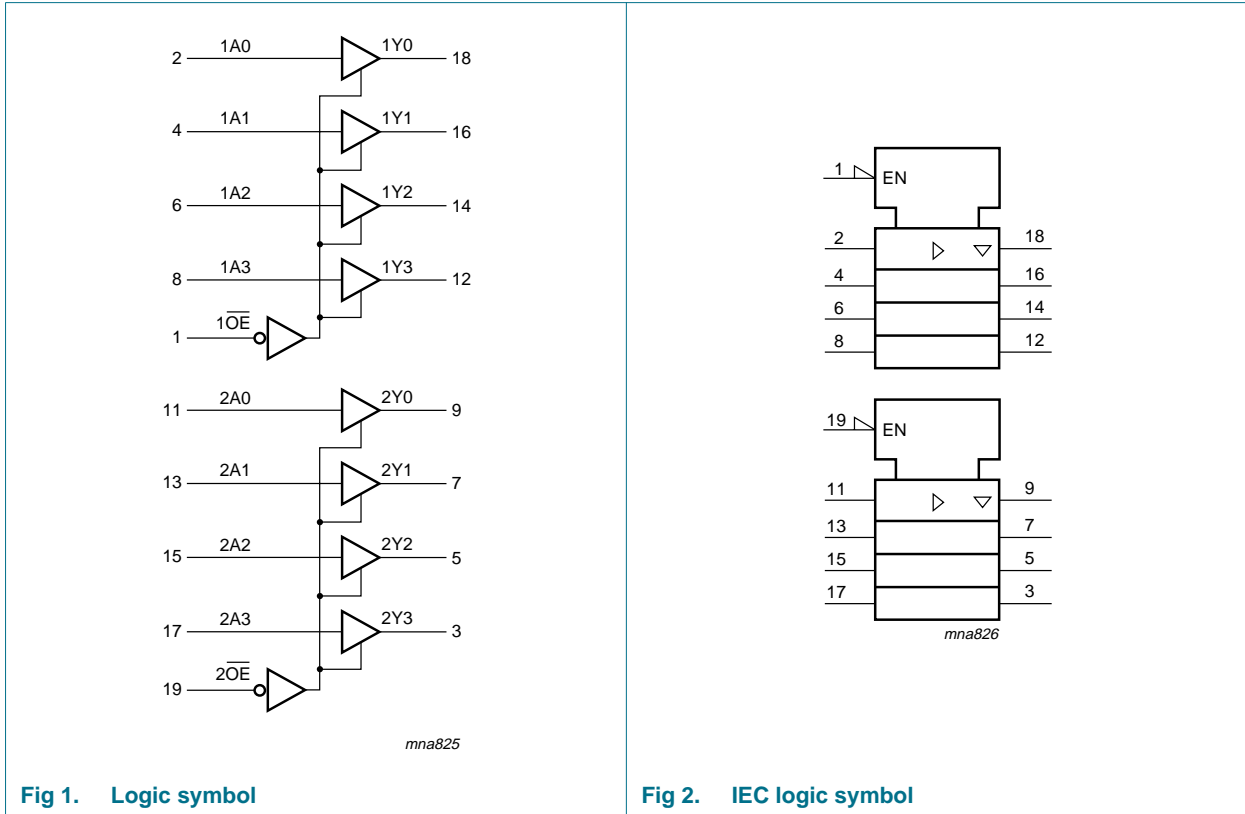
## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT244AD 74LVTH244AD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT244ADB 74LVTH244ADB	-40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT244APW 74LVTH244APW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVT244ABQ 74LVTH244ABQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

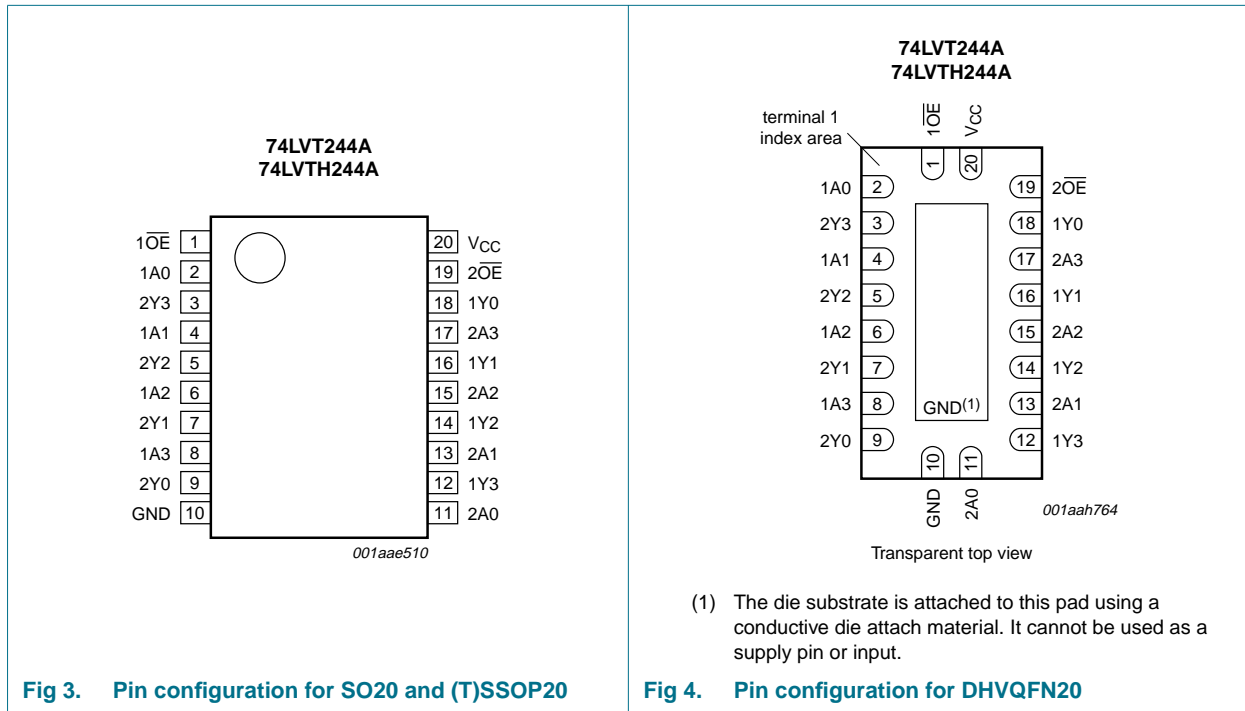


## 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
1 $\overline{OE}$ , 2 $\overline{OE}$	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3,	18, 16, 14, 12	data output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

### 6.1 Function table

Table 3. Function table [\[1\]](#)

Control	Input	Output
nOE	nAn	nYn
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		<a href="#">[1]</a> -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	<a href="#">[1]</a> -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-	-50	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		<a href="#">[2]</a> -	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C	<a href="#">[3]</a>	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
 For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
V <sub>I</sub>	input voltage		0	-	5.5	V
I <sub>OH</sub>	HIGH-level output current		-	-	-32	mA

Table 5. Operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz	-	-	64	mA
T <sub>amb</sub>	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C [1]</b>						
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub> - 0.1	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -8 mA	2.4	2.5	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -32 mA	2.0	2.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 100 μA	-	0.1	0.2	V
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 24 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA	-	0.4	0.55	V
I <sub>I</sub>	input leakage current	all input pins				
		V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	0.1	10	μA
		control pins				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	±0.1	±1	μA
		data pins [2]				
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>	-	0.1	1	μA
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V	-5	-1	-	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	1	±100	μA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V [3]	75	150	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V	-	-150	-75	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	nAn input; V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = 3.6 V	500	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	nAn input; V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = 3.6 V	-	-	-500	μA
I <sub>LO</sub>	output leakage current	nYn output in HIGH-state when V <sub>O</sub> > V <sub>CC</sub> ; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	60	125	μA
I <sub>O(pu/pd)</sub>	power-up/power-down output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; nOE = don't care [4]	-	±1	±100	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		V <sub>O</sub> = 3.0 V	-	1	5	μA	
		V <sub>O</sub> = 0.5 V	-5	-1	-	μA	
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> ; I <sub>O</sub> = 0 A					
		output HIGH	-	0.13	0.19	mA	
		output LOW	-	3	12	mA	
		outputs disabled	[5]	-	0.13	0.19	mA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 3.0 V to 3.6 V; one input at V <sub>CC</sub> - 0.6 V and other inputs at V <sub>CC</sub> or GND	[6]	-	0.1	0.2	mA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	4	-	pF	
C <sub>O</sub>	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or 3.0 V	-	8	-	pF	

[1] All typical values are at T<sub>amb</sub> = 25 °C.

[2] Unused pins at V<sub>CC</sub> or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 ms. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T<sub>amb</sub> = 25 °C only.

[5] I<sub>CC</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

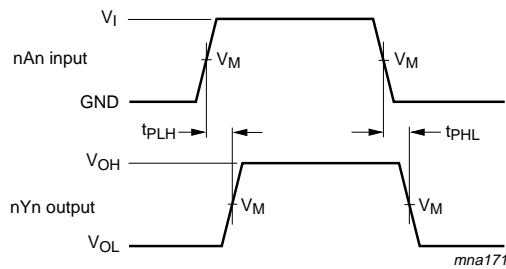
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C [1]</b>						
t <sub>PLH</sub>	LOW to HIGH propagation delay	nAn to nYn; see <a href="#">Figure 5</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1	2.5	4.1	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nAn to nYn; see <a href="#">Figure 5</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.1	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1	2.6	4.1	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1	3.2	5.2	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.7	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.1	3.1	5.2	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	6.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.9	3.3	5.6	ns

**Table 7. Dynamic characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	see <a href="#">Figure 6</a>				
		V <sub>CC</sub> = 2.7 V	-	-	5.6	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	3.3	5.1	ns

[1] All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

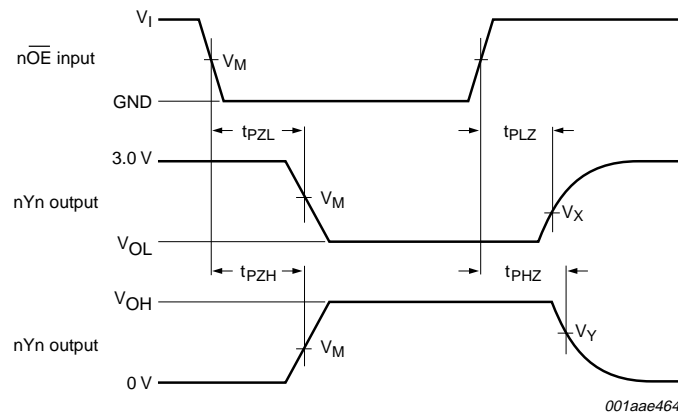
## 11. Waveforms



Measurement points are given in [Table 8](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 5. Propagation delay input (nAn) to output (nYn) propagation delays**



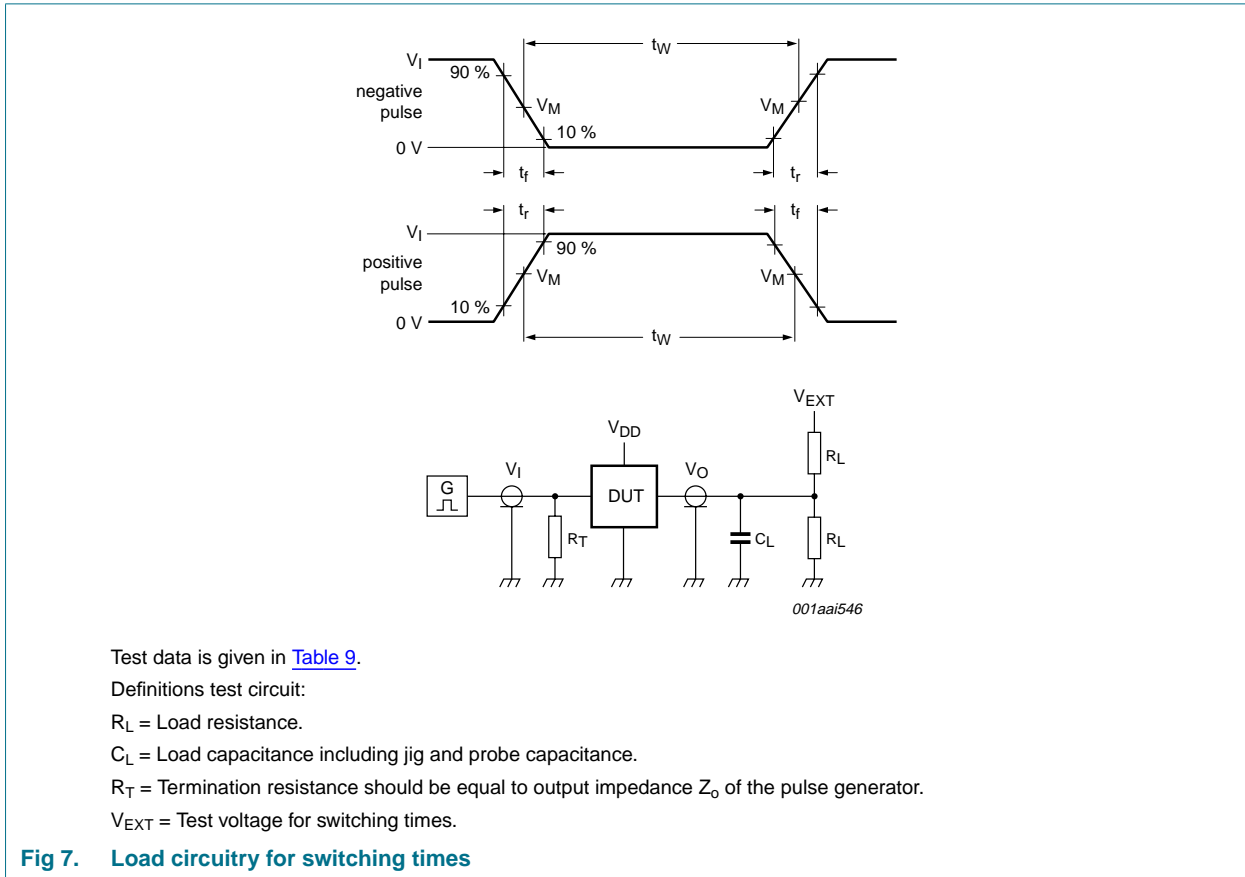
Measurement points are given in [Table 8](#).

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

**Fig 6. 3-state output enable and disable times**

**Table 8. Measurement points**

Input	Output		
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open



## 12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

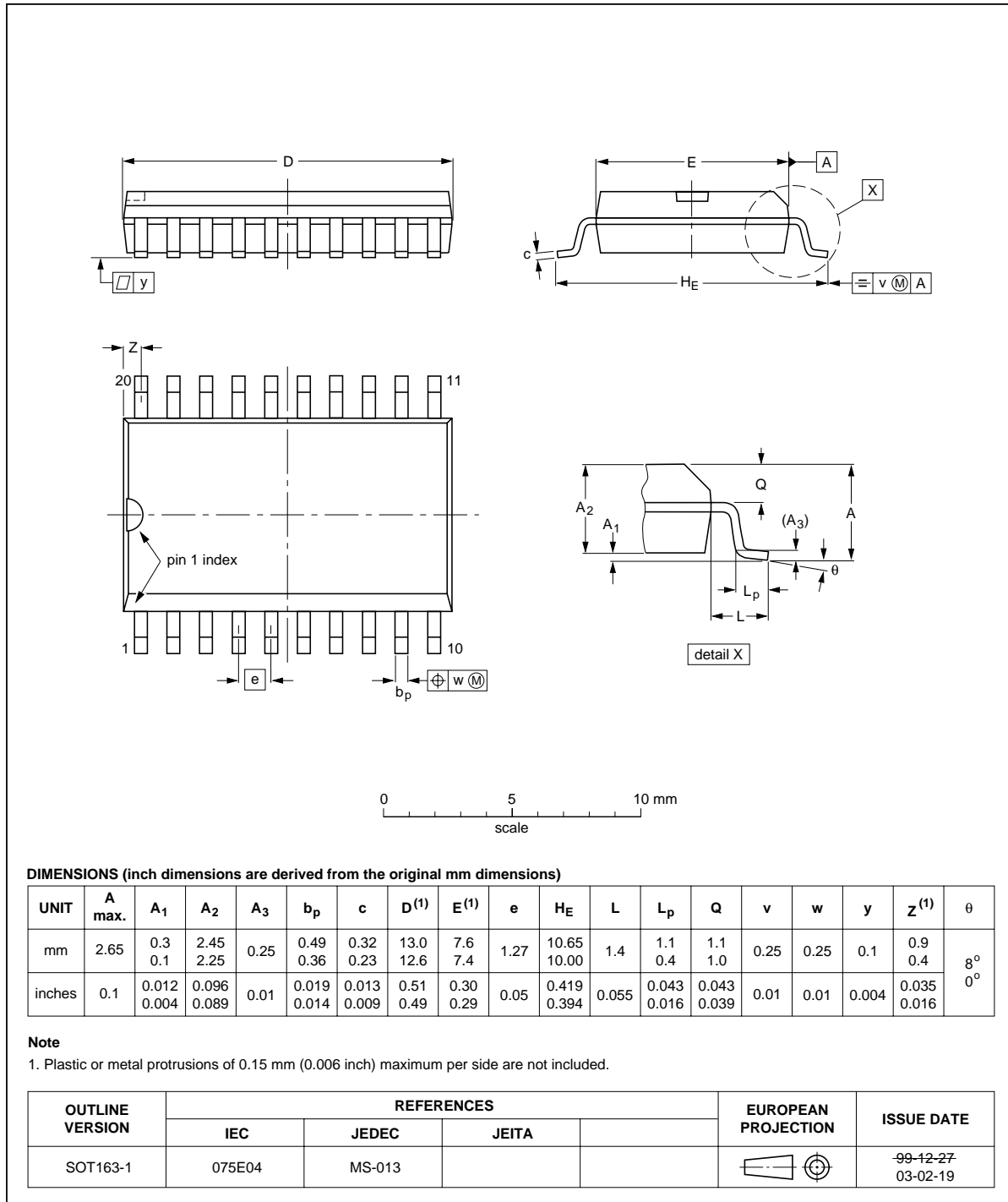


Fig 8. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

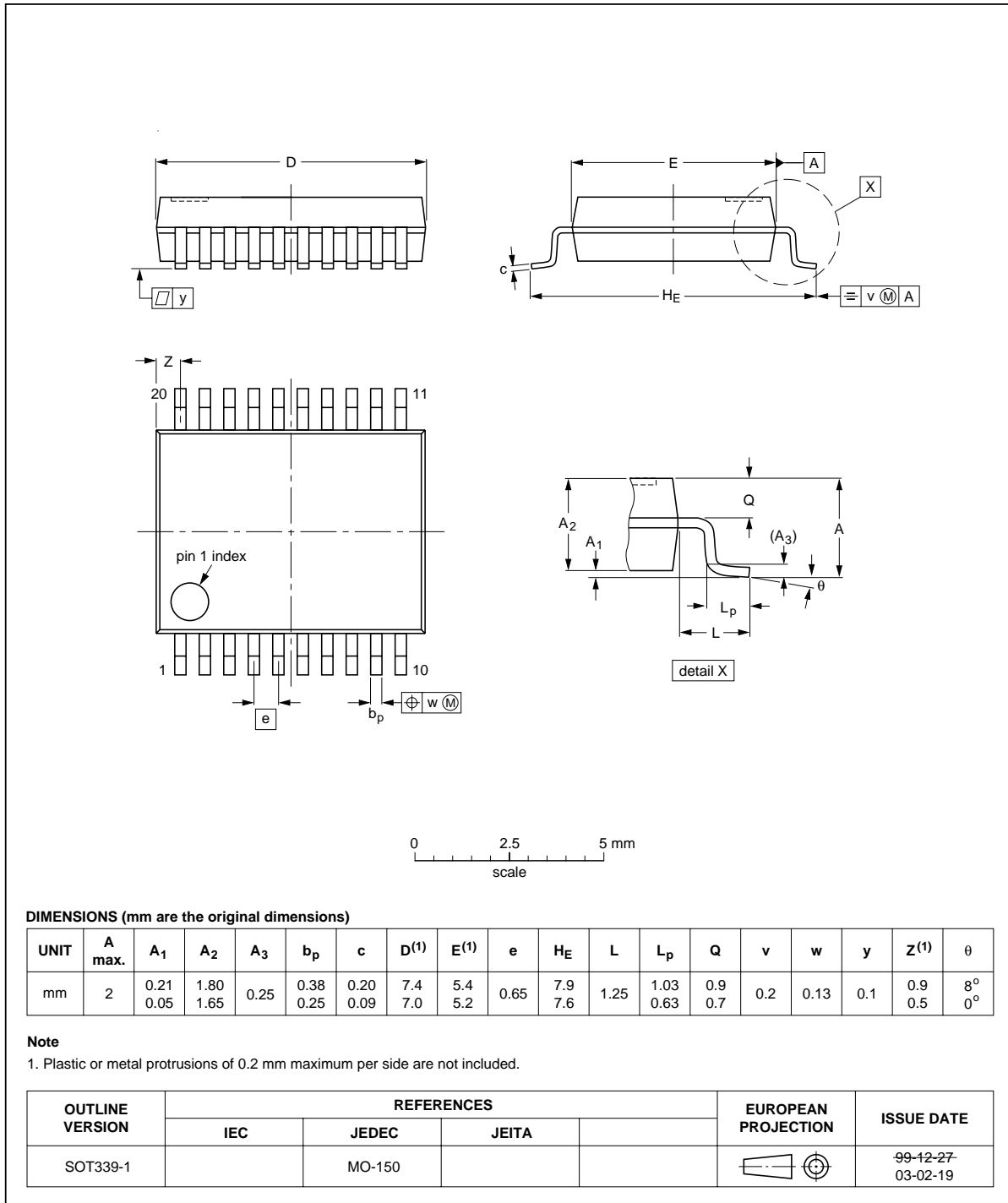


Fig 9. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

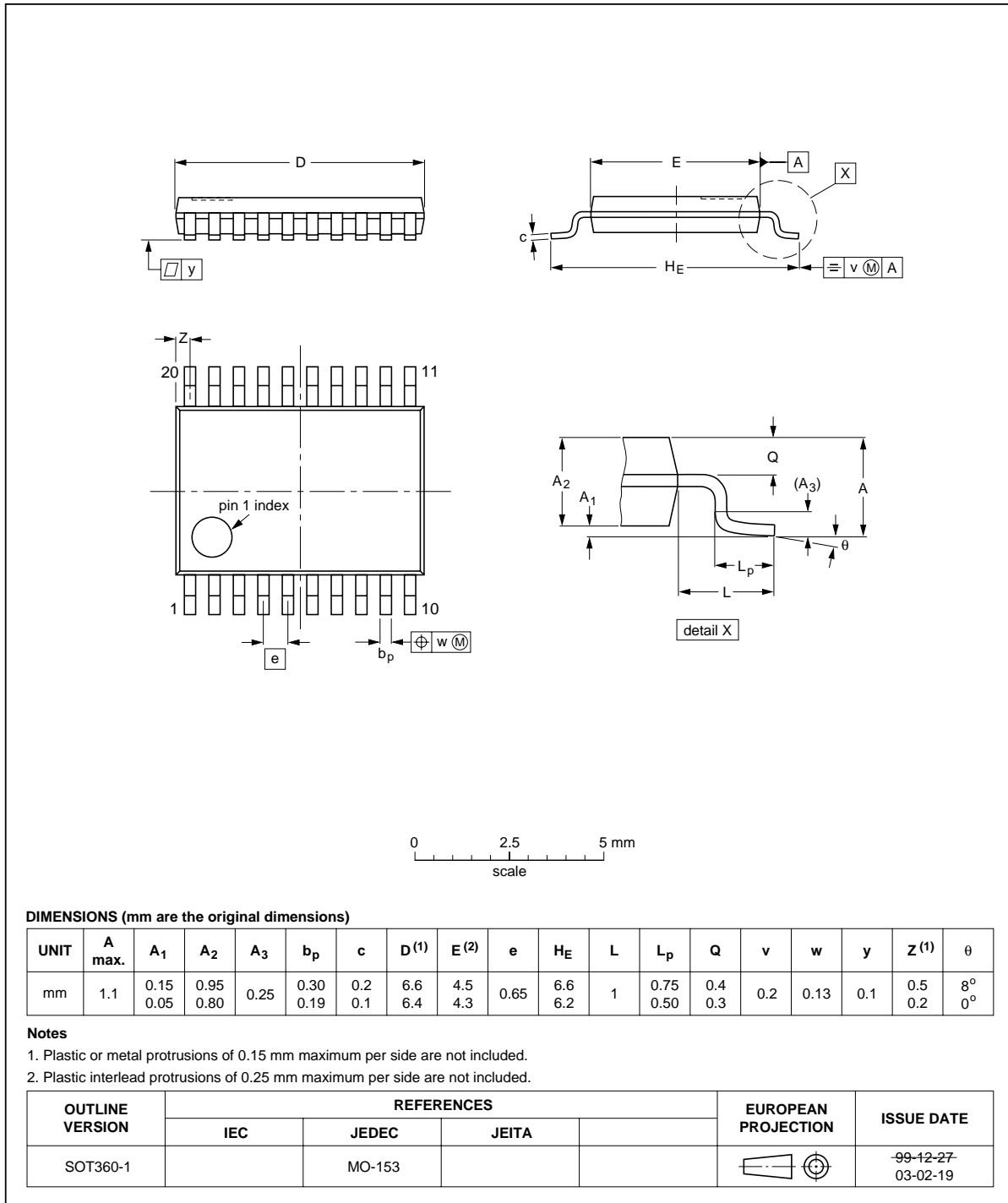
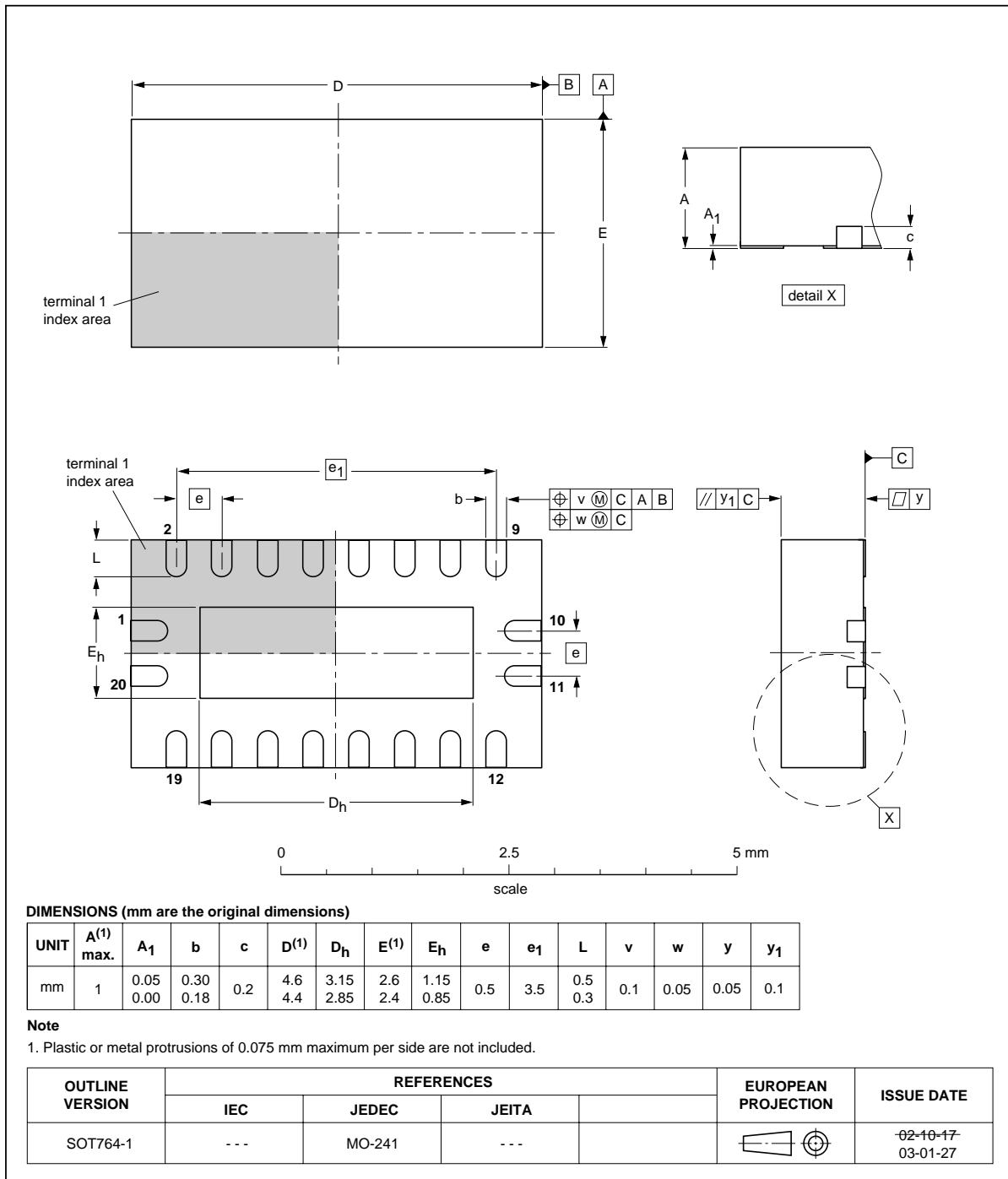


Fig 10. Package outline SOT360-1 (TSSOP20)

**DHVQFN20:** plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1



**Fig 11. Package outline SOT764-1 (DHVQFN20)**

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A_4	20080903	Product data sheet	-	74LVT_LVTH244A_3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 3 "Ordering information"</a> and <a href="#">Section 12 "Package outline"</a> DHVQFN20 package added.</li> </ul>			
74LVT_LVTH244A_3	20060315	Product specification	-	74LVT244A_2
74LVT244A_2	19980219	Product specification	-	74LVT244A_1

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 15.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

**17. Contents**

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>
<b>2</b>	<b>Features</b> . . . . .	<b>1</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>1</b>
<b>4</b>	<b>Functional diagram</b> . . . . .	<b>2</b>
<b>5</b>	<b>Pinning information</b> . . . . .	<b>3</b>
5.1	Pinning . . . . .	3
5.2	Pin description . . . . .	3
<b>6</b>	<b>Functional description</b> . . . . .	<b>4</b>
6.1	Function table . . . . .	4
<b>7</b>	<b>Limiting values</b> . . . . .	<b>4</b>
<b>8</b>	<b>Recommended operating conditions</b> . . . . .	<b>4</b>
<b>9</b>	<b>Static characteristics</b> . . . . .	<b>5</b>
<b>10</b>	<b>Dynamic characteristics</b> . . . . .	<b>6</b>
<b>11</b>	<b>Waveforms</b> . . . . .	<b>7</b>
<b>12</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>13</b>	<b>Abbreviations</b> . . . . .	<b>13</b>
<b>14</b>	<b>Revision history</b> . . . . .	<b>13</b>
<b>15</b>	<b>Legal information</b> . . . . .	<b>14</b>
15.1	Data sheet status . . . . .	14
15.2	Definitions . . . . .	14
15.3	Disclaimers . . . . .	14
15.4	Trademarks . . . . .	14
<b>16</b>	<b>Contact information</b> . . . . .	<b>14</b>
<b>17</b>	<b>Contents</b> . . . . .	<b>15</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 3 September 2008

Document identifier: 74LVT\_LVTH244A\_4