



May 2000
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74LVTH16835 Low Voltage 18-Bit Universal Bus Driver

74LVTH16835 Low Voltage 18-Bit Universal Bus Driver with 3-STATE Outputs (Preliminary)

General Description

The LVTH16835 consists of 18-bit universal bus drivers which combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. This device operates in the transparent mode when the latch-enable (LE) input is HIGH. The A data is latched if the clock (CLK) input is held at a HIGH or LOW logic level. If LE is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of the CLK. When \overline{OE} is HIGH, the outputs are in the high-impedance state.

The LVTH16835 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

The bus driver is designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVTH16835 is fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Latch-up performance exceeds 500 mA

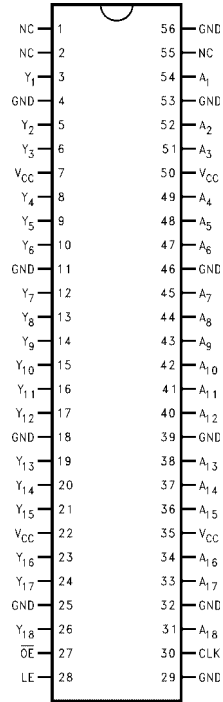
Ordering Code:

| Order Number | Package Number | Package Description |
|----------------|----------------|---|
| 74LVTH16835MEA | MS56A | 56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide |
| 74LVTH16835MTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74LVTH16835

Connection Diagram



Pin Descriptions

| Pin Names | Description |
|---------------------------------|----------------------|
| A ₁ –A ₁₈ | Data Register Inputs |
| Y ₁ –Y ₁₈ | 3-STATE Outputs |
| CLK | Clock Pulse Input |
| \overline{OE} | Output Enable Input |
| LE | Latch Enable Input |

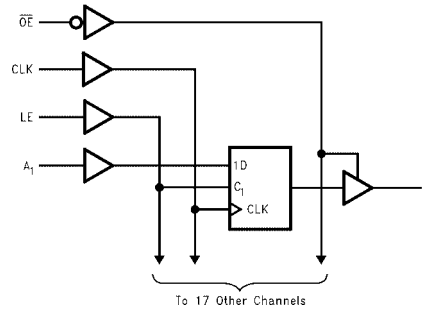
Truth Table

| \overline{OE} | Inputs | | | A | Output Y |
|-----------------|--------|-----|---|---|-------------------------|
| | LE | CLK | | | |
| H | X | X | X | X | Z |
| L | H | X | L | L | L |
| L | H | X | H | H | H |
| L | L | ↑ | L | L | L |
| L | L | ↑ | H | H | H |
| L | L | H | X | X | Y ₀ (Note 1) |
| L | L | L | X | X | Y ₀ (Note 2) |

H = HIGH Voltage Level
 X = Immaterial
 ↑ = HIGH-to-LOW Clock Transition
 L = LOW Voltage Level
 Z = High Impedance

Note 1: Output level before the indicated steady-state input conditions were established, provided that CLK was HIGH before LE went LOW.
Note 2: Output level before the indicated steady-state input conditions were established.

Logic Diagram



| Absolute Maximum Ratings ^(Note 3) | | | | |
|--|---|--------------|--------------------------------------|-------------|
| Symbol | Parameter | Value | Conditions | Units |
| V_{CC} | Supply Voltage | -0.5 to +4.6 | | V |
| V_I | DC Input Voltage | -0.5 to +7.0 | | V |
| V_O | DC Output Voltage | -0.5 to +7.0 | Output in 3-STATE | V |
| | | -0.5 to +7.0 | Output in HIGH or LOW State (Note 4) | V |
| I_{IK} | DC Input Diode Current | -50 | $V_I < GND$ | mA |
| I_{OK} | DC Output Diode Current | -50 | $V_O < GND$ | mA |
| I_O | DC Output Current | 64 | $V_O > V_{CC}$ Output at HIGH State | mA |
| | | 128 | $V_O > V_{CC}$ Output at LOW State | |
| I_{CC} | DC Supply Current per Supply Pin | ± 64 | | mA |
| I_{GND} | DC Ground Current per Ground Pin | ± 128 | | mA |
| T_{STG} | Storage Temperature | -65 to +150 | | $^{\circ}C$ |
| Recommended Operating Conditions | | | | |
| Symbol | Parameter | Min | Max | Units |
| V_{CC} | Supply Voltage | 2.7 | 3.6 | V |
| V_I | Input Voltage | 0 | 5.5 | V |
| I_{OH} | HIGH-Level Output Current | | -32 | mA |
| I_{OL} | LOW-Level Output Current | | 64 | mA |
| T_A | Free-Air Operating Temperature | -40 | 85 | $^{\circ}C$ |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$ | 0 | 10 | ns/V |
| <p>Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p>Note 4: I_O Absolute Maximum Rating must be observed.</p> | | | | |

DC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) | T _A = -40°C to +85°C | | Units | Conditions | |
|----------------------|--|------------------------|---------------------------------|------|-------|---|--|
| | | | Min | Max | | | |
| V _{IK} | Input Clamp Diode Voltage | 2.7 | | -1.2 | V | I _I = -18 mA | |
| V _{IH} | Input HIGH Voltage | 2.7-3.6 | 2.0 | | V | V _O ≤ 0.1V or | |
| V _{IL} | Input LOW Voltage | 2.7-3.6 | | 0.8 | | V _O ≥ V _{CC} - 0.1V | |
| V _{OH} | Output HIGH Voltage | 2.7-3.6 | V _{CC} - 0.2 | | V | I _{OH} = -100 μA | |
| | | 2.7 | 2.4 | | V | I _{OH} = -8 mA | |
| | | 3.0 | 2.0 | | V | I _{OH} = -32 mA | |
| V _{OL} | Output LOW Voltage | 2.7 | | 0.2 | V | I _{OL} = 100 μA | |
| | | 2.7 | | 0.5 | V | I _{OL} = 24 mA | |
| | | 3.0 | | 0.4 | V | I _{OL} = 16 mA | |
| | | 3.0 | | 0.5 | V | I _{OL} = 32 mA | |
| | | 3.0 | | 0.55 | V | I _{OL} = 64 mA | |
| I _{I(HOLD)} | Bushold Input Minimum Drive | 3.0 | 75 | | μA | V _I = 0.8V | |
| | | | -75 | | μA | V _I = 2.0V | |
| I _{I(OD)} | Bushold Input Over-Drive Current to Change State | 3.0 | 500 | | μA | (Note 5) | |
| | | | -500 | | μA | (Note 6) | |
| I _I | Input Current | 3.6 | | 10 | μA | V _I = 5.5V | |
| | | Control Pins | 3.6 | | ±1 | μA | V _I = 0V or V _{CC} |
| | | Data Pins | 3.6 | | -5 | μA | V _I = 0V |
| | | | | 1 | μA | V _I = V _{CC} | |
| I _{OFF} | Power Off Leakage Current | 0 | | ±100 | μA | 0V ≤ V _I or V _O ≤ 5.5V | |
| I _{PU/PD} | Power up/down 3-STATE Output Current | 0-1.5V | | ±100 | μA | V _O = 0.5V to 3.0V V _I = GND or V _{CC} | |
| I _{OZL} | 3-STATE Output Leakage Current | 3.6 | | -5 | μA | V _O = 0.5V | |
| I _{OZH} | 3-STATE Output Leakage Current | 3.6 | | 5 | μA | V _O = 3.0V | |
| I _{OZH+} | 3-STATE Output Leakage Current | 3.6 | | 10 | μA | V _{CC} < V _O ≤ 5.5V | |
| I _{CCH} | Power Supply Current | 3.6 | | 0.19 | mA | Outputs HIGH | |
| I _{CCL} | Power Supply Current | 3.6 | | 5 | mA | Outputs LOW | |
| I _{CCZ} | Power Supply Current | 3.6 | | 0.19 | mA | Outputs Disabled | |
| I _{CCZ+} | Power Supply Current | 3.6 | | 0.19 | mA | V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled | |
| ΔI _{CC} | Increase in Power Supply Current (Note 7) | 3.6 | | 0.2 | mA | One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND | |

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

| Symbol | Parameter | V _{CC} (V) | T _A = 25°C | | | Units | Conditions C _L = 50 pF, R _L = 500Ω |
|------------------|--|------------------------|-----------------------|------|-----|-------|---|
| | | | Min | Typ | Max | | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 3.3 | | 0.8 | | V | (Note 9) |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 3.3 | | -0.8 | | V | (Note 9) |

Note 8: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

| AC Electrical Characteristics | | | | | | |
|-------------------------------|-----------------------|---|-----|------------------------|-----|-------|
| Symbol | Parameter | T _A = -40°C to +85°C, C _L = 50 pF, R _L = 500 Ω | | | | Units |
| | | V _{CC} = 3.3 ± 0.3V | | V _{CC} = 2.7V | | |
| | | Min | Max | Min | Max | |
| f _{MAX} | | 150 | | 150 | | MHz |
| t _{PLH} | Propagation Delay | 1.3 | 3.7 | 1.3 | 4.0 | ns |
| t _{PHL} | A to Y | 1.3 | 3.7 | 1.3 | 4.0 | |
| t _{PLH} | Propagation Delay | 1.5 | 5.1 | 1.5 | 5.7 | ns |
| t _{PHL} | LE to Y | 1.5 | 5.1 | 1.5 | 5.7 | |
| t _{PLH} | Propagation Delay | 1.5 | 5.1 | 1.5 | 5.7 | ns |
| t _{PHL} | CLK to Y | 1.5 | 5.1 | 1.5 | 5.7 | |
| t _{PZH} | Output Enable Time | 1.3 | 4.6 | 1.3 | 5.5 | ns |
| t _{PZL} | | 1.3 | 4.6 | 1.3 | 5.5 | |
| t _{PHZ} | Output Disable Time | 1.7 | 5.8 | 1.7 | 6.3 | ns |
| t _{PLZ} | | 1.7 | 5.8 | 1.7 | 6.3 | |
| t _S | Setup Time | A before CLK | | 2.1 | 2.4 | ns |
| | | A before LE, CLK HIGH | | 2.3 | 1.5 | |
| | | A before LE, CLK LOW | | 1.5 | 0.5 | |
| t _H | Hold Time | A after CLK | | 1.0 | 0.0 | ns |
| | | A after LE | | 0.8 | 0.8 | |
| t _W | Pulse Duration | LE HIGH | | 3.3 | 3.3 | ns |
| | | CLK HIGH or LOW | | 3.3 | 3.3 | |
| t _{OSLH} | Output to Output Skew | | 1.0 | | 1.0 | ns |
| t _{OSHL} | (Note 10) | | 1.0 | | 1.0 | |

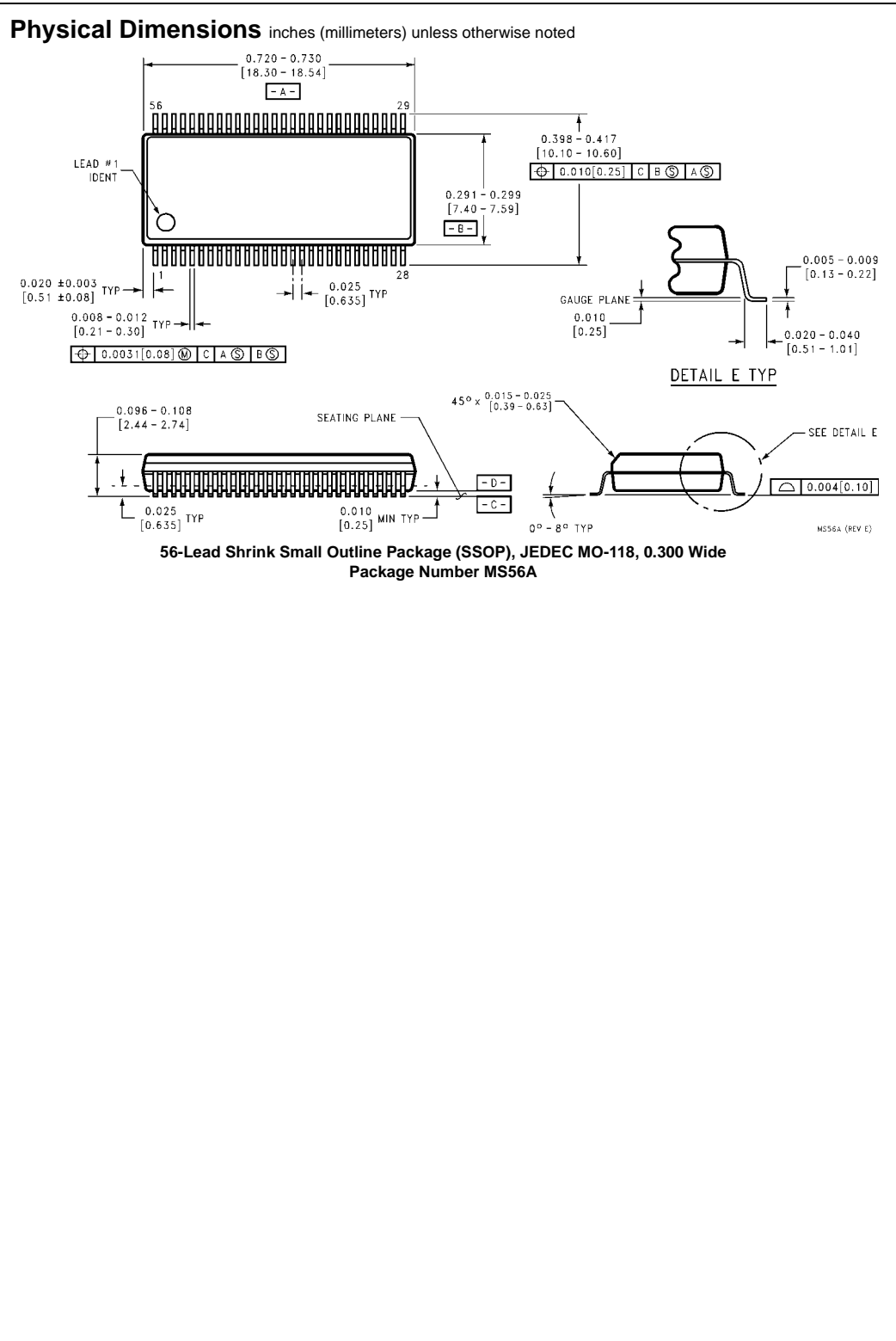
Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 11)

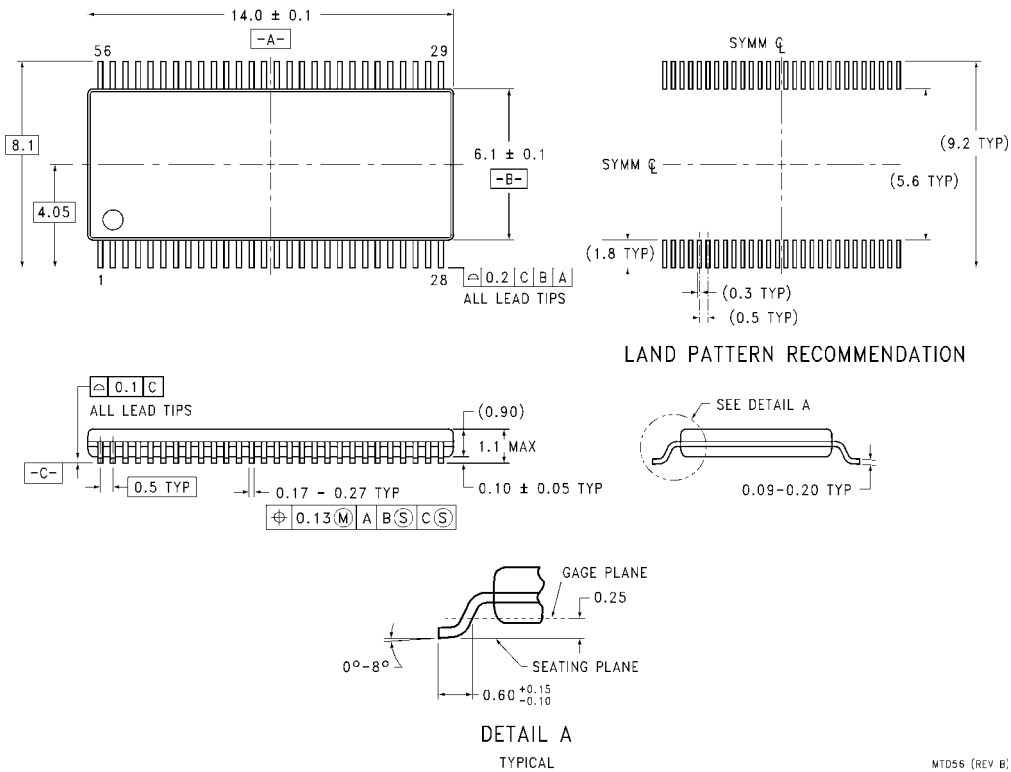
| Symbol | Parameter | Conditions | Typical | Units |
|------------------|--------------------|--|---------|-------|
| C _{IN} | Input Capacitance | V _{CC} = 0V, V _I = 0V or V _{CC} | 4 | pF |
| C _{OUT} | Output Capacitance | V _{CC} = 3.0V, V _O = 0V or V _{CC} | 8 | pF |

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

74LVTH16835



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56**

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