74LVT16245B; 74LVTH16245B

3.3 V 16-bit transceiver; 3-state

Rev. 04 — 23 March 2006 Product data sheet

1. General description

The 74LVT16245B; 74LVTH16245B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input ($\overline{OE}$) for easy cascading and a direction input (DIR) for direction control.

2. Features

- 16-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - Machine model: exceeds 200 V

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	-	1.9	-	ns
t_{PHL}	HIGH-to-LOW propagation delay nAx to nBx or nBx to nAx	C_L = 50 pF; V_{CC} = 3.3 V	-	1.7	-	ns

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Table 1. Quick reference data *…continued*

GND = 0 V; T_{amb} = 25 °C.

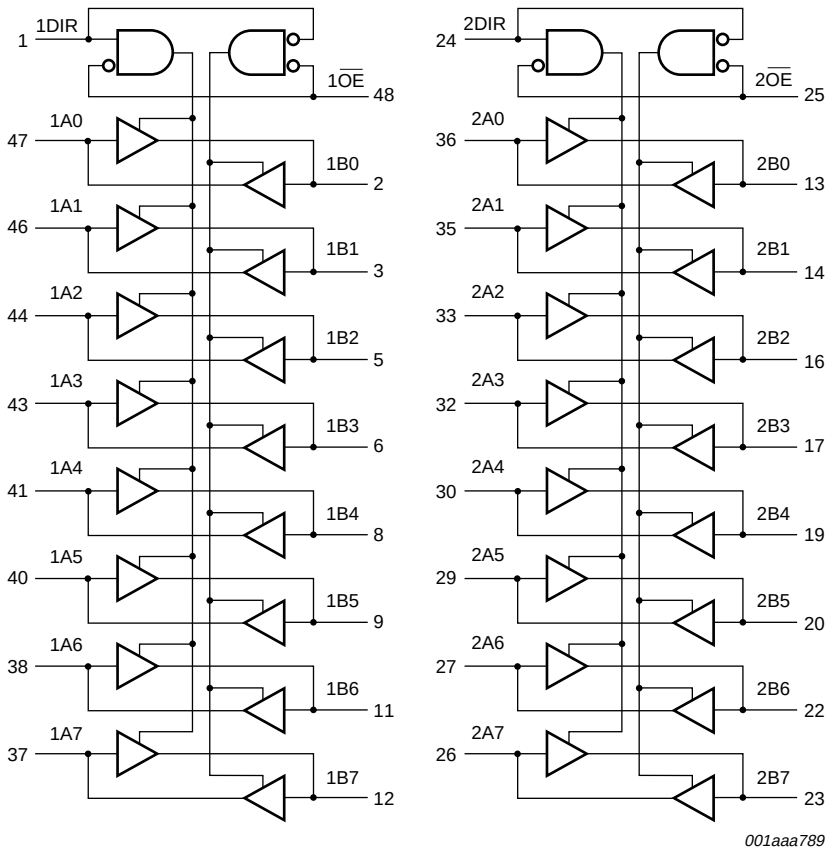
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance pins DIR and $\overline{OE}$	V_I = 0 V or 3.0 V	-	3	-	pF
C_{io}	input/output capacitance pins nAx and nBx	V_O = 0 V or 3.0 V	-	9	-	pF
I_{CC}	quiescent supply current	outputs disabled; V_{CC} = 3.6 V; I_O = 0 A V_I = GND or V_{CC}	-	0.07	-	mA

4. Ordering information

Table 2. Ordering information

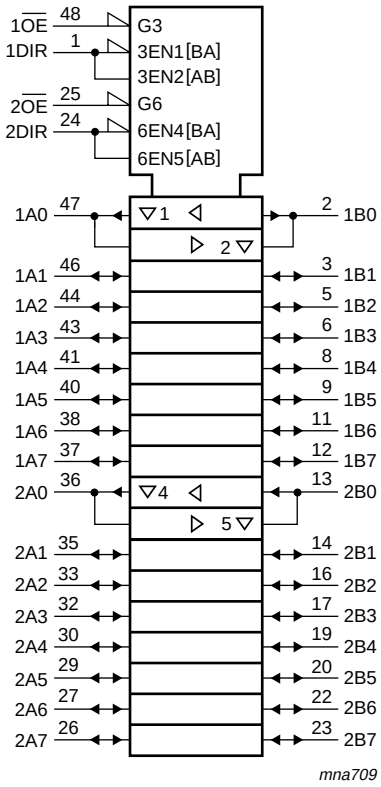
Type number	Package			
	Temperature range	Name	Description	Version
74LVT16245BDGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVT16245BDL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVT16245BEV	–40 °C to +85 °C	VFBGA56	plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 × 7 × 0.65 mm	SOT702-1
74LVTH16245BDGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVTH16245BDL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

5. Functional diagram



Pin numbers are shown for SSOP and TSSOP packages only.

Fig 1. Logic symbol



Pin numbers are shown for SSOP and TSSOP packages only.

Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

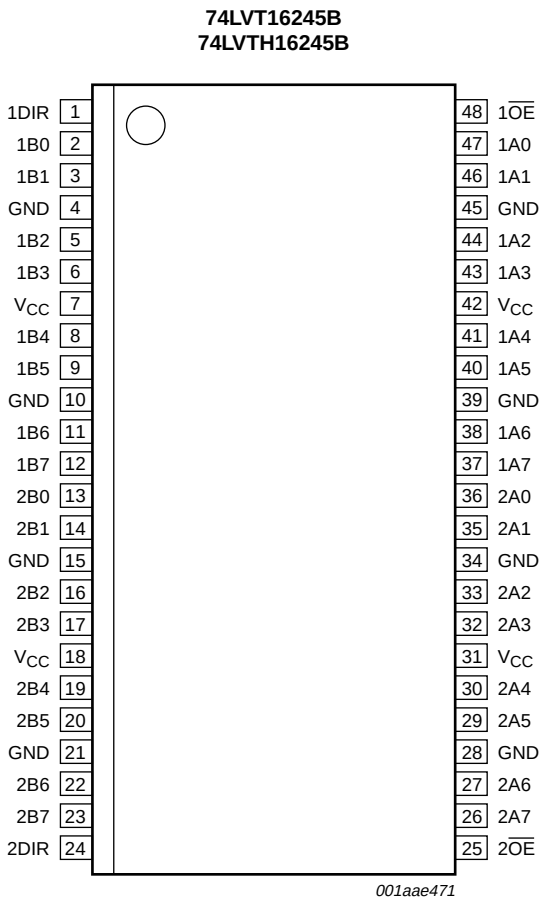


Fig 3. Pin configuration for SSOP48 and TSSOP48

74LVT16245B

	1	2	3	4	5	6
A	1DIR	n.c.	n.c.	n.c.	n.c.	1OE
B	1B1	1B0	GND	GND	1A0	1A1
C	1B3	1B2	VCC	VCC	1A2	1A3
D	1B5	1B4	GND	GND	1A4	1A5
E	1B7	1B6			1A6	1A7
F	2B0	2B1			2A1	2A0
G	2B2	2B3	GND	GND	2A3	2A2
H	2B4	2B5	VCC	VCC	2A5	2A4
J	2B6	2B7	GND	GND	2A7	2A6
K	2DIR	n.c.	n.c.	n.c.	n.c.	2OE

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Transparent top view

Fig 4. Pin configuration for VFBGA56

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1DIR	1	A1	direction control input 1DIR
n.c.	-	A2, A3	not connected
1B0	2	B2	data input/output 1B0
1B1	3	B1	data input/output 1B1
GND	4	B3	ground (0 V)
1B2	5	C2	data input/output 1B2
1B3	6	C1	data input/output 1B3
V_{CC}	7	C3	supply voltage

Table 3. Pin description *...continued*

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1B4	8	D2	data input/output 1B4
1B5	9	D1	data input/output 1B5
GND	10	D3	ground (0 V)
1B6	11	E2	data input/output 1B6
1B7	12	E1	data input/output 1B7
2B0	13	F1	data input/output 2B0
2B1	14	F2	data input/output 2B1
GND	15	G3	ground (0 V)
2B2	16	G1	data input/output 2B2
2B3	17	G2	data input/output 2B3
V_{CC}	18	H3	supply voltage
2B4	19	H1	data input/output 2B4
2B5	20	H2	data input/output 2B5
GND	21	J3	ground (0 V)
2B6	22	J1	data input/output 2B6
2B7	23	J2	data input/output 2B7
2DIR	24	K1	direction control input 2DIR
n.c.	-	K2, K3, K4, K5	not connected
$2\overline{OE}$	25	K6	output enable input $2\overline{OE}$ (active LOW)
2A7	26	J5	data input/output 2A7
2A6	27	J6	data input/output 2A6
GND	28	J4	ground (0 V)
2A5	29	H5	data input/output 2A5
2A4	30	H6	data input/output 2A4
V_{CC}	31	H4	supply voltage
2A3	32	G5	data input/output 2A3
2A2	33	G6	data input/output 2A2
GND	34	G4	ground (0 V)
2A1	35	F5	data input/output 2A1
2A0	36	F6	data input/output 2A0
1A7	37	E6	data input/output 1A7
1A6	38	E5	data input/output 1A6
GND	39	D4	ground (0 V)
1A5	40	D6	data input/output 1A5
1A4	41	D5	data input/output 1A4
V_{CC}	42	C4	supply voltage
1A3	43	C6	data input/output 1A3
1A2	44	C5	data input/output 1A2
GND	45	B4	ground (0 V)

Table 3. Pin description *...continued*

Symbol	Pin		Description
	(T)SSOP48	VFBGA56	
1A1	46	B6	data input/output 1A1
1A0	47	B5	data input/output 1A0
$1\overline{OE}$	48	A6	output enable input $1\overline{OE}$ (active LOW)
n.c.	-	A4, A5	not connected

7. Functional description

7.1 Function table

Table 4. Function table [1]

Control		Input/output	
$n\overline{OE}$	nDIR	nAx	nBx
L	L	output nAx = nBx	input
	H	input	output nBx = nAx
H	X	Z	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH-state	[1]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$		-	–50	mA
I_{OK}	output clamping current	$V_O < 0$		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
I_{OH}	HIGH-state output current		-	-	–32	mA
I_{OL}	LOW-state output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C[1]							
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		-	–0.85	–1.2	V
V_{OH}	HIGH-state output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC}	-	V
		V_{CC} = 2.7 V; I_{OH} = –8 mA		2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = –32 mA		2.0	2.3	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA		-	0.07	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA		-	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA		-	0.4	0.55	V
I_{LI}	input leakage current	control pins					
		V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	0.1	±1	µA
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.1	10	µA
		input/output data pins; V_{CC} = 3.6 V	[2]				
		V_I = 5.5 V		-	0.1	20	µA
		V_I = V_{CC}		-	0.5	10	µA
		V_I = 0 V		-	+0.1	–5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	0.1	±100	µA
I_{HOLD}	bus hold current data input	V_{CC} = 3 V	[3]				
		V_I = 0.8 V		75	135	-	µA
		V_I = 2.0 V		–75	–135	-	µA
		V_{CC} = 0 V to 3.6 V	[3]				
		V_I = 3.6 V		±500	-	-	µA

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 3.0 V		-	75	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care	[4]	-	40	±100	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A					
		outputs HIGH		-	0.07	0.12	mA
		outputs LOW		-	4.7	6	mA
		outputs disabled	[5]	-	0.07	0.12	mA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} – 0.6 V; other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_i	input capacitance pins DIR and $\overline{OE}$	V_O = 0 V or 3.0 V		-	3	-	pF
C_{io}	input/output capacitance pins nAx and nBx	outputs disabled; V_{CC} = 3.6 V; I_O = 0 A V_I = GND or V_{CC}		-	9	-	pF

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus-hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]						
t_{PLH}	LOW-to-HIGH propagation delay nAx to nBx or nBx to nAx	see Figure 5				
		V_{CC} = 2.7 V	-	-	3.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	1.9	3.3	ns
t_{PHL}	HIGH-to-LOW propagation delay nAx to nBx or nBx to nAx	see Figure 5				
		V_{CC} = 2.7 V	-	-	3.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	1.7	3.3	ns
t_{PZH}	output enable time to HIGH-state $n\overline{OE}$ to nAx or nBx	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	4.5	ns
t_{PZL}	output enable time to LOW-state $n\overline{OE}$ to nAx or nBx	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	4.1	ns

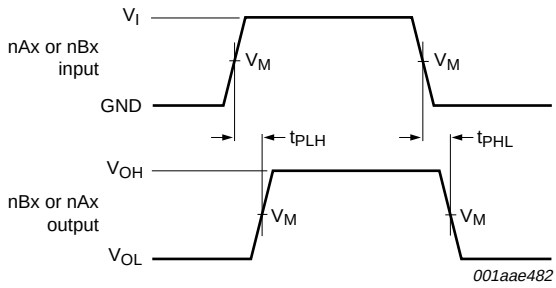
Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time from HIGH-state $n\overline{OE}$ to nAx or nBx	see Figure 6				
		V_{CC} = 2.7 V	-	-	5.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.2	5.1	ns
t_{PLZ}	output disable time from LOW-state $n\overline{OE}$ to nAx or nBx	see Figure 6				
		V_{CC} = 2.7 V	-	-	4.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	3.0	4.6	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

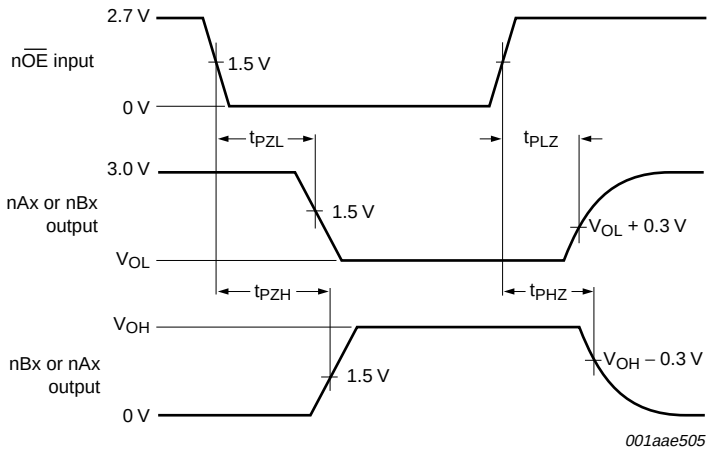
12. Waveforms



V_M = 1.5 V

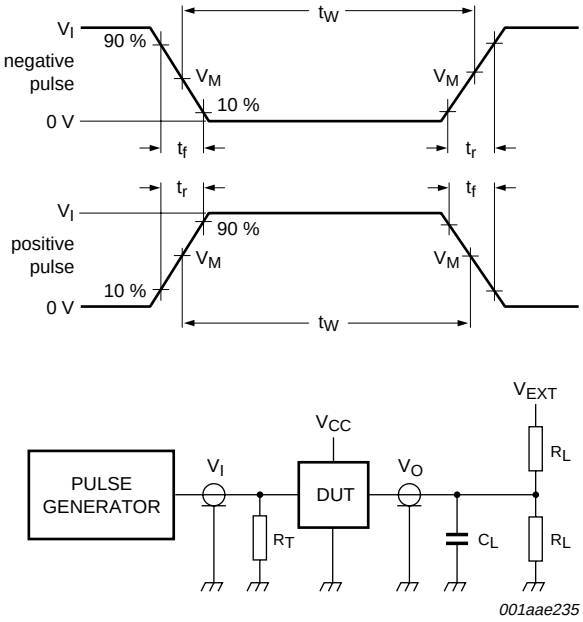
V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. Input to output propagation delays



V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 6. 3-state output enable and disable times



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

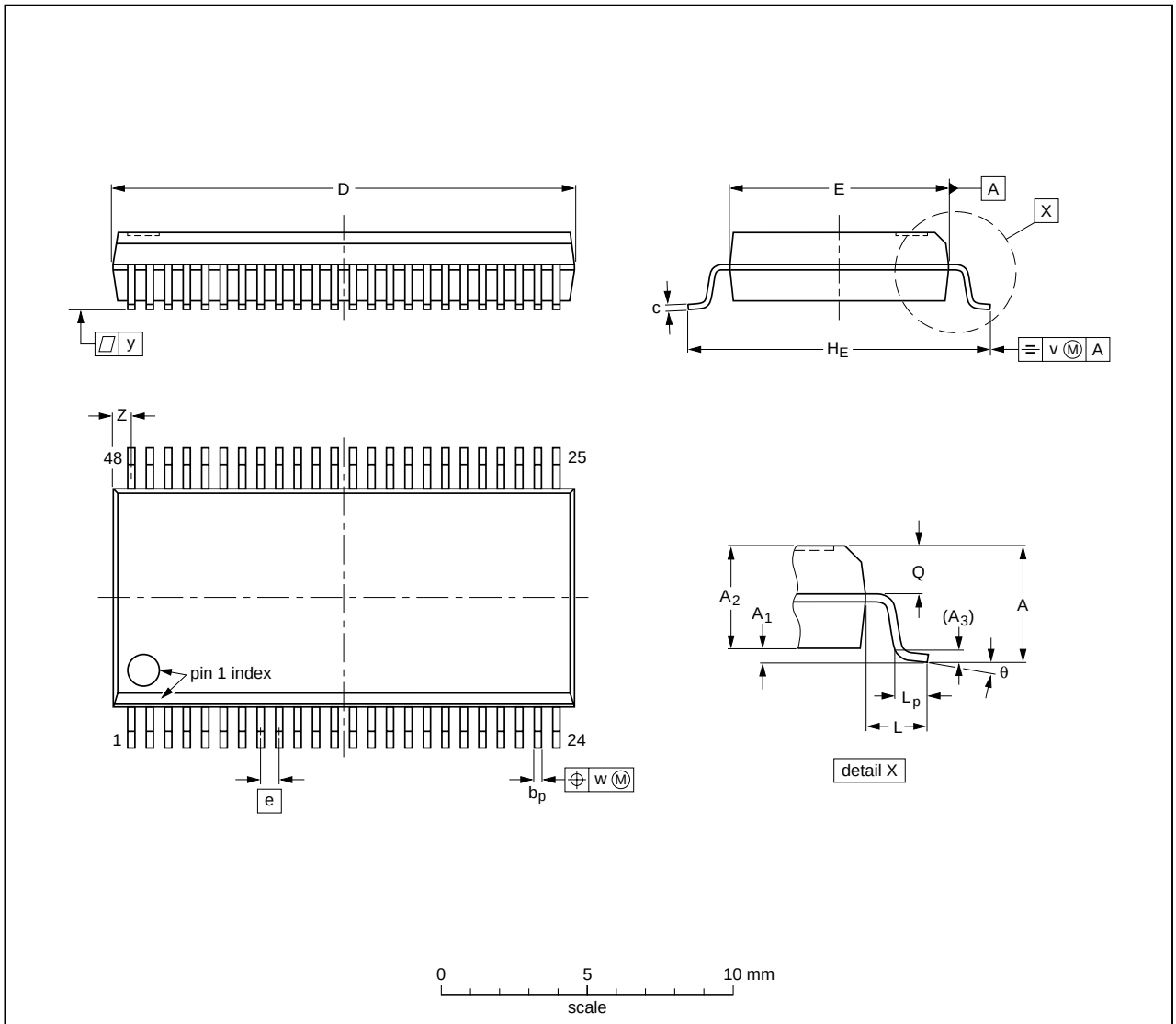
Fig 7. Load circuitry for switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

13. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

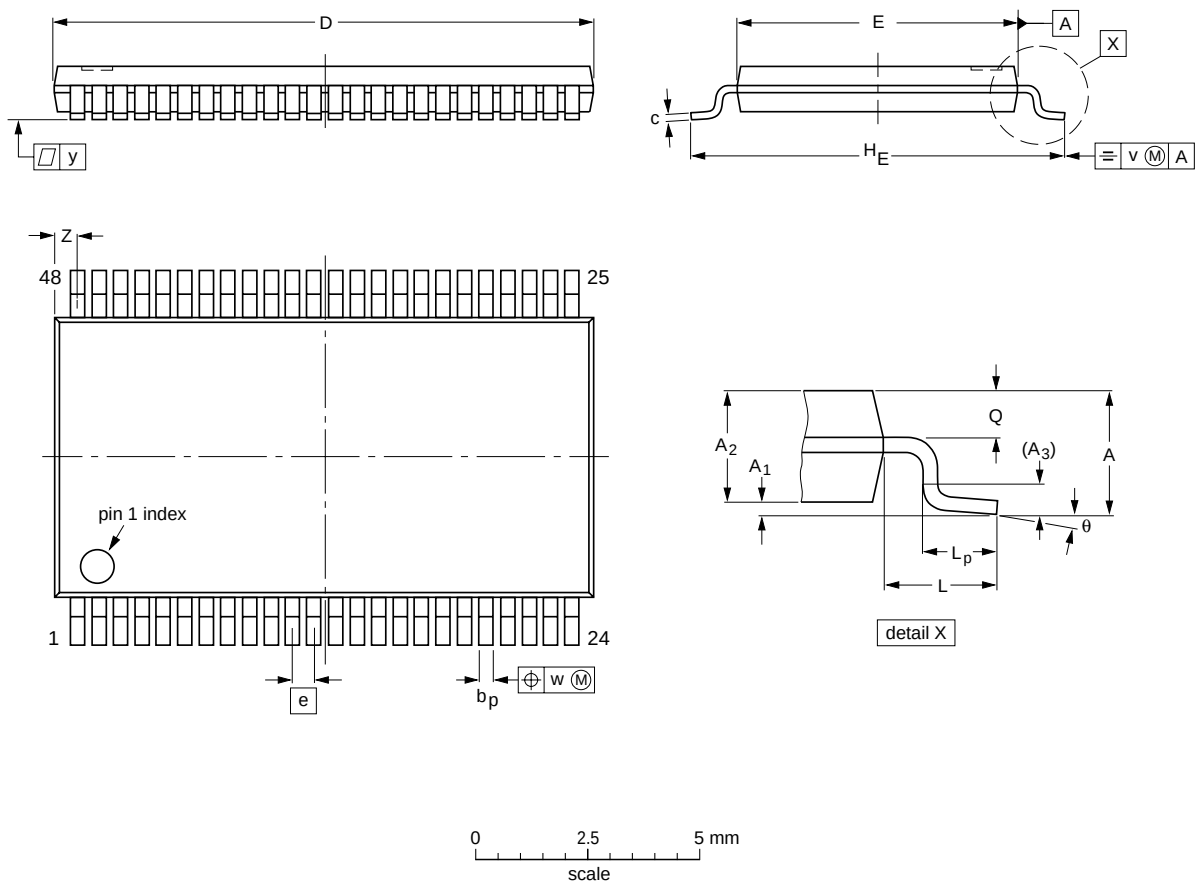
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

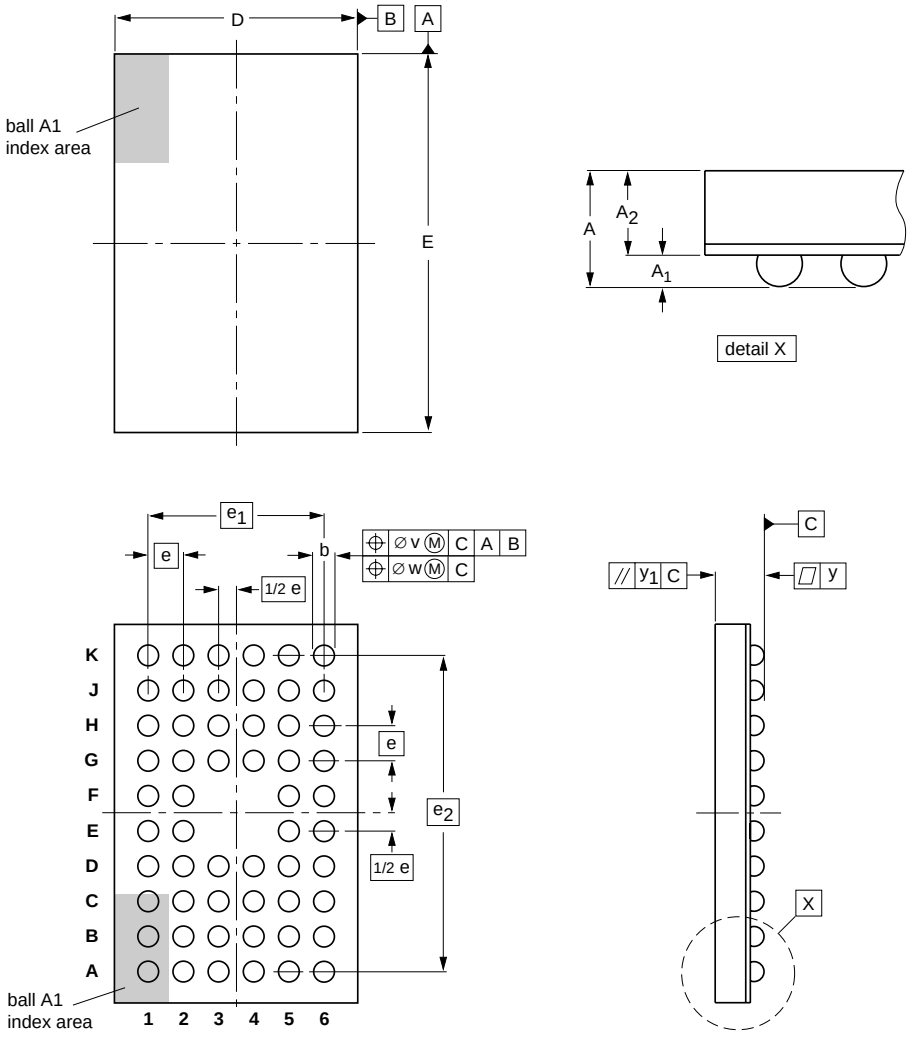
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT362-1 (TSSOP48)

VFBGA56: plastic very thin fine-pitch ball grid array package; 56 balls; body 4.5 x 7 x 0.65 mm **SOT702-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1	0.3 0.2	0.7 0.6	0.45 0.35	4.6 4.4	7.1 6.9	0.65	3.25	5.85	0.15	0.08	0.08	0.1

0 2.5 5 mm

scale

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT702-1		MO-225				~~02-08-08~~ 03-07-01

Fig 10. Package outline SOT702-1 (VFBGA56)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16245B_4	20060323	Product data sheet	-	74LVT16245B_3 (9397 750 09135)
Modifications:	• The format of this data sheet is redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Section 2 “Features”: changed JEDEC Std. 17 into JESD78 • Section 4 “Ordering information”: added type numbers 74LVTH16245BDGG and 74LVTH16245BDL			
74LVT16245B_3 (9397 750 09135)	20021031	Product data sheet	-	74LVT16245B_2 (9397 750 03552)
74LVT16245B_2 (9397 750 03552)	19980219	Product specification	-	74LVT16245B_1
74LVT16245B_1	19940523	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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