

74LVC4245A

Octal dual supply translating transceiver; 3-state

Rev. 06 — 18 January 2008

Product data sheet

1. General description

The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

The device features an output enable input (pin $\overline{\text{OE}}$) for easy cascading and a send/receive input (pin DIR) for direction control. Pin $\overline{\text{OE}}$ controls the outputs so that the buses are effectively isolated.

In suspend mode, when V_{CCA} is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than V_{diode} (typical 0.7 V).

$V_{\text{CCA}} \geq V_{\text{CCB}}$, except in suspend mode.

2. Features

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range:
 - ◆ 3 V port (V_{CCB}): 1.5 V to 3.6 V
 - ◆ 5 V port (V_{CCA}): 1.5 V to 5.5 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when $V_{\text{CC}} = 0$ V
- Complies with JEDEC standard no. JESD8B/JESD36
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|--------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74LVC4245AD | -40 °C to +125 °C | SO24 | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |
| 74LVC4245ADB | -40 °C to +125 °C | SSOP24 | plastic shrink small outline package; 24 leads; body width 5.3 mm | SOT340-1 |
| 74LVC4245APW | -40 °C to +125 °C | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm | SOT355-1 |
| 74LVC4245ABQ | -40 °C to +125 °C | DHVQFN24 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm | SOT815-1 |

4. Functional diagram

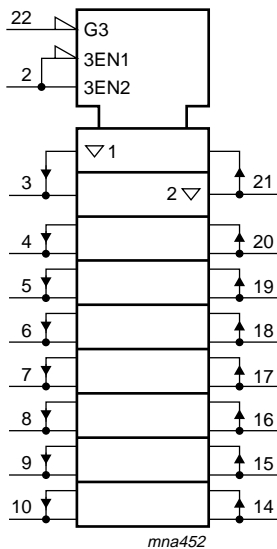


Fig 1. IEC Logic symbol

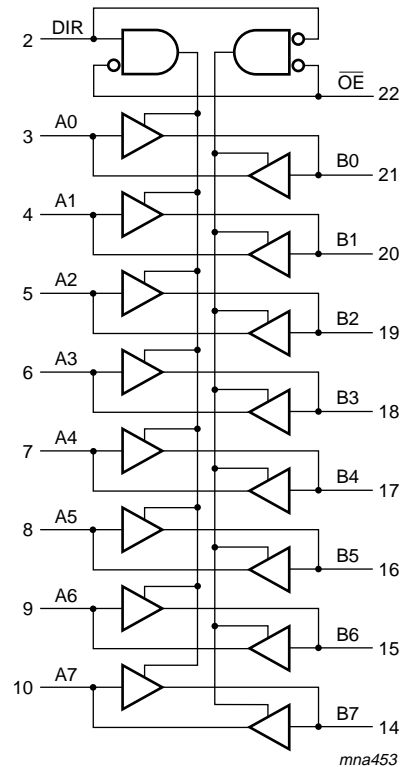
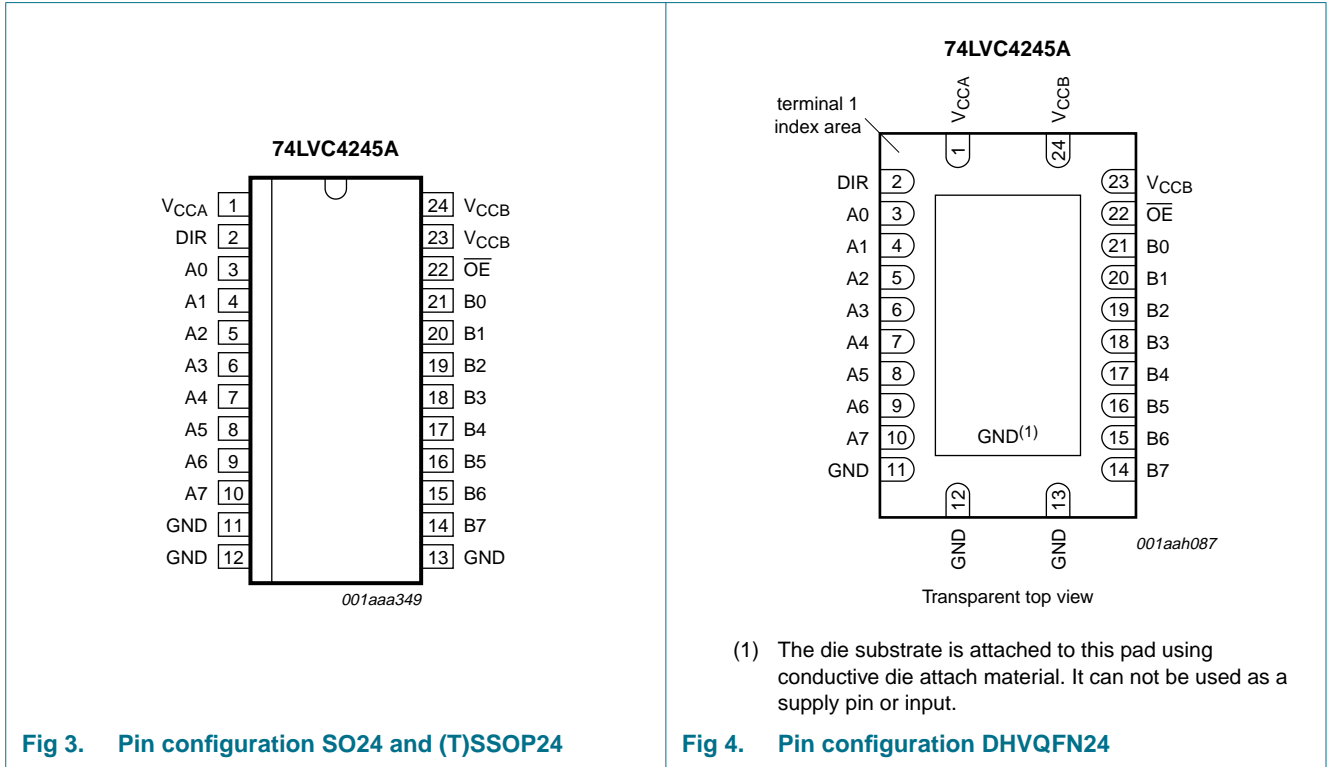


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|------------------|--------------------------------|----------------------------------|
| V _{CCA} | 1 | supply voltage (5 V bus) |
| V _{CCB} | 23, 24 | supply voltage (3 V bus) |
| GND | 11, 12, 13 | ground (0 V) |
| DIR | 2 | direction control |
| A[0:7] | 3, 4, 5, 6, 7, 8, 9, 10 | data input or output |
| B[0:7] | 21, 20, 19, 18, 17, 16, 15, 14 | data input or output |
| \overline{OE} | 22 | output enable input (active LOW) |

6. Functional description

Table 3. Functional table^[1]

| Input | | Input/output | | |
|-----------------|-----|--------------|-------|--|
| \overline{OE} | DIR | An | Bn | |
| L | L | A = B | input | |
| L | H | input | B = A | |
| H | X | Z | Z | |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|----------|----------------|------|
| V_{CCA} | supply voltage 5 V port | | -0.5 | +6.5 | V |
| V_{CCB} | supply voltage 3 V port | | -0.5 | +4.6 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| V_O | output voltage | output HIGH or LOW state | [1] -0.5 | $V_{CC} + 0.5$ | V |
| | | output 3-state | [1] -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ±50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | power dissipation | $T_{amb} = -40$ °C to +125 °C | [2] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
 For (T)SSOP24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.
 For DHVQFN24 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---|---|-----|-----|----------|------|
| V_{CCA} | supply voltage 5 V port (for maximum speed performance) | $V_{CCA} \geq V_{CCB}$; see Figure 5 | 1.5 | - | 5.5 | V |
| V_{CCB} | supply voltage 3 V port (for low-voltage applications) | $V_{CCA} \geq V_{CCB}$; see Figure 5 | 1.5 | - | 3.6 | V |
| V_I | input voltage | for control inputs | 0 | - | 5.5 | V |
| V_O | output voltage | output HIGH or LOW state | 0 | - | V_{CC} | V |
| | | output 3-state | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |

Table 5. Recommended operating conditions ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---|-----|-----|-----|------|
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CCB} = 2.7 \text{ V to } 3.0 \text{ V}$ | - | - | 20 | ns/V |
| | | $V_{CCB} = 3.0 \text{ V to } 3.6 \text{ V}$ | - | - | 10 | ns/V |
| | | $V_{CCA} = 3.0 \text{ V to } 4.5 \text{ V}$ | - | - | 20 | ns/V |
| | | $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|---------------------------|--|--------------------------|-----------------------------------|---------|---------------|
| $T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$ | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$ | 2.0 | - | - | V |
| | | $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}$ | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$ | - | - | 0.8 | V |
| | | $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}$ | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}; I_O = -100 \text{ } \mu\text{A}$ | $V_{CCB} - 0.2$ | V_{CCB} | - | V |
| | | $V_{CCB} = 2.7 \text{ V}; I_O = -12 \text{ mA}$ | $V_{CCB} - 0.5$ | - | - | V |
| | | $V_{CCB} = 3.0 \text{ V}; I_O = -24 \text{ mA}$ | $V_{CCB} - 0.8$ | - | - | V |
| | | $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}; I_O = -100 \text{ } \mu\text{A}$ | $V_{CCA} - 0.2$ | V_{CCA} | - | V |
| | | $V_{CCA} = 4.5 \text{ V}; I_O = -12 \text{ mA}$ | $V_{CCA} - 0.5$ | - | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | $V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}; I_O = 100 \text{ } \mu\text{A}$ | - | - | 0.20 | V |
| | | $V_{CCB} = 2.7 \text{ V}; I_O = 12 \text{ mA}$ | - | - | 0.40 | V |
| | | $V_{CCB} = 3.0 \text{ V}; I_O = 24 \text{ mA}$ | - | - | 0.55 | V |
| | | $V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V}; I_O = 100 \text{ } \mu\text{A}$ | - | - | 0.20 | V |
| | | $V_{CCA} = 4.5 \text{ V}; I_O = 12 \text{ mA}$ | - | - | 0.40 | V |
| I_I | input leakage current | $V_I = 5.5 \text{ V or GND}$ | - | ± 0.1 | ± 5 | μA |
| | | I_{OZ} | OFF-state output current | $V_I = V_{IH} \text{ or } V_{IL}$ | [2] | |
| I_{CC} | supply current | $I_O = 0 \text{ A}$ | | | | |
| | | $V_{CCB} = 3.6 \text{ V};$ other inputs at V_{CCB} or GND | - | 0.1 | 10 | μA |
| | | $V_{CCA} = 5.5 \text{ V};$ other inputs at V_{CCA} or GND | - | 0.1 | 10 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|--|---------------------------|---|------------------|--------------------|----------|---------|
| ΔI_{CC} | additional supply current | per control pin; $I_O = 0$ A | [3] | | | |
| | | $V_{CCB} = 2.7$ V to 3.6 V; $V_I = V_{CCB} - 0.6$ V; other inputs at V_{CCB} or GND | - | 5 | 500 | μ A |
| | | $V_{CCA} = 4.5$ V to 5.5 V; $V_I = V_{CCA} - 0.6$ V; other inputs at V_{CCA} or GND | - | 5 | 500 | μ A |
| C_I | input capacitance | | - | 4.0 | - | pF |
| $C_{I/O}$ | input/output capacitance | An and Bn | - | 5.0 | - | pF |
| $T_{amb} = -40$ °C to $+125$ °C | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CCB} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| | | $V_{CCA} = 4.5$ V to 5.5 V | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CCB} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| | | $V_{CCA} = 4.5$ V to 5.5 V | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $V_{CCB} = 2.7$ V to 3.6 V; $I_O = -100$ μ A | $V_{CCB} - 0.3$ | - | - | V |
| | | $V_{CCB} = 2.7$ V; $I_O = -12$ mA | $V_{CCB} - 0.65$ | - | - | V |
| | | $V_{CCB} = 3.0$ V; $I_O = -24$ mA | $V_{CCB} - 1.0$ | - | - | V |
| | | $V_{CCA} = 4.5$ V to 5.5 V; $I_O = -100$ μ A | $V_{CCA} - 0.3$ | - | - | V |
| | | $V_{CCA} = 4.5$ V; $I_O = -12$ mA | $V_{CCA} - 0.65$ | - | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $V_{CCB} = 2.7$ V to 3.6 V; $I_O = 100$ μ A | - | - | 0.30 | V |
| | | $V_{CCB} = 2.7$ V; $I_O = 12$ mA | - | - | 0.60 | V |
| | | $V_{CCB} = 3.0$ V; $I_O = 24$ mA | - | - | 0.80 | V |
| | | $V_{CCA} = 4.5$ V to 5.5 V; $I_O = 100$ μ A | - | - | 0.30 | V |
| | | $V_{CCA} = 4.5$ V; $I_O = 12$ mA | - | - | 0.60 | V |
| | | $V_{CCA} = 4.5$ V; $I_O = 24$ mA | - | - | 0.80 | V |
| I_I | input leakage current | $V_I = 5.5$ V or GND | - | - | ± 20 | μ A |
| I_{OZ} | OFF-state output current | $V_I = V_{IH}$ or V_{IL} | [2] | | | |
| | | $V_{CCB} = 3.6$ V; $V_O = V_{CCB}$ or GND | - | - | ± 20 | μ A |
| | | $V_{CCA} = 5.5$ V; $V_O = V_{CCA}$ or GND | - | - | ± 20 | μ A |
| I_{CC} | supply current | $I_O = 0$ A | | | | |
| | | $V_{CCB} = 3.6$ V; other inputs at V_{CCB} or GND | - | - | 40 | μ A |
| | | $V_{CCA} = 5.5$ V; other inputs at V_{CCA} or GND | - | - | 40 | μ A |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------------|---------------------------|---|-----|--------------------|------|---------|
| ΔI_{CC} | additional supply current | per control pin; $I_O = 0$ A | [3] | | | |
| | | $V_{CCB} = 2.7$ V to 3.6 V; $V_I = V_{CCB} - 0.6$ V; other inputs at V_{CCB} or GND | - | - | 5000 | μ A |
| | | $V_{CCA} = 4.5$ V to 5.5 V; $V_I = V_{CCA} - 0.6$ V; other inputs at V_{CCA} or GND | - | - | 5000 | μ A |

[1] All typical values are measured at $V_{CCA} = 5.0$ V, $V_{CCB} = 3.3$ V and $T_{amb} = 25$ °C.

[2] For transceivers, the parameter I_{OZ} includes the input leakage current.

[3] $V_{CCB} = 2.7$ V to 3.6 V: other inputs at V_{CCB} or GND.
 $V_{CCA} = 4.5$ V to 5.5 V: other inputs at V_{CCA} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). $V_{CCA} = 4.5$ V to 5.5 V; $t_r = t_f \leq 2.5$ ns. For test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | V_{CCB} | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-----------|-------------------------------------|--|----------------|------------------|--------------------|-----|-------------------|------|------|
| | | | | Min | Typ ^[1] | Max | Min | Max | |
| t_{PHL} | HIGH to LOW propagation delay | An to Bn; see Figure 6 | 2.7 V | 1.0 | 3.6 | 6.3 | 1.0 | 8.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.3 | 6.3 | 1.0 | 8.0 | ns |
| | | Bn to An; see Figure 6 | 2.7 V | 1.0 | 3.4 | 6.1 | 1.0 | 8.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.4 | 6.1 | 1.0 | 8.0 | ns |
| t_{PLH} | LOW to HIGH propagation delay | An to Bn; see Figure 6 | 2.7 V | 1.0 | 3.3 | 6.7 | 1.0 | 8.5 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 2.8 | 6.5 | 1.0 | 8.5 | ns |
| | | Bn to An; see Figure 6 | 2.7 V | 1.0 | 3.0 | 5.0 | 1.0 | 6.5 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.0 | 5.0 | 1.0 | 6.5 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | \overline{OE} to An; see Figure 7 | 2.7 V | 1.0 | 4.5 | 9.0 | 1.0 | 11.5 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 4.5 | 9.0 | 1.0 | 11.5 | ns |
| | | \overline{OE} to Bn; see Figure 7 | 2.7 V | 1.0 | 4.4 | 8.7 | 1.0 | 11.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.8 | 8.1 | 1.0 | 10.5 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | \overline{OE} to An; see Figure 7 | 2.7 V | 1.0 | 4.5 | 8.1 | 1.0 | 10.5 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 4.5 | 8.1 | 1.0 | 10.5 | ns |
| | | \overline{OE} to Bn; see Figure 7 | 2.7 V | 1.0 | 4.3 | 8.7 | 1.0 | 11.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.2 | 8.1 | 1.0 | 10.5 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | \overline{OE} to An; see Figure 7 | 2.7 V | 1.0 | 2.9 | 7.0 | 1.0 | 9.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 2.9 | 7.0 | 1.0 | 9.0 | ns |
| | | \overline{OE} to Bn; see Figure 7 | 2.7 V | 1.0 | 3.9 | 7.7 | 1.0 | 10.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 3.5 | 7.7 | 1.0 | 10.0 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | \overline{OE} to An; see Figure 7 | 2.7 V | 1.0 | 2.8 | 5.8 | 1.0 | 7.5 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 2.8 | 5.8 | 1.0 | 7.5 | ns |
| | | \overline{OE} to Bn; see Figure 7 | 2.7 V | 1.0 | 3.3 | 7.8 | 1.0 | 10.0 | ns |
| | | | 3.0 V to 3.6 V | 1.0 | 2.9 | 7.8 | 1.0 | 10.0 | ns |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). $V_{CCA} = 4.5\text{ V to }5.5\text{ V}$; $t_r = t_f \leq 2.5\text{ ns}$. For test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | V_{CCB} | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit | | |
|-------------|-------------------------------|---|-----------|------------------|--------------------|-----|-------------------|-----|------|----|----|
| | | | | Min | Typ ^[1] | Max | Min | Max | | | |
| $t_{sk(o)}$ | output skew time | | | [2] | - | - | 1.0 | - | 1.5 | ns | |
| C_{PD} | power dissipation capacitance | 5 V port: Bn to An; $V_I = \text{GND to } V_{CCA}$; $V_{CCA} = 5.0\text{ V}$ | | [3] | outputs enabled | - | 17 | - | - | - | pF |
| | | | | | outputs disabled | - | 5 | - | - | - | pF |
| | | 3 V port: An to Bn; $V_I = \text{GND to } V_{CCB}$; $V_{CCB} = 3.3\text{ V}$ | | [3] | outputs enabled | - | 17 | - | - | - | pF |
| | | | | | outputs disabled | - | 5 | - | - | - | pF |

- [1] Typical values are measured at $T_{amb} = 25\text{ °C}$, $V_{CCA} = 5.0\text{ V}$, and $V_{CCB} = 2.7\text{ V}$ and 3.3 V respectively.
- [2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. AC waveforms

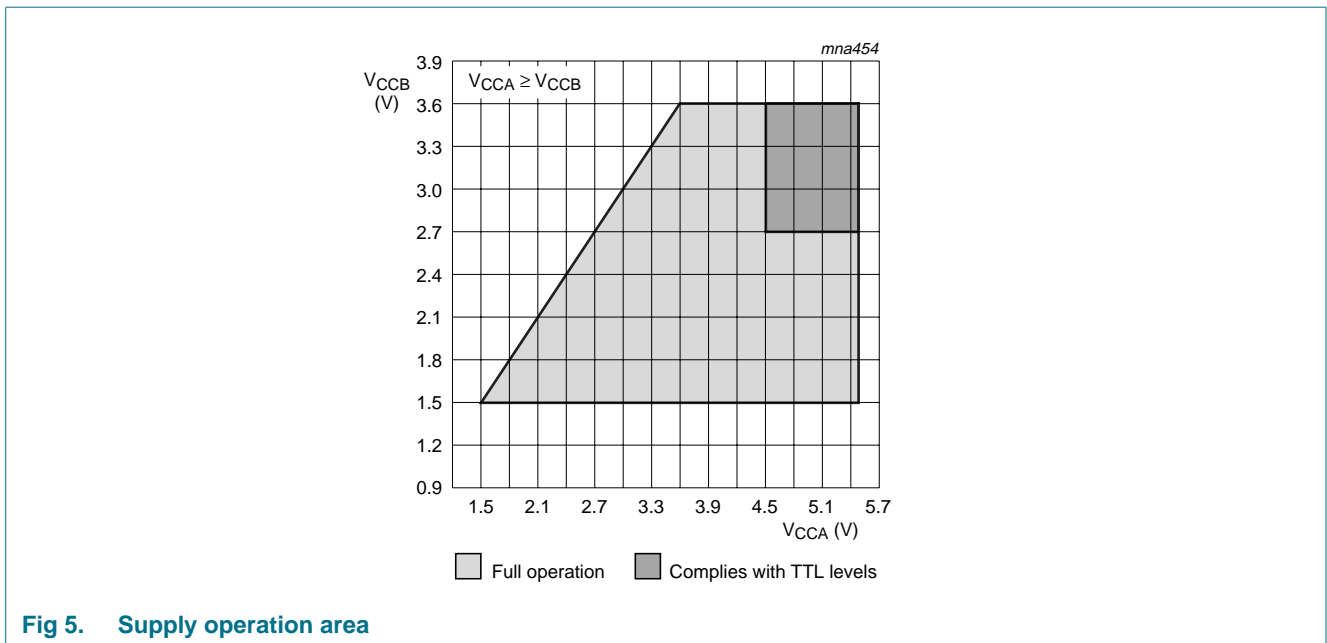
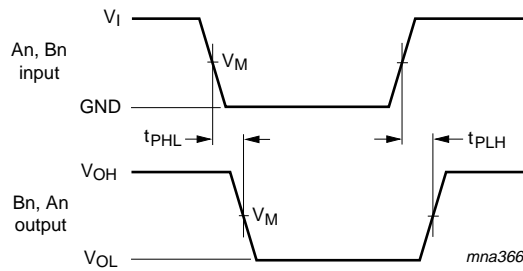


Fig 5. Supply operation area

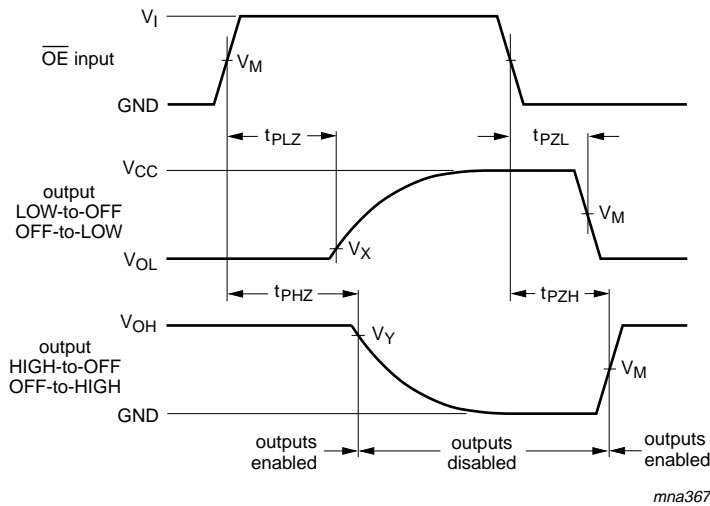


$V_M = 1.5\text{ V}$ at $2.7\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$;

$V_M = 0.5V_{CCA}$ at $V_{CCA} \geq 4.5\text{ V}$.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 6. Input (An, Bn) to output (Bn, An) propagation delays



$V_M = 1.5\text{ V}$ at $2.7\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$;

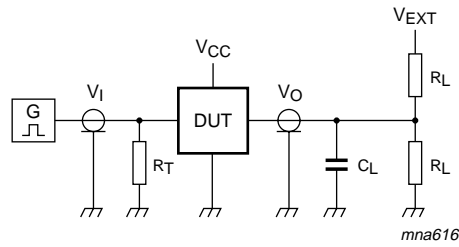
$V_M = 0.5V_{CCA}$ at $V_{CCA} \geq 4.5\text{ V}$.

$V_X = V_{OL} + 0.3\text{ V}$ at $V_{CCB} \geq 2.7\text{ V}$;

$V_Y = V_{OH} - 0.3\text{ V}$ at $V_{CCB} \geq 2.7\text{ V}$.

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 7. 3-state enable and disable times



Test data is given in [Table 8](#). Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Load circuitry for switching times

Table 8. Test data

| Supply voltage | | Input | Load | | V_{EXT} | | |
|----------------|----------------|-----------|-------|--------------|--------------------|--------------------|------------------------|
| V_{CCA} | V_{CCB} | V_I [1] | C_L | R_L | t_{PLH}, t_{PHL} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} [2] |
| < 2.7 V | < 2.7 V | V_{CCI} | 50 pF | 500 Ω | open | GND | $2 \times V_{CCO}$ |
| - | 2.7 V to 3.6 V | 2.7 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CCO}$ |
| 4.5 V to 5.5 V | - | 3.0 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CCO}$ |

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

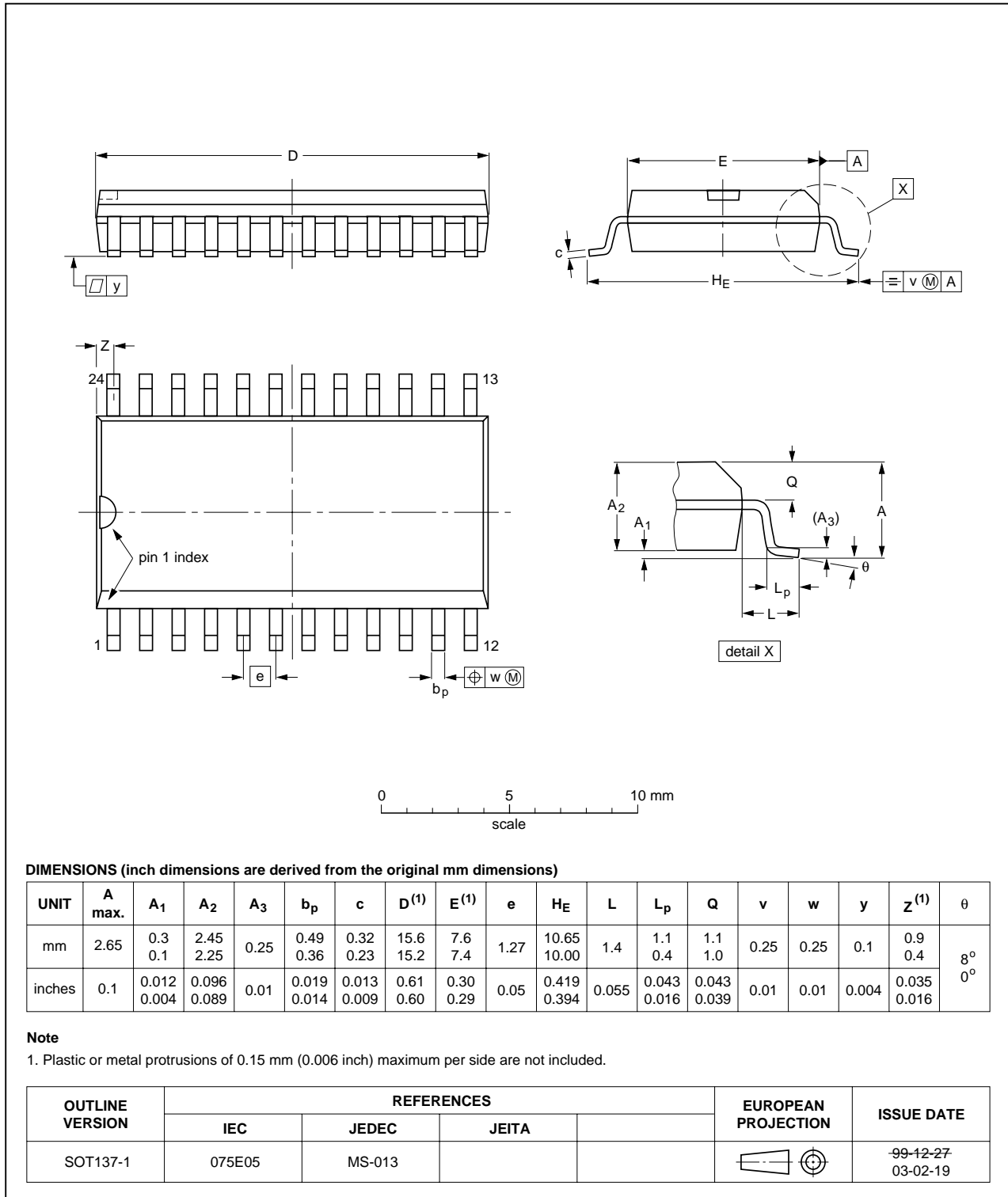


Fig 9. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

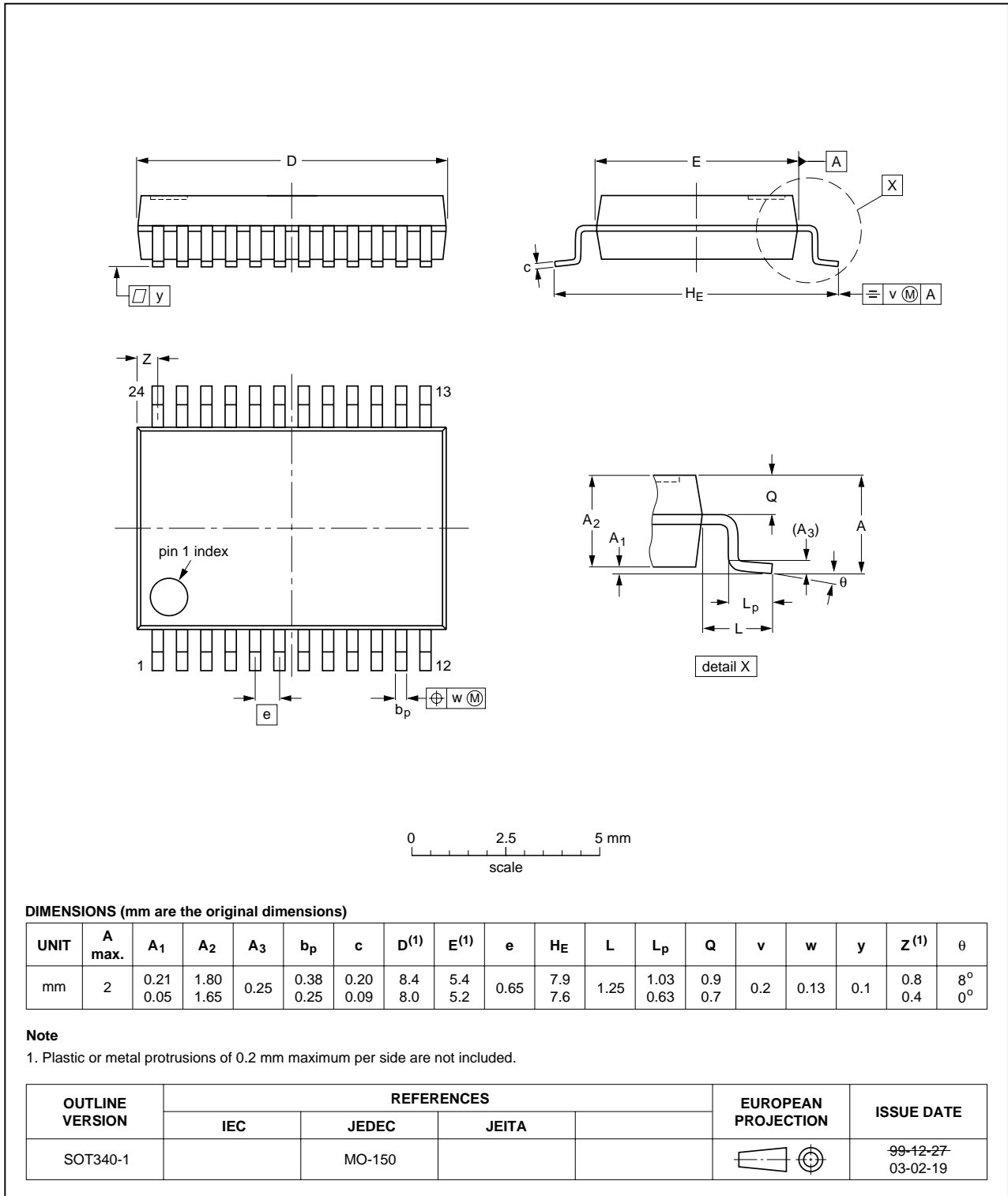


Fig 10. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

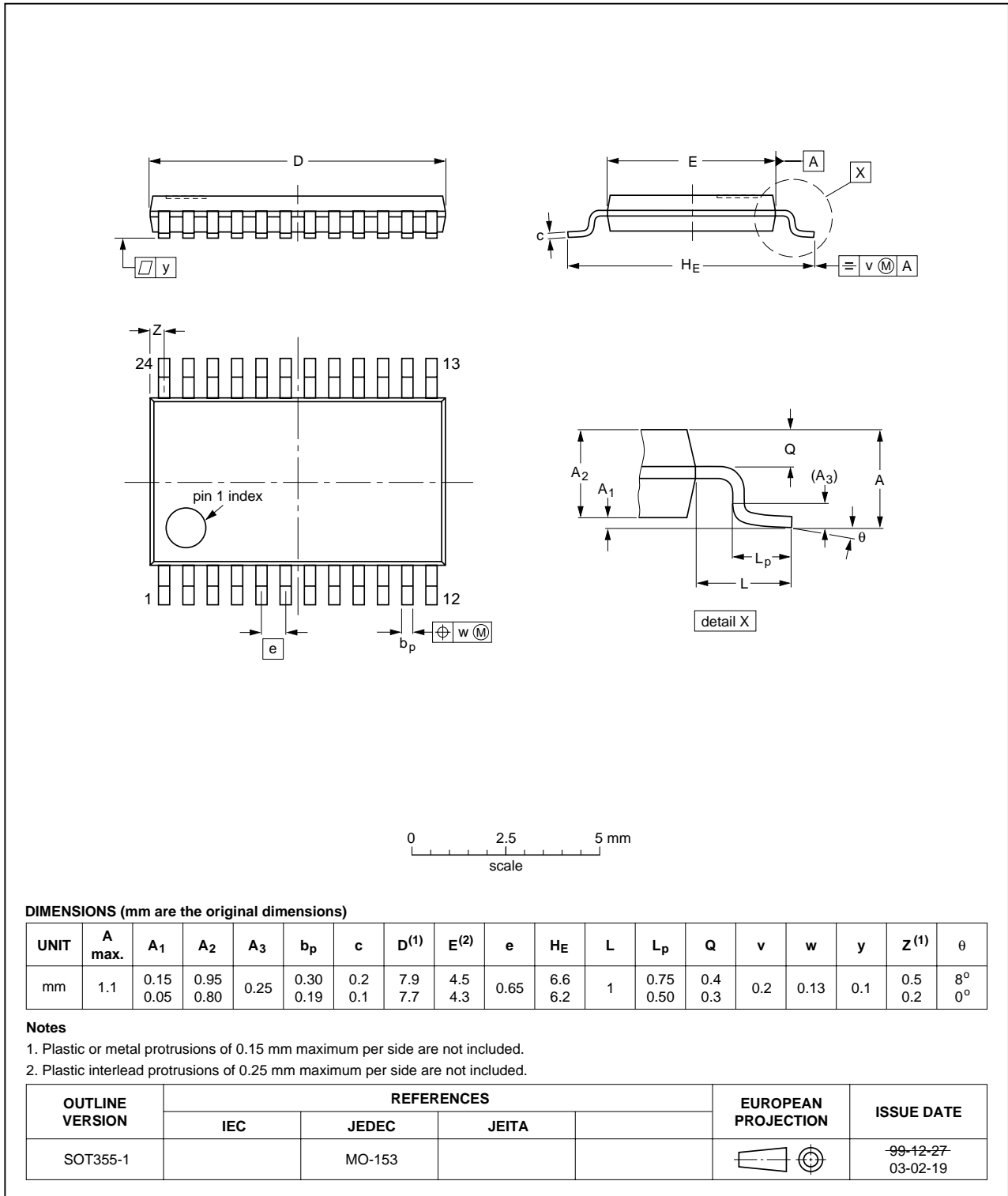


Fig 11. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

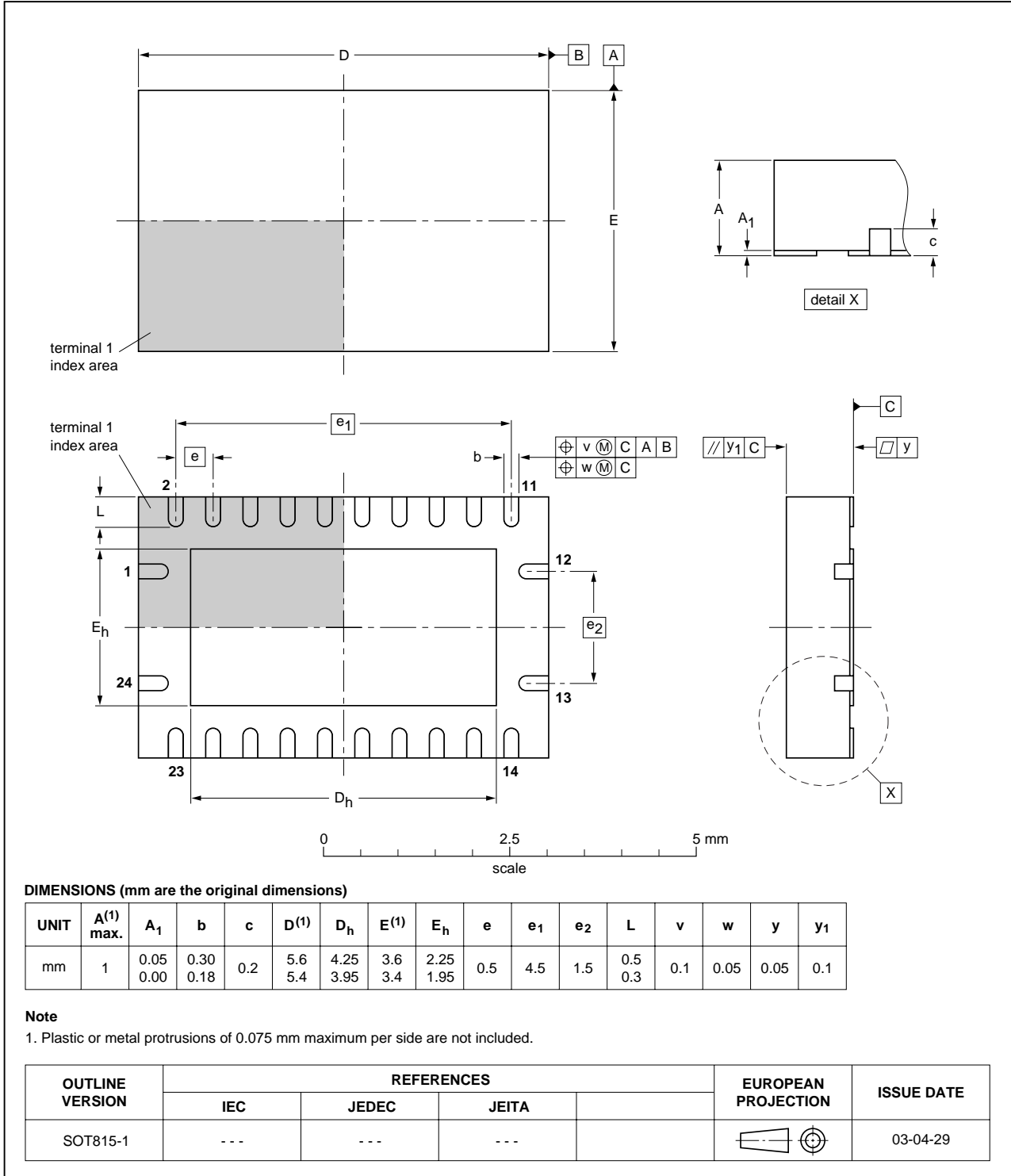


Fig 12. Package outline SOT815-1 (DHVQFN24)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|--------------|
| 74LVC4245A_6 | 20080118 | Product data sheet | - | 74LVC4245A_5 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN24 package added. Section 7: derating values added for DHVQFN24 package. Section 12: outline drawing added for DHVQFN24 package. | | | |
| 74LVC4245A_5 | 20040330 | Product specification | - | 74LVC4245A_4 |
| 74LVC4245A_4 | 20040211 | Product specification | - | 74LVC4245A_3 |
| 74LVC4245A_3 | 19990615 | Product specification | - | 74LVC4245A_2 |
| 74LVC4245A_2 | 19980729 | Product specification | - | 74LVC4245A_1 |
| 74LVC4245A_1 | 19980729 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

15.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental

damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

17. Contents

1 General description 1

2 Features 1

3 Ordering information 2

4 Functional diagram 2

5 Pinning information 3

5.1 Pinning 3

5.2 Pin description 3

6 Functional description 4

7 Limiting values 4

8 Recommended operating conditions 4

9 Static characteristics 5

10 Dynamic characteristics 7

11 AC waveforms 8

12 Package outline 11

13 Abbreviations 15

14 Revision history 15

15 Legal information 16

15.1 Data sheet status 16

15.2 Definitions 16

15.3 Disclaimers 16

15.4 Trademarks 16

16 Contact information 16

17 Contents 17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

