DATA SHEET

74LVC652

Octal transceiver/register with dual enable (3-State)

Product specification
Supercedes data of 1993 Dec 01
IC24 Data Handbook

1998 Jul 29

Philips
Semiconductors

PHILIPS

Octal transceiver/register with dual enable (3-State) 74LVC652

*FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC652 is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC652 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropriate clock inputs (CPAB or CPBA) regardless of the select inputs (SAB and SBA) or output enable (OEAB and $\overline{OE}$BA) control inputs. Depending on the select inputs SAB and SBA data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OEn inputs this operating mode permits. The output enable inputs OEAB and OEBA determine the operation mode of the transceiver.

When OEAB is LOW, no data transmission from An to Bn is possible and when $\overline{OE}$BA is HIGH, there is no data transmission from Bn to An possible. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OE}$BA. In this configuration each output reinforces its input.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A_n to B_n; B_n to A_n	C_L = 50pF V_{CC} = 3.3V	5.0	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	45	pF

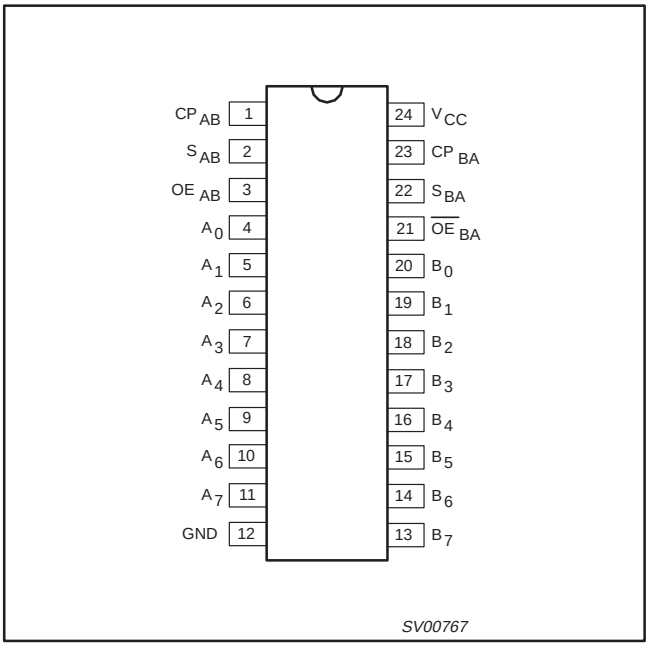
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	–40°C to +85°C	74LVC652 D	74LVC652 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74LVC652 DB	74LVC652 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74LVC652 PW	4LVC652PW DH	SOT355-1

PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP_{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S_{AB}	Select 'A' to 'B' source input
3	OE_{AB}	Output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A_0 to A_7	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B_0 to B_7	'B' data inputs/outputs
21	$\overline{OE}_{BA}$	Output enable A to B input
22	S_{BA}	Select 'B' to 'A' source input
23	CP_{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V_{CC}	Positive supply voltage

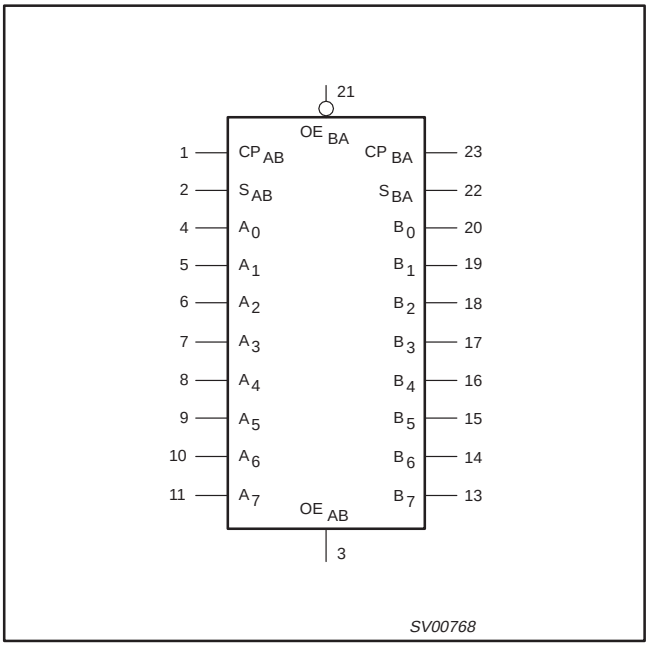
FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE_{AB}	$\overline{OE}_{BA}$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}	A_0 to A_7	B_0 to B_7	
L L	H H	H or L ↑	H or L ↑	X X	X X	input	input	isolation store A and B data
X H	H H	↑ ↑	H or L ↑	X L	X X	input input	un * output	store A, hold B, store A in both registers
L L	X L	H or L ↑	↑ ↑	X X	X L	un * output	input input	hold A, store B, store B in both registers
L L	L L	X X	X H or L	X X	L H	output	input	real-time B data to A bus stored B data to A bus
H H	H H	X H or L	X X	L H	X X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

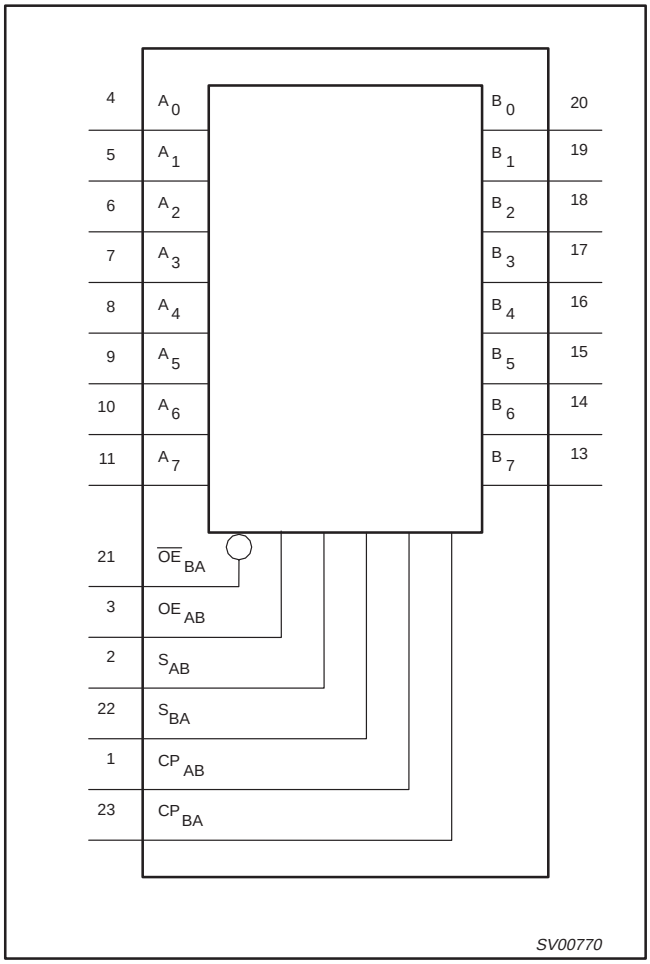
* The data output functions may be enabled or disabled by various signals at the OE_{AB} and $\overline{OE}_{BA}$ inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

un = unspecified
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW–to–HIGH level transition

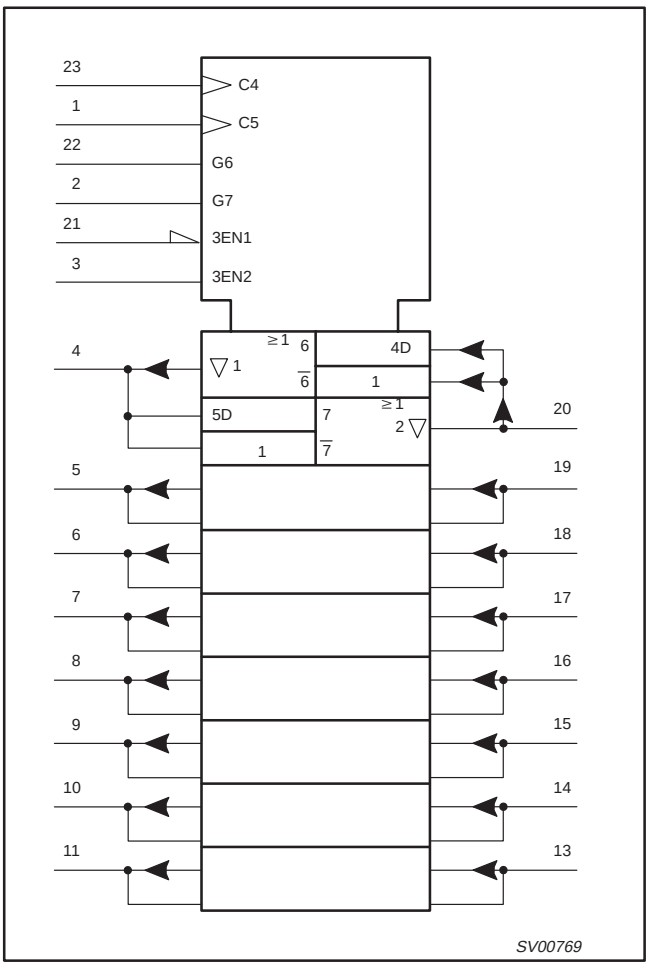
LOGIC SYMBOL



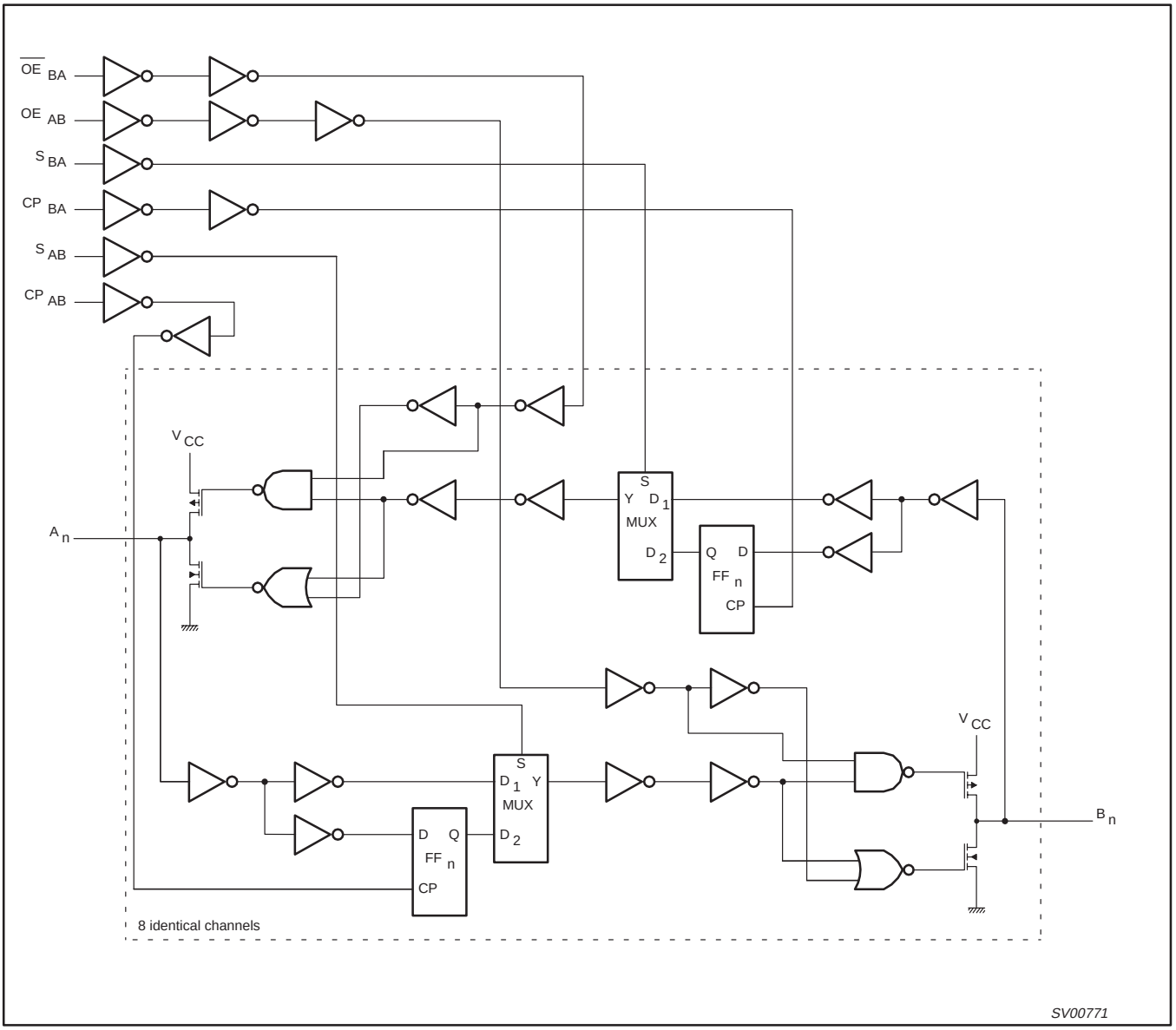
FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_{I/O}$	DC output voltage; output HIGH or LOW	Note 2	–0.5 to V_{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	–0.5 to V_{CC} +0.5	V
I_O	DC output diode current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 2.7 to 3.6V	2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V			GND	V
		V_{CC} = 2.7 to 3.6V			0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = –12mA	V_{CC} – 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –18mA	V_{CC} – 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = –24mA	V_{CC} – 0.8			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA			0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or $V_{IL;}$ I_O = 24mA			0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND; Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; V_I = 5.5V or GND		±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; V_O = 5.5V or GND		0.1	±10	µA
I_{OFF}	Power off leakage current	V_{CC} = 0.0V; V_I = 5.5V; V_O = 5.5V		0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0		0.1	10	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ –0.6V; I_O = 0		5	500	µA

NOTES:

1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V		V_{CC} = 1.2V		
			MIN	TYP[1]	MAX	MIN	MAX	MIN	TYP	
t_{PHL}/t_{PLH}	Propagation delay An to Bn, Bn to An	Figures 1, 5	1.5	4.6	7.9	1.5	9.2	1.5	24	ns
t_{PHL}/t_{PLH}	Propagation delay CP_{AB}, CP_{BA} to B_n, A_n	Figures 2, 5	1.5	5.2	8.9	1.5	11	1.5	26	ns
t_{PHL}/t_{PLH}	Propagation delay S_{AB}, S_{BA} to B_n, A_n	Figures 3, 5	1.5	5.2	8.8	1.5	11	1.5	27	ns
t_{PZH}/t_{PZL}	3-State output enable time OE_{AB} to Bn	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OE_{AB} to Bn	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}_{BA}$ to An	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}_{BA}$ to An	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_W	Clock pulse width HIGH or LOW CP_{AB} or CP_{BA}	Figures 4, 5	–	3.0	–	3.0	–	–	–	ns
t_{su}	Set-up time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.5	0.5	–	1.5	–	–	–	ns
t_h	Hold time An, Bn to CP_{AB}, CP_{BA}	Figure 2	1.0	0	–	1.0	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	7.5	150	–	–	–	–	–	MHz

NOTE:
1. These typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

AC WAVEFORMS

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

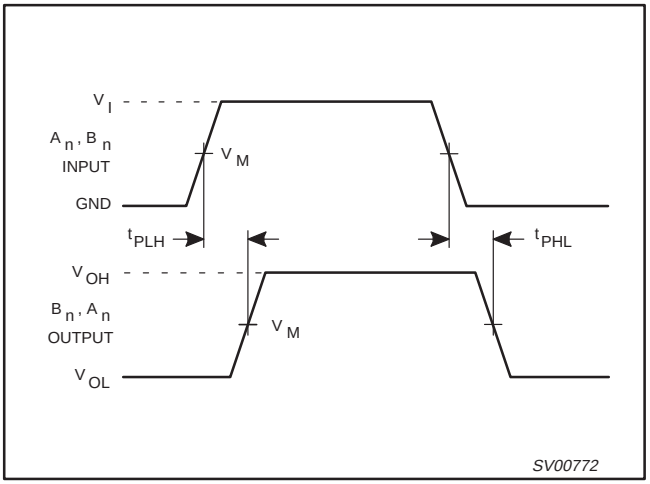


Figure 1. Input An, Bn to output Bn, An propagation delays.

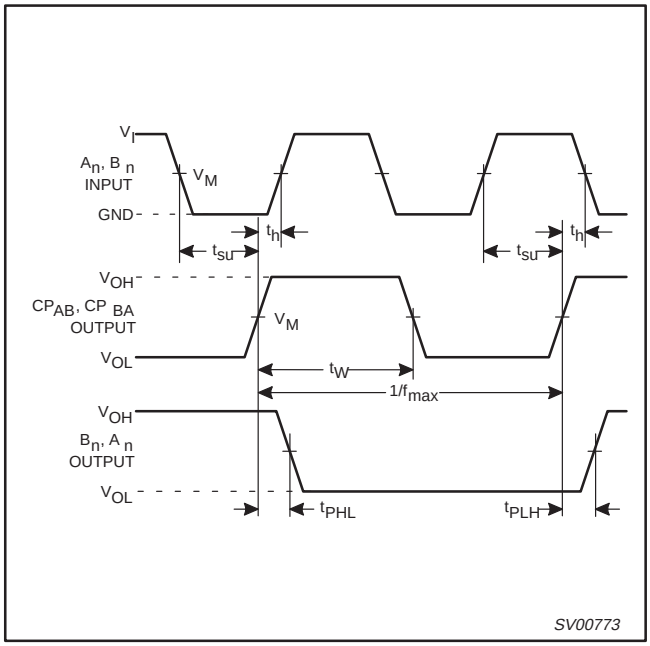


Figure 2. A_n, B_n to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

AC WAVEFORMS (Continued)

V_M = 1.5V at $V_{CC} \geq$ 2.7V
V_M = 0.5V * V_{CC} at V_{CC} < 2.7V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_X = V_{OL}$ + 0.3V at $V_{CC} \geq$ 2.7V
$V_X = V_{OL}$ + 0.1V_{CC} at V_{CC} < 2.7V
$V_Y = V_{OH}$ – 0.3V at $V_{CC} \geq$ 2.7V
$V_Y = V_{OH}$ – 0.1V_{CC} at V_{CC} < 2.7V

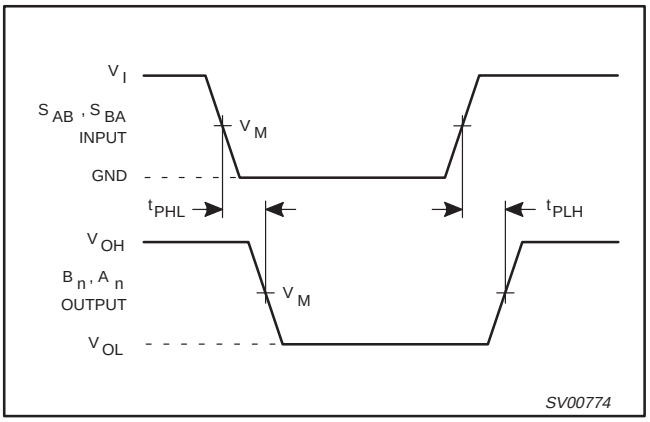


Figure 3. Input S_{AB}, S_{BA} to output B_n, A_n propagation delay times.

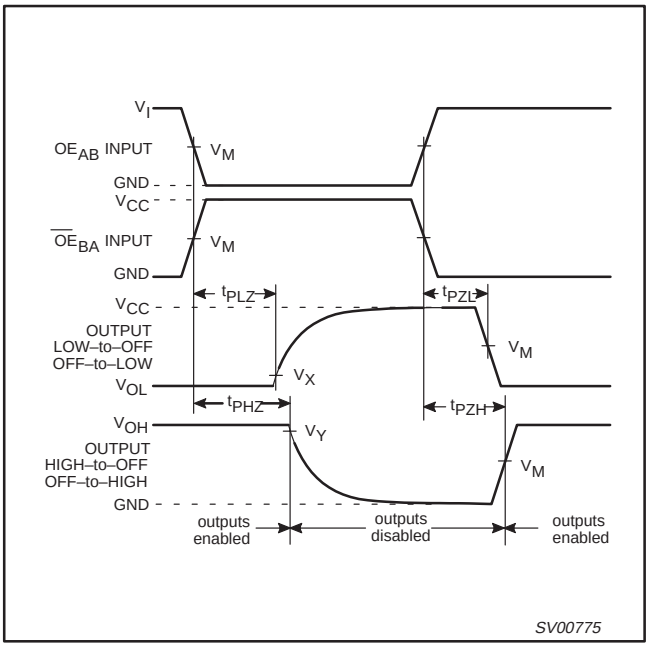
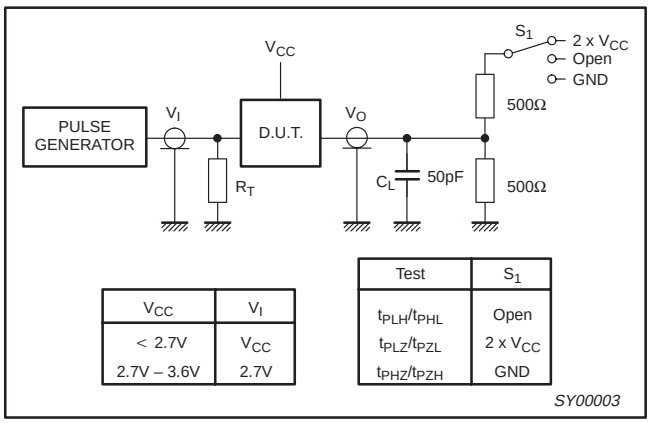


Figure 4. OE inputs (OE_{AB}, $\overline{OE}_{BA}$) to outputs A_n, B_n enable and disable times.

TEST CIRCUIT



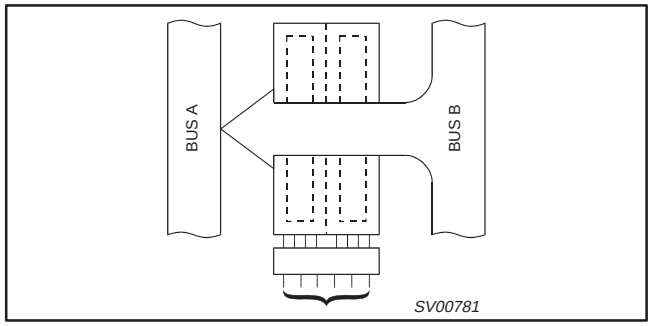
V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

Figure 5. Load circuitry for switching times.

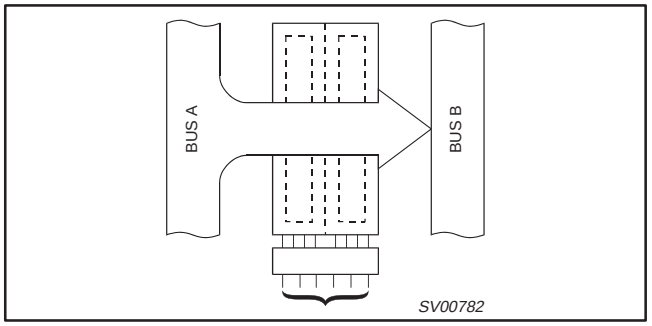
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



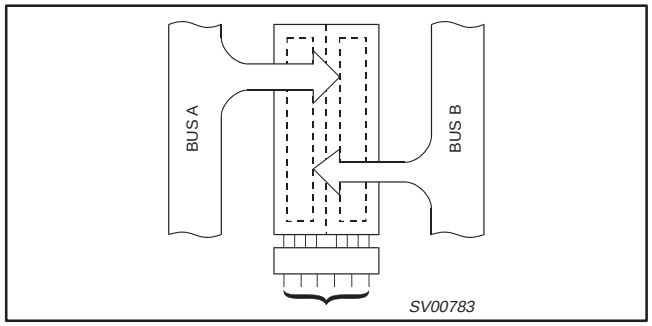
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



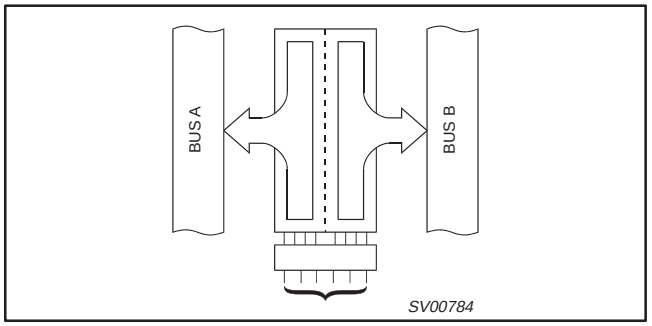
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



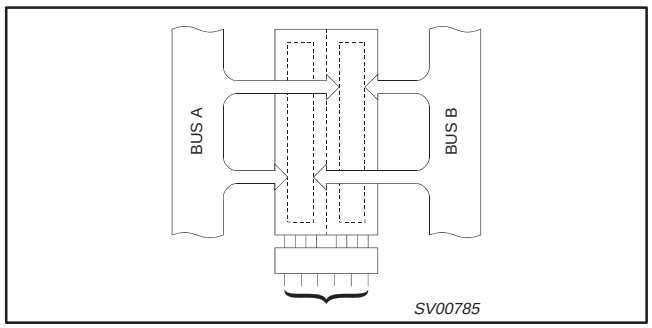
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
X	H	↑	↑	L	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



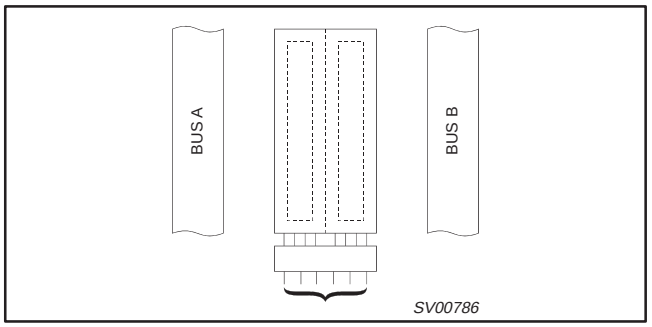
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



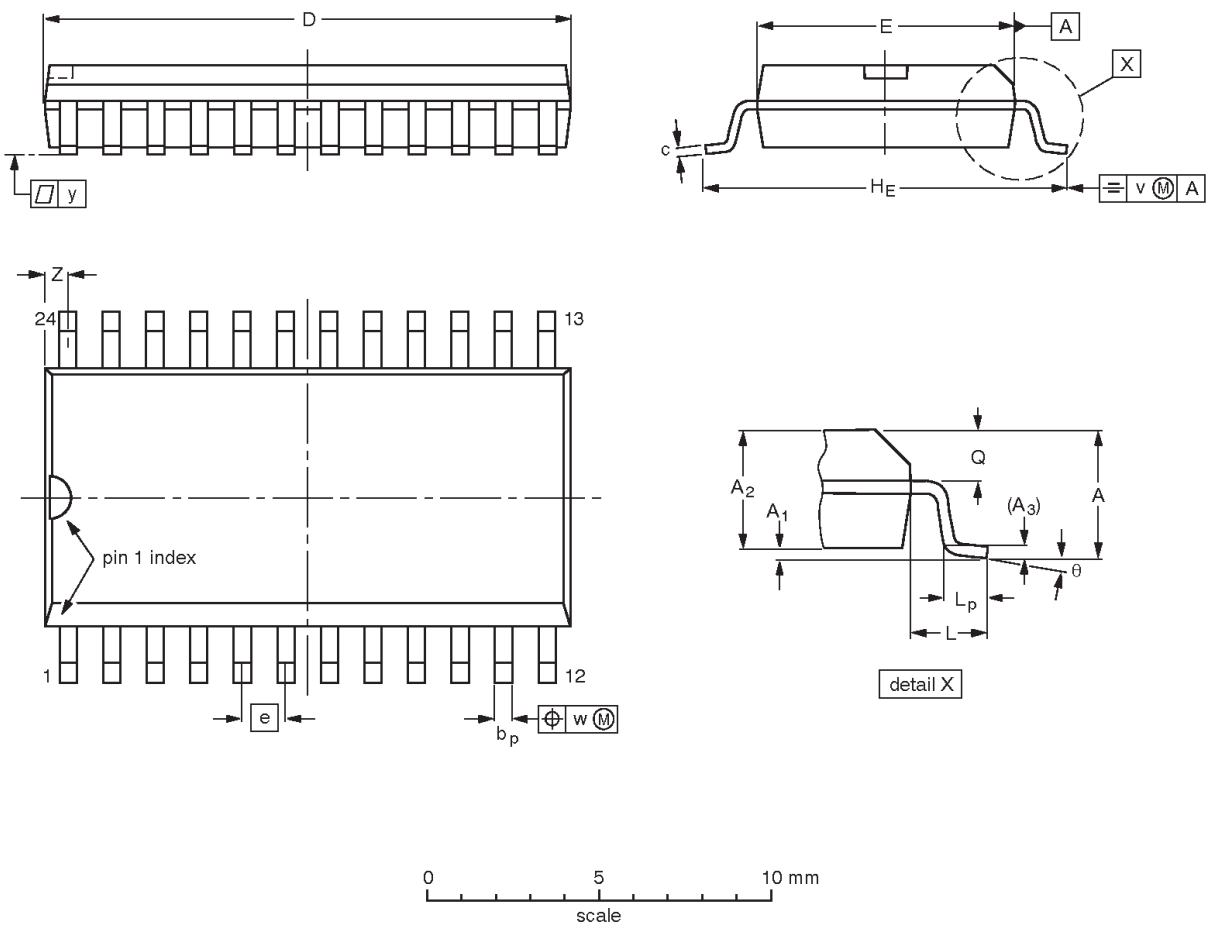
OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



OE_{AB}	$\overline{OE}BA$	CP_{AB}	CP_{BA}	S_{AB}	S_{BA}
L	H	H or L	H or L	X	X

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

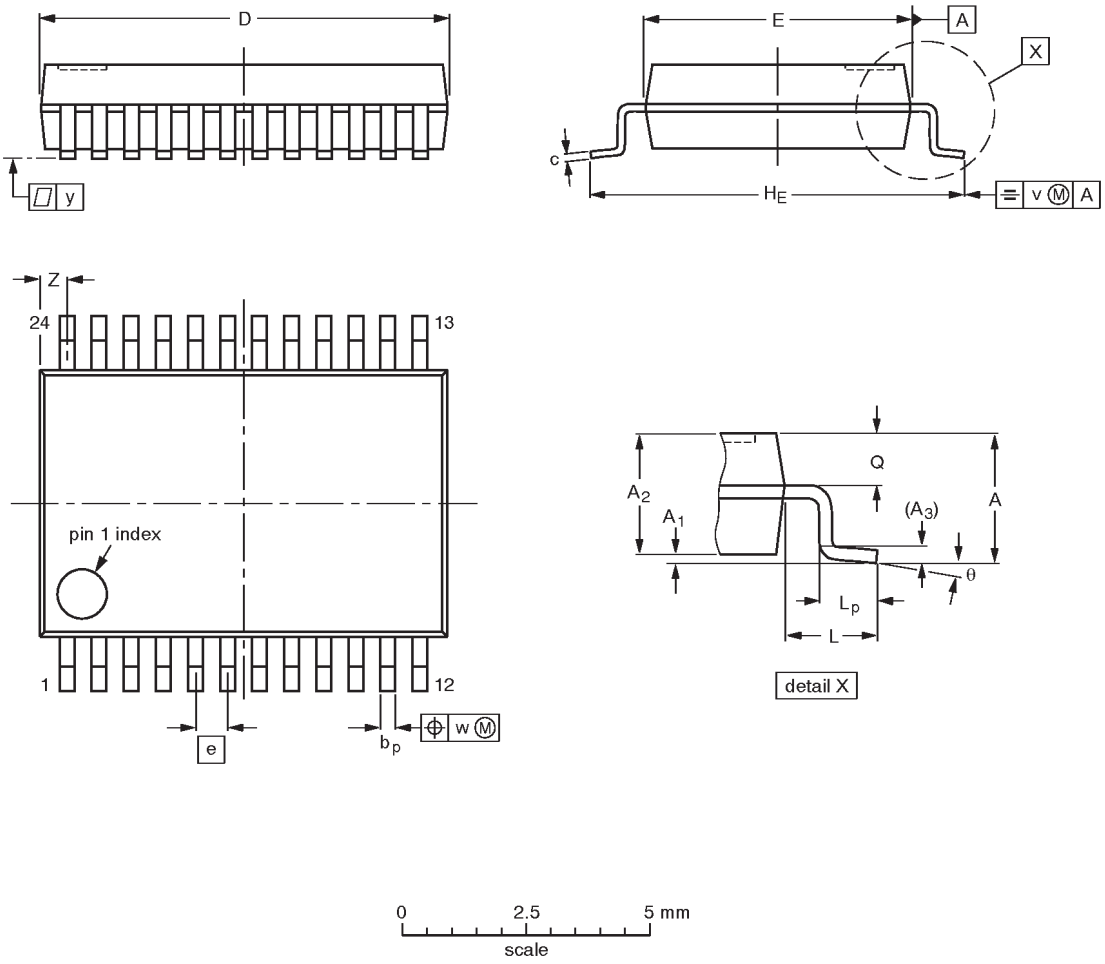
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

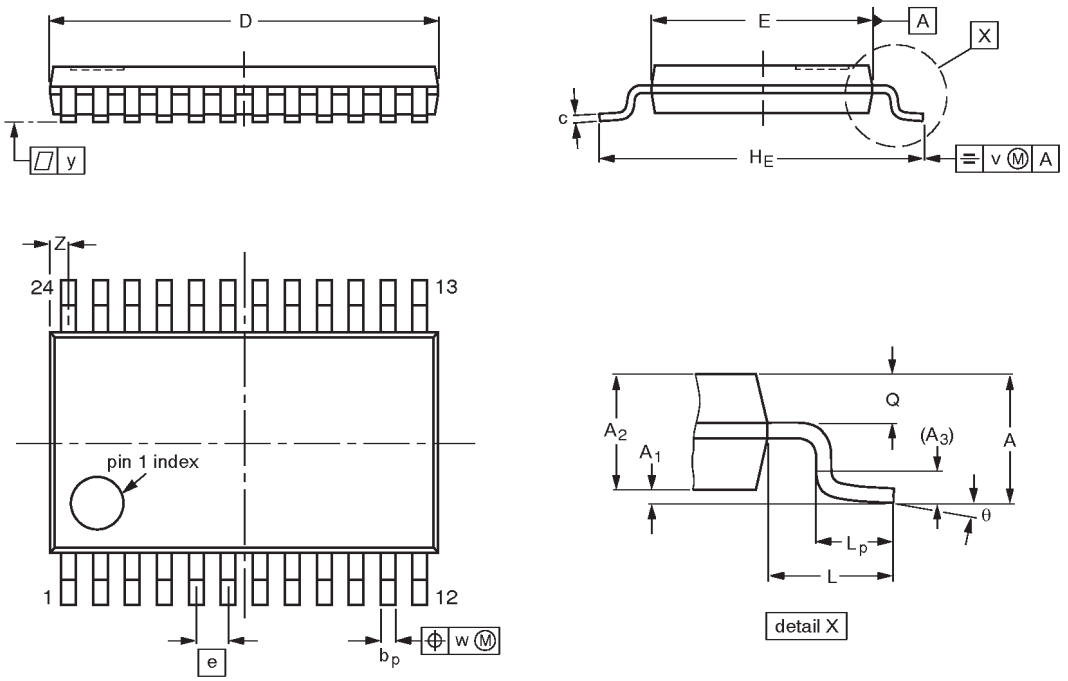
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

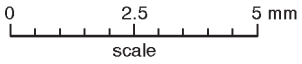
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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