74LVC544A

Octal D-type registered transceiver; inverting; 3-state

Rev. 03 — 11 May 2004 Product data sheet

1. General description

The 74LVC544A is a high-performance, low-power, low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74LVC544A is an octal registered inverting transceiver containing two sets of D-type latches for temporary storage of the data flow in either direction. Separate latch enable inputs ($\overline{LEAB}$ and $\overline{LEBA}$) and output enable inputs ($\overline{OEAB}$ and $\overline{OEBA}$) are provided for each register to permit independent control of inputting and outputting in either direction of the data flow.

The 74LVC544A contains eight D-type latches, with separate inputs and controls for each set. For data flow from pins A to B, for example, the A to B enable input (pin $\overline{EAB}$) must be LOW in order to enter data from pins A0 to A7 or take data from pins B0 to B7. With pin $\overline{EAB}$ LOW, a LOW signal on the A to B latch enable input (pin $\overline{LEAB}$) makes the A to B latches transparent; a subsequent LOW-to-HIGH transition on pin $\overline{LEAB}$ puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With pins $\overline{EAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

2. Features

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B/JESD36
- CMOS low-power consumption
- Direct interface with TTL levels
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Supports partial power-down applications; inputs/outputs are high-impedance when V_{CC} = 0 V
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

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3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay $\overline{An}$ to $\overline{Bn}$; $\overline{Bn}$ to $\overline{An}$	C_L = 50 pF; V_{CC} = 3.3 V		-	3.6	-	ns
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	4.0	-	pF
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V	[1] [2]				
		outputs enabled		-	16.0	-	pF
		outputs disabled		-	4.0	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC544AD	–40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC544ADB	–40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC544APW	–40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

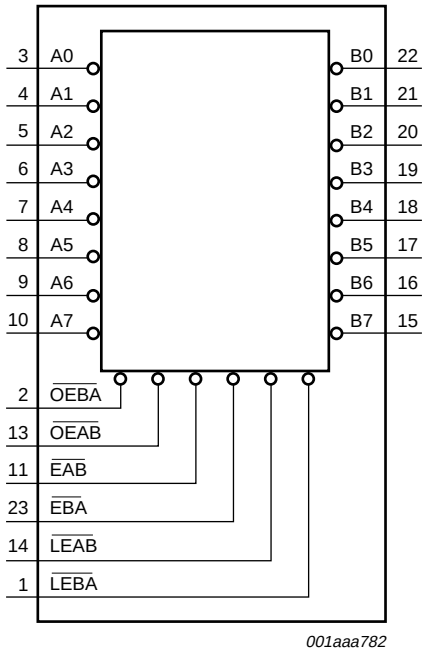


Fig 1. Logic symbol.

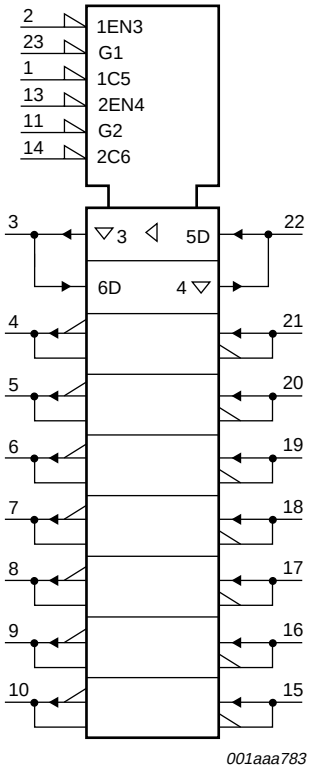


Fig 2. IEC logic symbol.

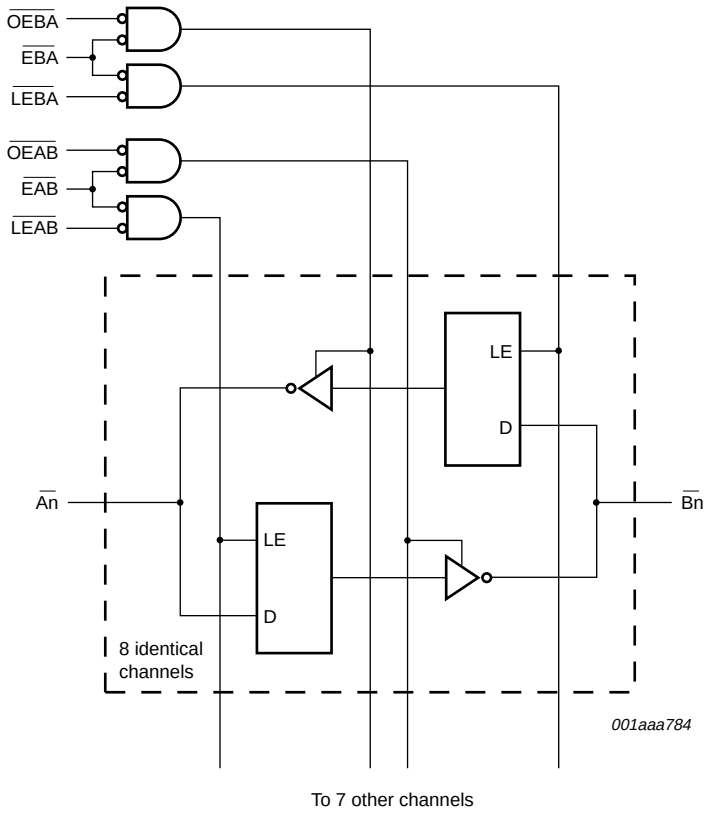


Fig 3. Logic diagram.

6. Pinning information

6.1 Pinning

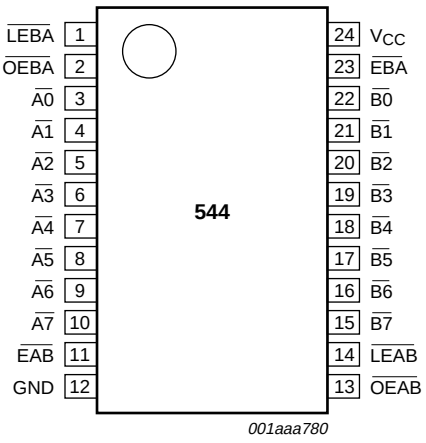


Fig 4. Pin configuration for SO24 and (T)SSOP24.

6.2 Pin description

Table 3: Pin description

Pin	Symbol	Description
1	$\overline{LEBA}$	B to A latch enable input (active LOW)
2	$\overline{OEBA}$	B to A output enable input (active LOW)
3	$\overline{A0}$	A data input or output
4	$\overline{A1}$	A data input or output
5	$\overline{A2}$	A data input or output
6	$\overline{A3}$	A data input or output
7	$\overline{A4}$	A data input or output
8	$\overline{A5}$	A data input or output
9	$\overline{A6}$	A data input or output
10	$\overline{A7}$	A data input or output
11	$\overline{EAB}$	A to B enable input (active LOW)
12	GND	ground (0 V)
13	$\overline{OEAB}$	A to B output enable input (active LOW)
14	$\overline{LEAB}$	A to B latch enable input (active LOW)
15	$\overline{B7}$	B data output or input
16	$\overline{B6}$	B data output or input
17	$\overline{B5}$	B data output or input
18	$\overline{B4}$	B data output or input
19	$\overline{B3}$	B data output or input
20	$\overline{B2}$	B data output or input
21	$\overline{B1}$	B data output or input
22	$\overline{B0}$	B data output or input
23	$\overline{EBA}$	B to A enable input (active LOW)
24	V_{CC}	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Input				Output
	$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	data	
Disabled	H	X	X	X	Z
	X	H	X	X	Z
Disabled plus latch	L	↑	L	h	Z
	L	↑	L	l	Z
Latch plus display	L	L	↑	h	L
	L	L	↑	l	H

Table 4: Function table [1]

Operating mode	Input				Output
	$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	data	
Transparent	L	L	L	H	L
	L	L	L	L	H
Hold (do nothing)	L	L	H	X	NC

[1] XX = AB for A to B direction and BA for B to A direction;
H = HIGH voltage level;
L = LOW voltage level;
h = HIGH state must be present one set-up time before the LOW-TO-HIGH transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ and $\overline{EBA}$;
l = LOW state must be present one set-up time before the LOW-TO-HIGH transition of $\overline{LEAB}$, $\overline{LEBA}$, $\overline{EAB}$ and $\overline{EBA}$;
X = don't care;
↑ = LOW-TO-HIGH level transition;
NC = no change;
Z = high-impedance OFF-state.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	output HIGH or LOW state	[1]	–0.5	V_{CC} + 0.5	V
		output 3-state	[1]	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For T(SSOP)24 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V

Table 6: Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	operating ambient temperature	in free air	–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	[2]	V_{CC} – 0.2	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V		V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V		V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V		V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	[2]	-	GND	0.2	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	-	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; V_{CC} = 3.6 V		-	±0.1	±5	µA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; V_{CC} = 3.6 V	[3]	-	0.1	±10	µA
I_{off}	power-off leakage current	V_I or V_O = 5.5 V; V_{CC} = 0 V		-	0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{CC} = 3.6 V; I_O = 0 A		-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	V_I = V_{CC} – 0.6 V; V_{CC} = 2.7 V to 3.6 V; I_O = 0 A	[2]	-	5	500	µA
C_I	input capacitance			-	5.0	-	pF
$C_{I/O}$	input/output capacitance			-	4.0	-	pF
T_{amb} = –40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V		V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V		-	-	0	V
		V_{CC} = 2.7 V to 3.6 V		-	-	0.8	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = -100$ µA; $V_{CC} = 2.7$ V to 3.6 V		$V_{CC} - 0.3$	-	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V		$V_{CC} - 0.65$	-	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V		$V_{CC} - 0.75$	-	-	V
		$I_O = -24$ mA; $V_{CC} = 3.0$ V		$V_{CC} - 1$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		$I_O = 100$ µA; $V_{CC} = 2.7$ V to 3.6 V		-	-	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V		-	-	0.6	V
		$I_O = 24$ mA; $V_{CC} = 3.0$ V		-	-	0.8	V
I_{LI}	input leakage current	$V_I = 5.5$ V or GND; $V_{CC} = 3.6$ V		-	-	±20	µA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; $V_O = 5.5$ V or GND; $V_{CC} = 3.6$ V	[3]	-	-	±20	µA
I_{off}	power-off leakage current	V_I or $V_O = 5.5$ V; $V_{CC} = 0$ V		-	-	±20	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{CC} = 3.6$ V; $I_O = 0$ A		-	-	40	µA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC} - 0.6$ V; $V_{CC} = 2.7$ V to 3.6 V; $I_O = 0$ A		-	-	5000	µA

[1] All typical values are measured $T_{amb} = 25$ °C.

[2] These typical values are measured at $V_{CC} = 3.3$ V.

[3] For transceivers, the parameter I_{OZ} includes the input leaking current.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; see Figure 9 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay $\overline{An}$ to $\overline{Bn}$; $\overline{Bn}$ to $\overline{An}$	see Figure 5					
		$V_{CC} = 1.2$ V		-	17	-	ns
		$V_{CC} = 2.7$ V		1.5	-	7.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2]	1.0	3.6	6.5	ns
	propagation delay $\overline{LEBA}$ to $\overline{An}$; $\overline{LEAB}$ to $\overline{Bn}$	see Figure 6					
		$V_{CC} = 1.2$ V		-	19	-	ns
		$V_{CC} = 2.7$ V		1.5	-	8.5	ns
		$V_{CC} = 3.0$ V to 3.6 V	[2]	1.0	3.3	7.5	ns

Table 8: Dynamic characteristics *...continued*

GND = 0 V; see Figure 9 for test circuit.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OEBA}$ to $\overline{An}$; $\overline{OEAB}$ to $\overline{Bn}$	see Figure 8					
		V_{CC} = 1.2 V		-	18	-	ns
		V_{CC} = 2.7 V		1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.4	8.5	ns
	3-state output enable time $\overline{EBA}$ to $\overline{An}$; $\overline{EAB}$ to $\overline{Bn}$	see Figure 8					
		V_{CC} = 1.2 V		-	20	-	ns
		V_{CC} = 2.7 V		1.5	-	9.9	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.7	8.9	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OEBA}$ to $\overline{An}$; $\overline{OEAB}$ to $\overline{Bn}$	see Figure 8					
		V_{CC} = 1.2 V		-	8.0	-	ns
		V_{CC} = 2.7 V		1.5	-	7.5	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.5	6.5	ns
	3-state output disable time $\overline{EBA}$ to $\overline{An}$; $\overline{EAB}$ to $\overline{Bn}$	see Figure 8					
		V_{CC} = 1.2 V		-	9.0	-	ns
		V_{CC} = 2.7 V		1.5	-	7.9	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	3.6	6.9	ns
t_W	$\overline{LEXX}$ pulse with LOW	see Figure 6					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		2.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.0	0.9	-	ns
t_{su}	set-up time $\overline{An}$, $\overline{Bn}$ to $\overline{LEXX}$; $\overline{An}$, $\overline{Bn}$ to $\overline{EXX}$	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		2.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.0	–0.5	-	ns
t_h	hold time $\overline{An}$, $\overline{Bn}$ to $\overline{LEXX}$; $\overline{An}$, $\overline{Bn}$ to $\overline{EXX}$	see Figure 7					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3.0	1.5	-	ns
$t_{sk(0)}$	skew		[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per latch	V_{CC} = 3.3 V	[4] [5]				
		outputs enabled		-	16.0	-	pF
		outputs disabled		-	4.0	-	pF

Table 8: Dynamic characteristics *...continued*

GND = 0 V; see Figure 9 for test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay $\overline{A}_n$ to $\overline{B}_n$; $\overline{B}_n$ to $\overline{A}_n$	see Figure 5				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	8.5	ns
	propagation delay $\overline{LE}_{BA}$ to $\overline{A}_n$; $\overline{LE}_{AB}$ to $\overline{B}_n$	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	11.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	9.5	ns
t_{PZH}, t_{PZL}	3-state output enable time $\overline{OEBA}$ to $\overline{An}$; $\overline{OEAB}$ to $\overline{Bn}$	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	12.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	11.0	ns
	3-state output enable time $\overline{EBA}$ to $\overline{An}$; $\overline{EAB}$ to $\overline{Bn}$	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	12.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	11.5	ns
t_{PHZ}, t_{PLZ}	3-state output disable time $\overline{OEBA}$ to $\overline{An}$; $\overline{OEAB}$ to $\overline{Bn}$	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	9.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	8.5	ns
	3-state output disable time $\overline{EBA}$ to $\overline{An}$; $\overline{EAB}$ to $\overline{Bn}$	see Figure 8				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.5	-	10.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	9.0	ns
t_W	$\overline{LEXX}$ pulse with LOW	see Figure 6				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	2.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	ns
t_{su}	set-up time $\overline{An}$, $\overline{Bn}$ to $\overline{LEXX}$; $\overline{An}$, $\overline{Bn}$ to $\overline{EXX}$	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	2.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	ns
t_h	hold time $\overline{An}$, $\overline{Bn}$ to $\overline{LEXX}$; $\overline{An}$, $\overline{Bn}$ to $\overline{EXX}$	see Figure 7				
		V_{CC} = 1.2 V	-	-	-	ns
		V_{CC} = 2.7 V	1.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	3.0	-	-	ns
$t_{sk(0)}$	skew	[3]	-	-	1.5	ns

[1] All typical values are measured T_{amb} = 25 °C.

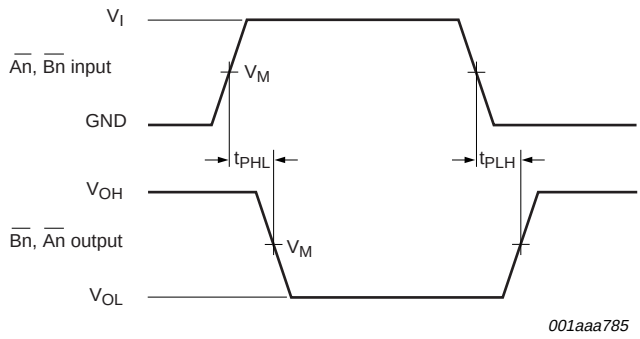
[2] These typical values are measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

12. Waveforms



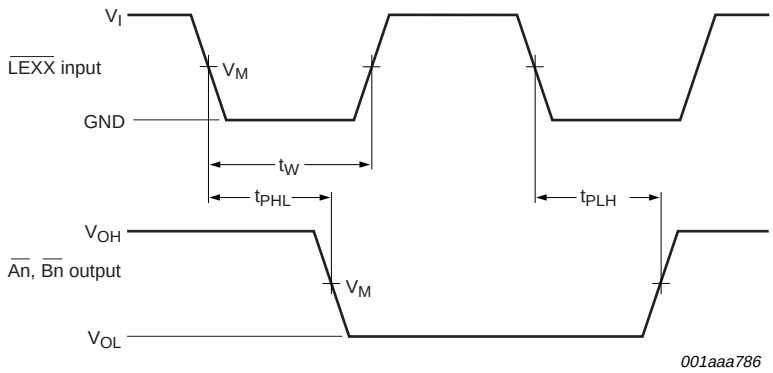
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 5. Input ($\overline{An}$, $\overline{Bn}$) to output ($\overline{Bn}$, $\overline{An}$) propagation delays.

Table 9: Measurement points

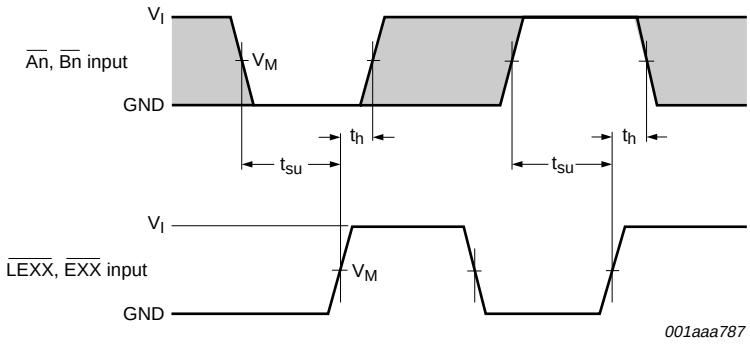
Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

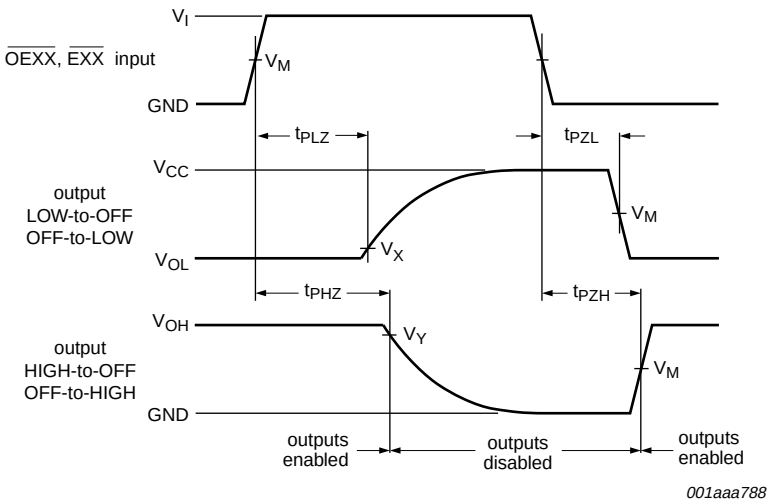
Fig 6. Latch enable input ($\overline{LEXX}$) pulse width and latch enable input to output ($\overline{An}$, $\overline{Bn}$) propagation delays.



Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance

Fig 7. Data set-up and hold times for the inputs ($\overline{An}$, $\overline{Bn}$) to $\overline{LEXX}$ and $\overline{EXX}$ inputs.



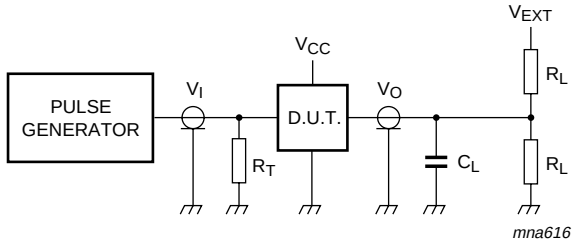
Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 8. 3-state enable and disable times.

Table 10: Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.1 V	V_{OH} − 0.1 V
2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V
3.0 V to 3.6 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

Fig 9. Load circuitry for switching times.

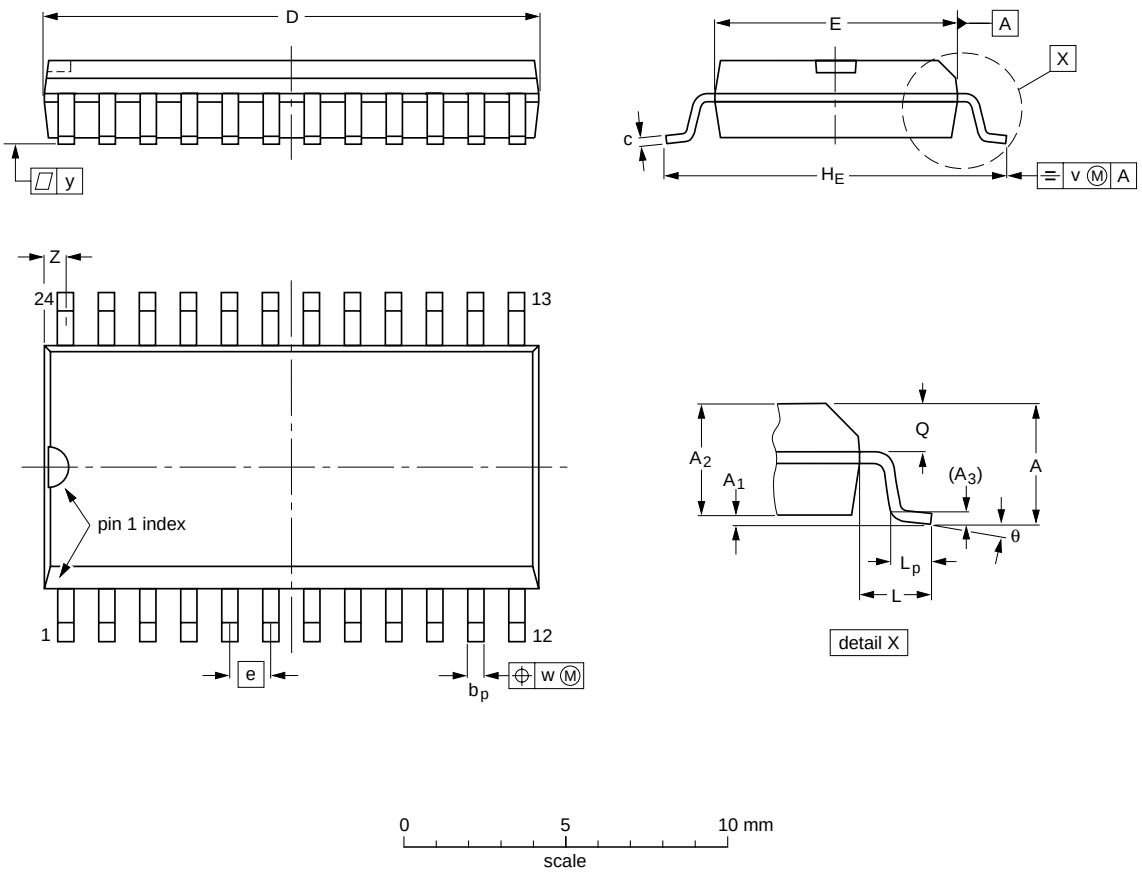
Table 11: Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when R_L = 1000 Ω.

13. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

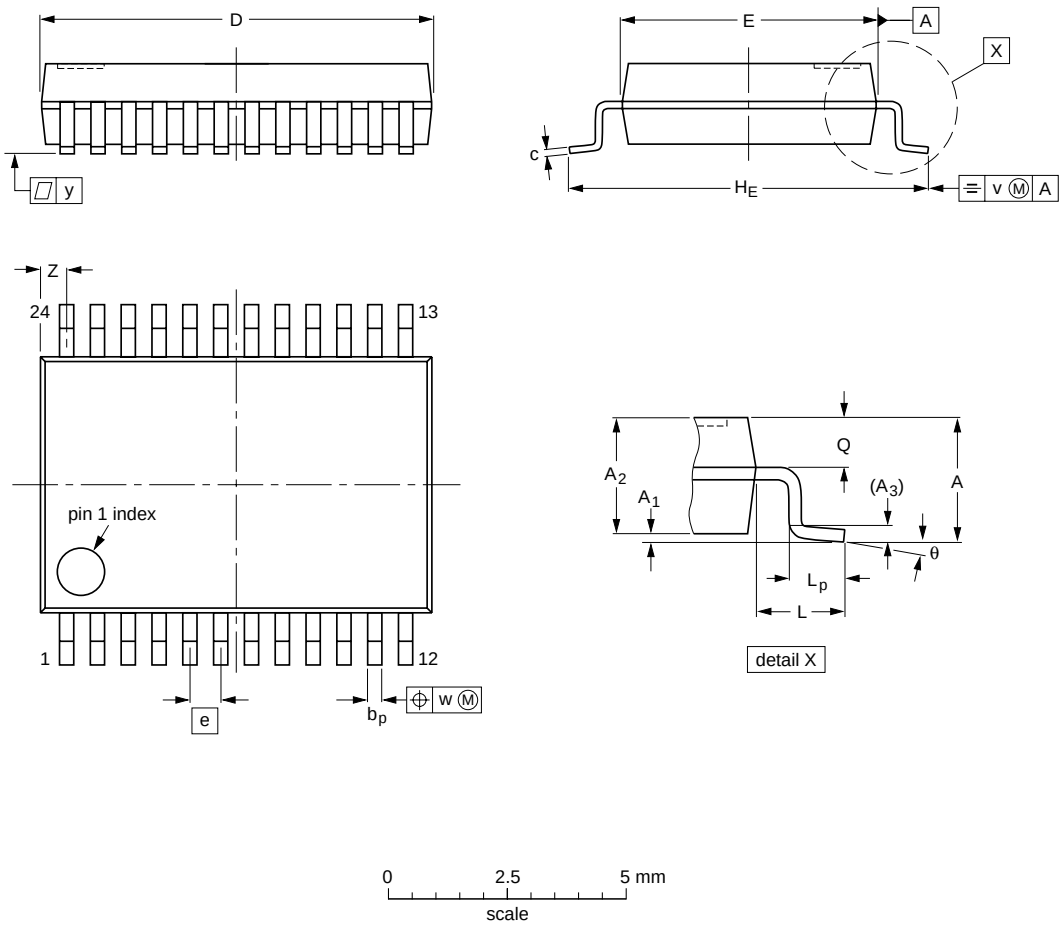
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SO24.

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

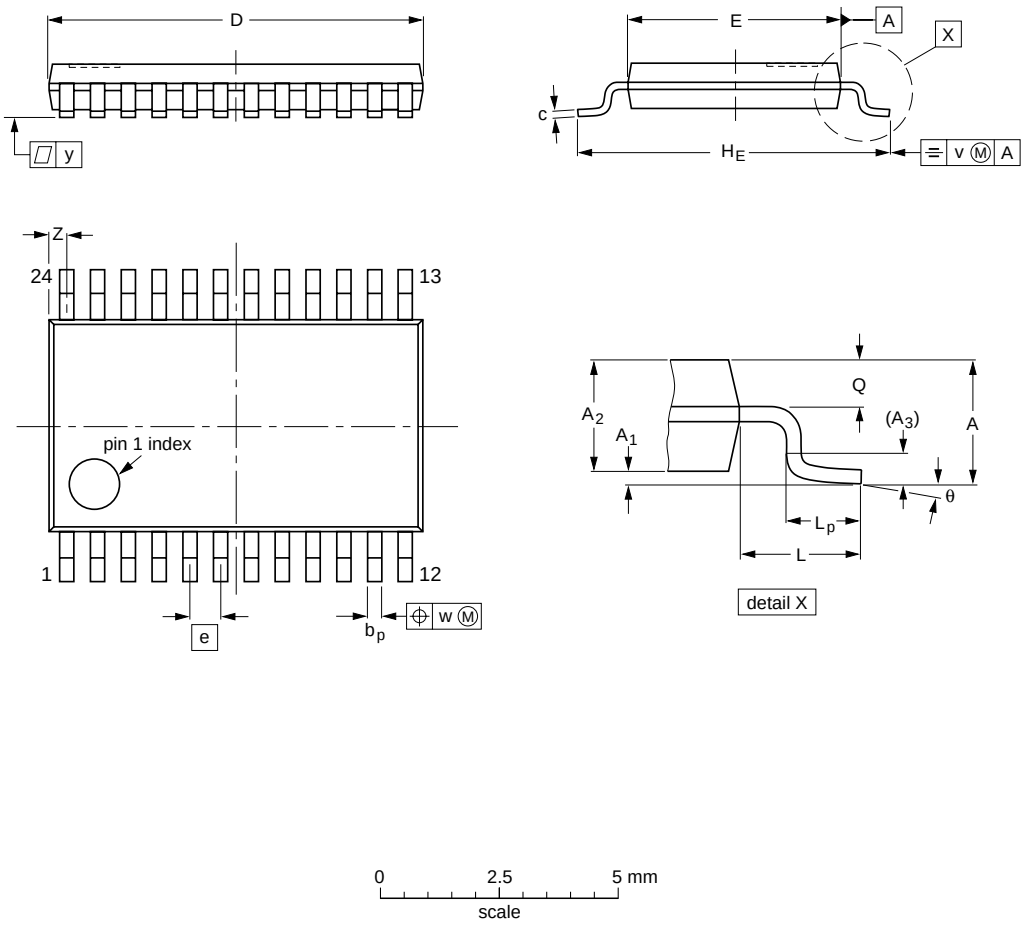
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SSOP24.

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline TSSOP24.

14. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74LVC544A_3	20040511	Product data	-	9397 750 13127	74LVC544A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors • Table 1: updated various values • Table 7: changed various values • Table 7: added values for T_{amb} = –40 °C to +125 °C • Table 8: changed various values • Table 8: added values for T_{amb} = –40 °C to +125 °C.				
74LVC544A_2	19980729	Product specification	-	9397 750 04512	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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19. Contents

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