DATA SHEET

74LVCH162374A

16-bit edge triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

Product specification
Supersedes data of 2004 Mar 25

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Philips Semiconductors

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16-bit edge triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

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FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bushold
- High-impedance outputs when V_{CC} = 0 V
- Complies with JEDEC standard JESD8-B/JESD36
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVCH162374A is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. The 74LVCH162374A consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74LVCH162374A bushold data inputs eliminates the need for external pull-up resistors to hold unused inputs.

The 74LVCH162374A is designed with 30 Ω series termination resistors in both high and low output stages to reduce line noise.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.7	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.4	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nQn	C_L = 50 pF; V_{CC} = 3.3 V	3.1	ns
f_{max}	maximum clock frequency		330	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per flip-flop	V_{CC} = 3.3 V; notes 1 and 2		pF
		outputs enabled	13.5	pF
		outputs disabled	10	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

OPERATION MODES	INPUT			INTERNAL FLIP-FLOP	OUTPUT
	$n\overline{OE}$	nCP	nD0 to nD7		nQ0 to nQ7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Latch register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   Z = high-impedance OFF-state;
   ↑ = LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVCH162374ADGG	–40 °C to +125 °C	48	TSSOP48	plastic	SOT362-1
74LVCH162374ADL	–40 °C to +125 °C	48	SSOP48	plastic	SOT370-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	$1\overline{OE}$	output enable input (active LOW)
2	1Q0	data output
3	1Q1	data output
4	GND	ground (0 V)
5	1Q2	data output
6	1Q3	data output
7	V_{CC}	supply voltage
8	1Q4	data output
9	1Q5	data output
10	GND	ground (0 V)
11	1Q6	data output
12	1Q7	data output
13	2Q0	data output
14	2Q1	data output
15	GND	ground (0 V)
16	2Q2	data output
17	2Q3	data output
18	V_{CC}	supply voltage
19	2Q4	data output
20	2Q5	data output
21	GND	ground (0 V)
22	2Q6	data output
23	2Q7	data output
24	$2\overline{OE}$	output enable input (active LOW)
25	2CP	clock input
26	2D7	data input
27	2D6	data input
28	GND	ground (0 V)
29	2D5	data input
30	2D4	data input
31	V_{CC}	supply voltage
32	2D3	data input
33	2D2	data input
34	GND	ground (0 V)
35	2D1	data input
36	2D0	data input
37	1D7	data input
38	1D6	data input
39	GND	ground (0 V)
40	1D5	data input
41	1D4	data input
42	V_{CC}	supply voltage
43	1D3	data input
44	1D2	data input
45	GND	ground (0 V)
46	1D1	data input
47	1D0	data input
48	1CP	clock input

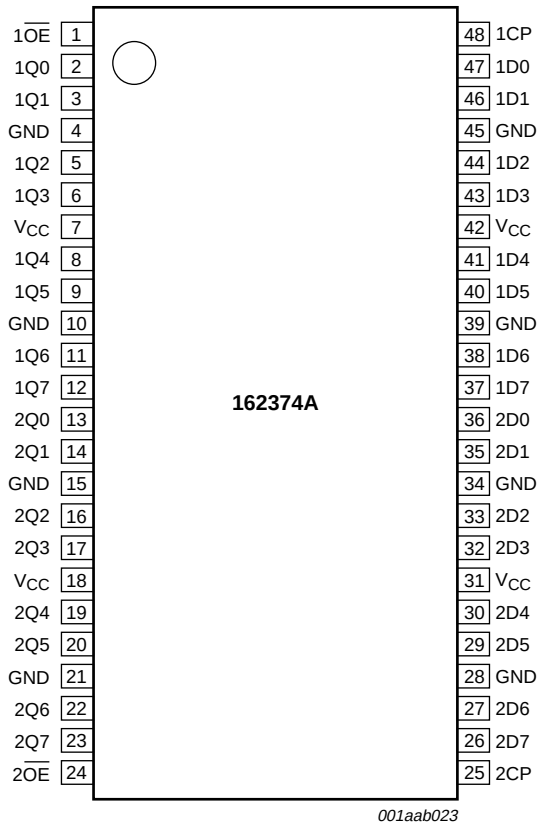


Fig.1 Pin configuration SSOP48 and TSSOP48.

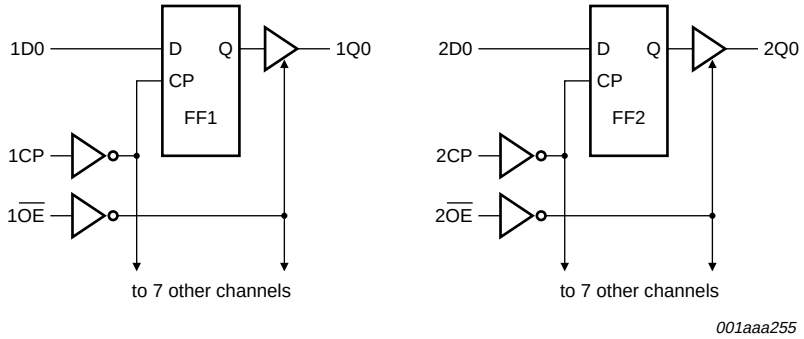


Fig.2 Logic diagram.

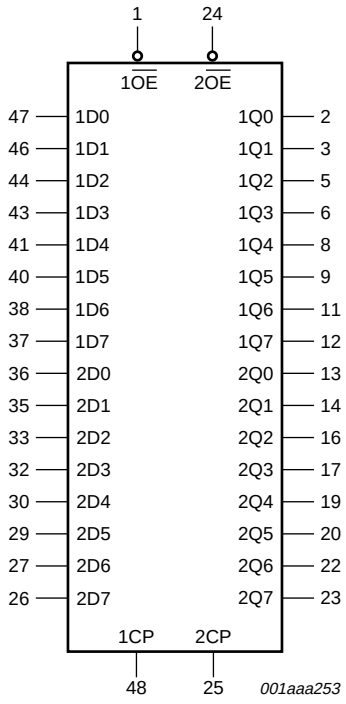


Fig.3 Logic symbol.

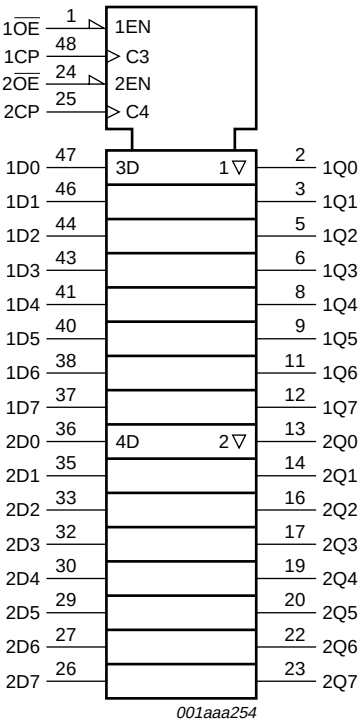


Fig.4 Logic symbol (IEEE/IEC).

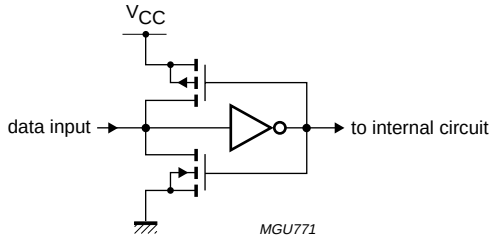


Fig.5 Bushold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	5.5	V
T_{amb}	operating ambient temperature	in free air	−40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		−0.5	+6.5	V
I_{IK}	input diode current	V_I < 0 V	−	−50	mA
V_I	input voltage	note 1	−0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	−	±50	mA
V_O	output voltage	output HIGH or LOW state; note 1	−0.5	V_{CC} + 0.5	V
		output 3-state; note 1	−0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	−	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		−	±100	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	power dissipation	T_{amb} = −40 °C to +125 °C; note 2	−	500	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –6 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –100 μA	3.0	V_{CC} – 0.2	V_{CC}	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 6 mA	2.7	–	–	0.40	V
		I_O = 100 μA	3.0	–	GND	0.20	V
		I_O = 12 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 2	3.6	–	±0.1	±5	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	20	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0 A	2.7 to 3.6	–	5	500	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 3 and 4	3.0	75	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 3 and 4	3.0	–75	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 3 and 5	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 3 and 5	3.6	–500	–	–	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –6 mA	2.7	V_{CC} – 0.5	–	–	V
		I_O = –100 μA	3.0	V_{CC} – 0.2	–	–	V
		I_O = –12 mA	3.0	V_{CC} – 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 6 mA	2.7	–	–	0.40	V
		I_O = 100 μA	3.0	–	–	0.20	V
		I_O = 12 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND; note 2	3.6	–	–	±20	μA
I_{OZ}	3-state output OFF-state current	V_I = V_{IH} or V_{IL}; V_O = 5.5 V or GND; note 2	3.6	–	–	±20	μA
I_{off}	power-off leakage supply current	V_I or V_O = 5.5 V	0.0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	–	80	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} – 0.6 V; I_O = 0 A	2.7 to 3.6	–	–	5000	μA
I_{BHL}	bushold LOW sustaining current	V_I = 0.8 V; notes 3 and 4	3.0	60	–	–	μA
I_{BHH}	bushold HIGH sustaining current	V_I = 2.0 V; notes 3 and 4	3.0	–60	–	–	μA
I_{BHLO}	bushold LOW overdrive current	notes 3 and 5	3.6	500	–	–	μA
I_{BHHO}	bushold HIGH overdrive current	notes 3 and 5	3.6	–500	–	–	μA

Notes

1. All typical values are measured at T_{amb} = 25 °C.
2. The bushold circuit is switched off when $V_I > V_{CC}$ allowing 5.5 V on the input pin.
3. For data inputs only, control inputs do not have a bushold circuit.
4. The specified sustaining current at the data inputs do not have a bushold circuit.
5. The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

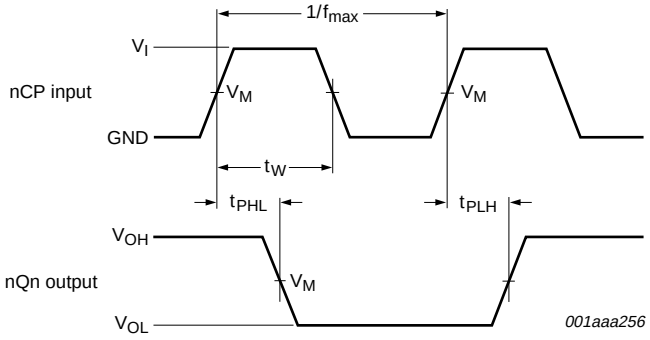
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note1							
t_{PHL}/t_{PLH}	propagation delay nCP to nQn	see Figs. 6 and 9	1.2	–	14	–	ns
			2.7	1.5	–	7.8	ns
			3.0 to 3.6	1.5	3.7(2)	6.8	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nQn	see Figs. 8 and 9	1.2	–	20	–	ns
			2.7	1.5	–	8.3	ns
			3.0 to 3.6	1.5	3.4(2)	6.6	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nQn	see Figs. 8 and 9	1.2	–	12	–	ns
			2.7	1.5	–	4.6	ns
			3.0 to 3.6	1.5	3.1(2)	4.4	ns
t_W	nCP pulse width HIGH	see Fig.6	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	1.5(2)	–	ns
t_{su}	set-up time nDn to nCP	see Fig.7	1.2	–	–	–	ns
			2.7	1.9	–	–	ns
			3.0 to 3.6	1.9	0.3(2)	–	ns
t_h	hold time nDn to nCP	see Fig.7	1.2	–	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	–0.3(2)	–	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns
f_{max}	maximum clock pulse frequency	see Fig.6	2.7	150	–	–	MHz
			3.0 to 3.6	150	330(2)	–	MHz

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nCP to nQn	see Figs. 6 and 9	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.5	–	8.5	ns
t_{PZH}/t_{PZL}	3-state output enable time n$\overline{OE}$ to nQn	see Figs. 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	10.5	ns
			3.0 to 3.6	1.5	–	8.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time n$\overline{OE}$ to nQn	see Figs. 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.5	–	5.5	ns
t_W	nCP pulse width HIGH	see Fig.6	1.2	–	–	–	ns
			2.7	3.0	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
t_{su}	set-up time nDn to nCP	see Fig.7	1.2	–	–	–	ns
			2.7	1.9	–	–	ns
			3.0 to 3.6	1.9	–	–	ns
t_h	hold time nDn to nCP	see Fig.7	1.2	–	–	–	ns
			2.7	1.5	–	–	ns
			3.0 to 3.6	1.5	–	–	ns
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns
f_{max}	maximum clock pulse frequency	see Fig.6	2.7	150	–	–	MHz
			3.0 to 3.6	150	–	–	MHz

Notes

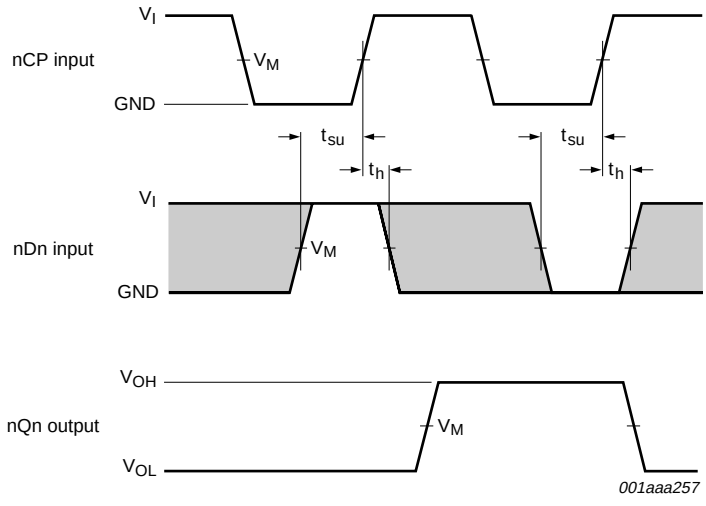
1. All typical values are measured at T_{amb} = 25 °C.
2. These typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

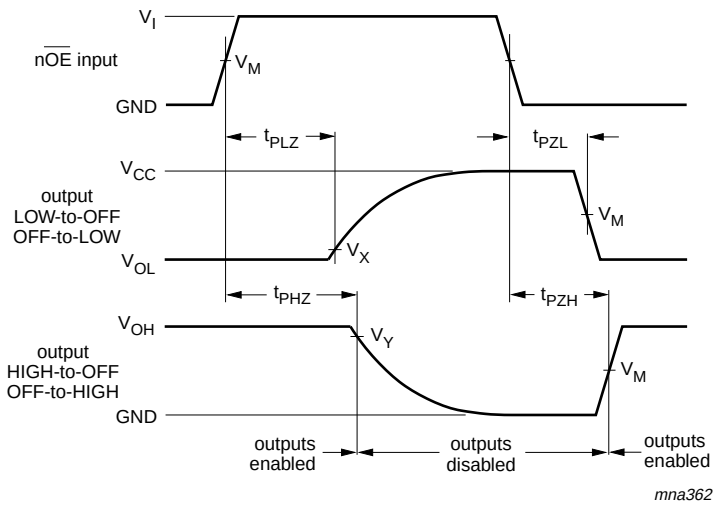
Fig.6 Clock input (nCP) to output (nQn) propagation delay, the clock pulse width and the maximum clock pulse frequency.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

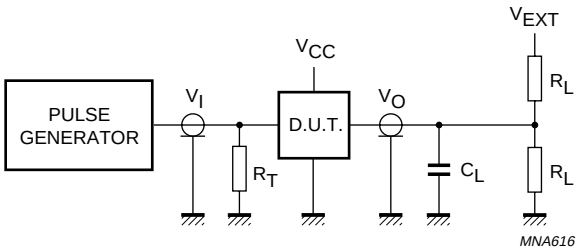
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.7 Data set-up and hold times for the nDn input to the nCP input.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V;
$V_M = 0.5 \times V_{CC}$ at V_{CC} < 2.7 V;
$V_X = V_{OL}$ + 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_X = V_{OL}$ + 0.1 V at V_{CC} < 2.7 V;
$V_Y = V_{OH}$ − 0.3 V at $V_{CC} \geq$ 2.7 V;
$V_Y = V_{OH}$ − 0.1 V at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.8 3-state enable and disable times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω(1)	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuit:

R_L = Load resistor.

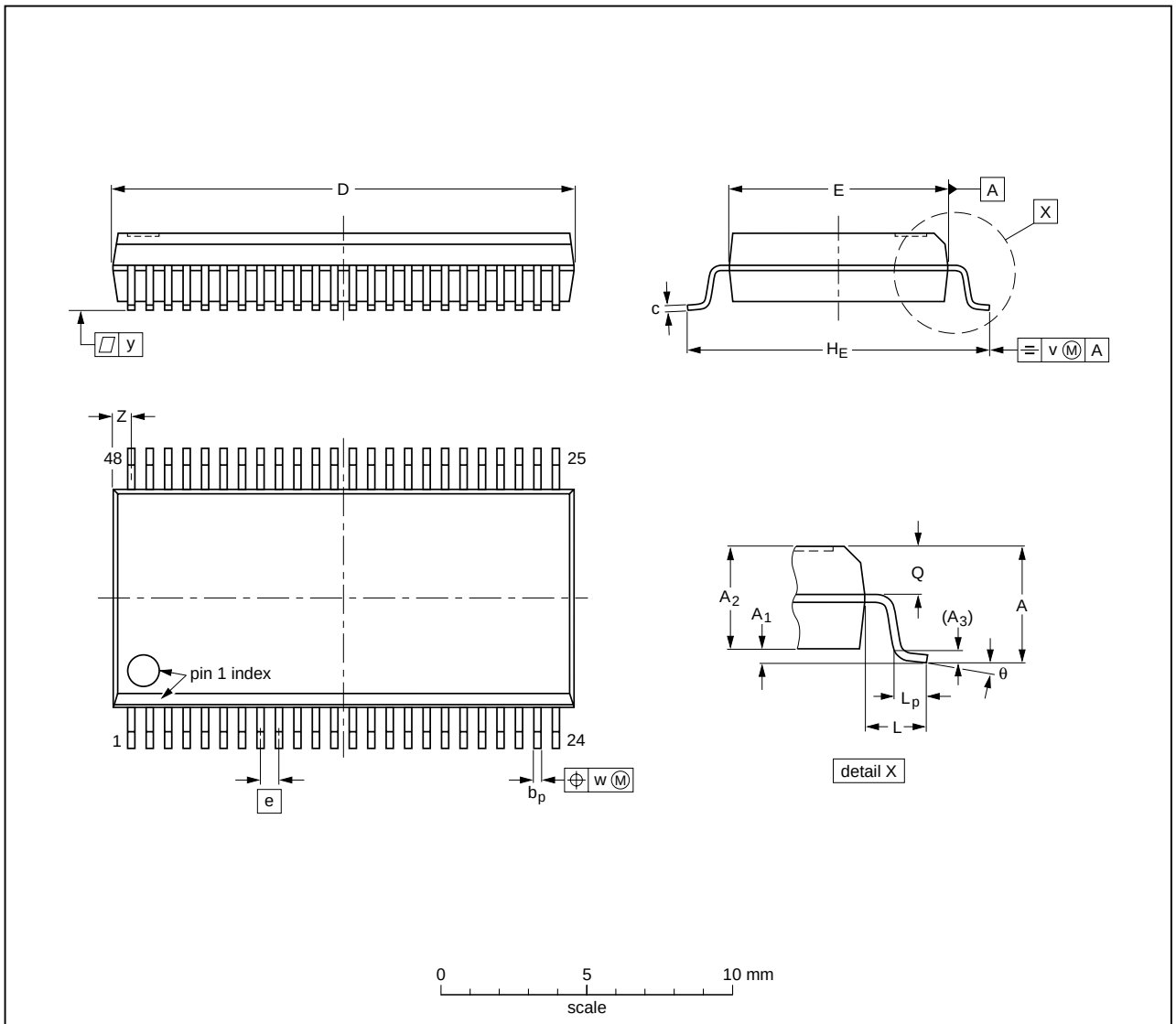
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

PACKAGE OUTLINES

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

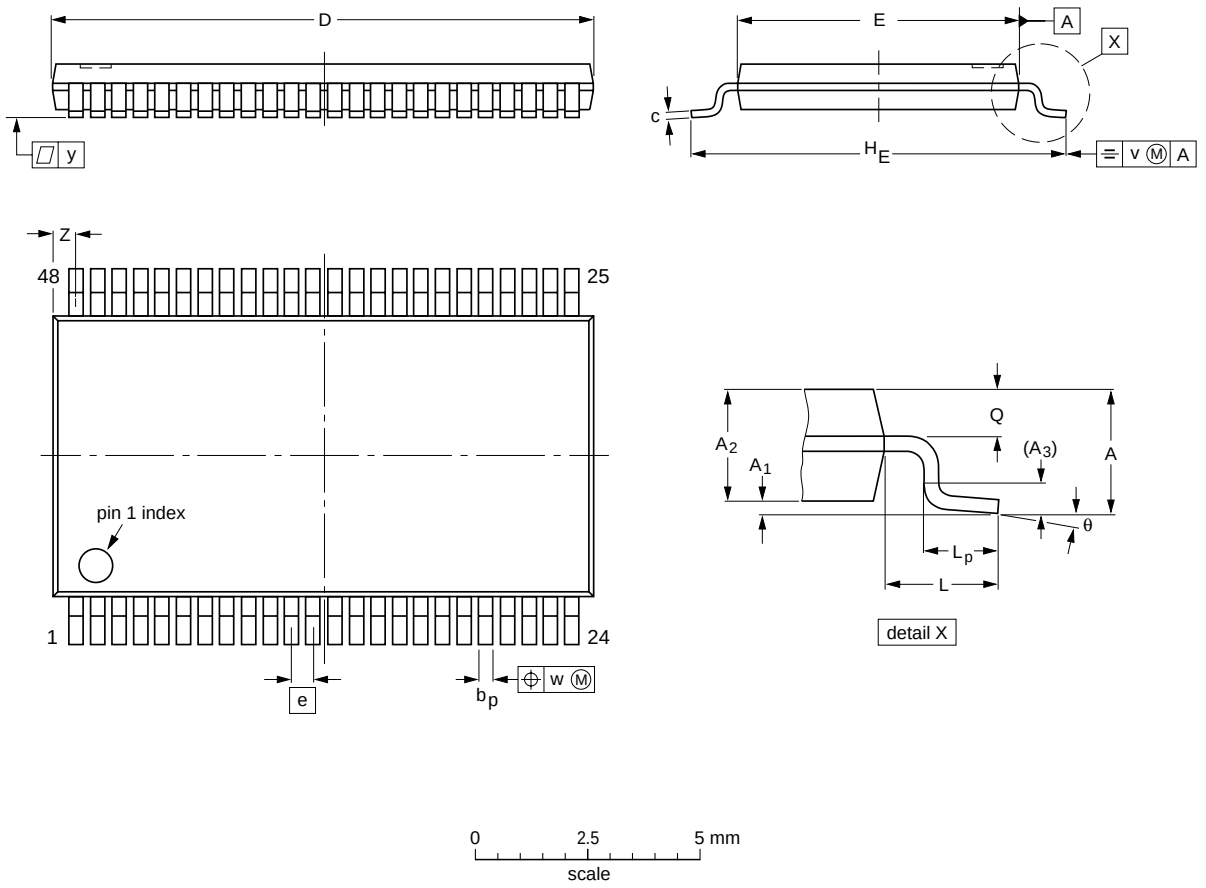
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	**0.2** **0.1**	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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