

# DATA SHEET

## **74LVC257A**

Quad 2-input multiplexer with 5 V  
tolerant inputs/outputs; 3-state

Product specification  
Supersedes data of 2003 Nov 17

2004 Jan 23

## Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

## 74LVC257A

### FEATURES

- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 to +85 °C and –40 to +125 °C.

### DESCRIPTION

The 74LVC257A is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5.0 V devices. In 3-state operation, outputs can handle 5 V. This feature allows the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC257A is a quad 2-input multiplexer with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (pin S). The data inputs from source 0 (pins 1I0 to 4I0) are selected when pin S is LOW and the data inputs from source 1 (pins 1I1 to 4I1) are selected when pin S is HIGH. Data appears at the outputs (pins 1Y to 4Y) in true (non-inverting) form from the selected inputs. The 74LVC257A is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to pin S. The outputs are forced to a high-impedance OFF-state when pin  $\overline{OE}$  is HIGH.

### QUICK REFERENCE DATA

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $T_{amb} = 25$  °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nI0, nI1 to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.9	ns
	propagation delay S to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.2	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}$ to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.7	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}$ to nY	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.2	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2 outputs enabled	16	pF
		outputs disabled	7.0	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

# Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

**FUNCTION TABLE**

See note 1.

INPUT				OUTPUT
$\overline{\text{OE}}$	S	nI0	nI1	nY
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

**Note**

- H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

**ORDERING INFORMATION**

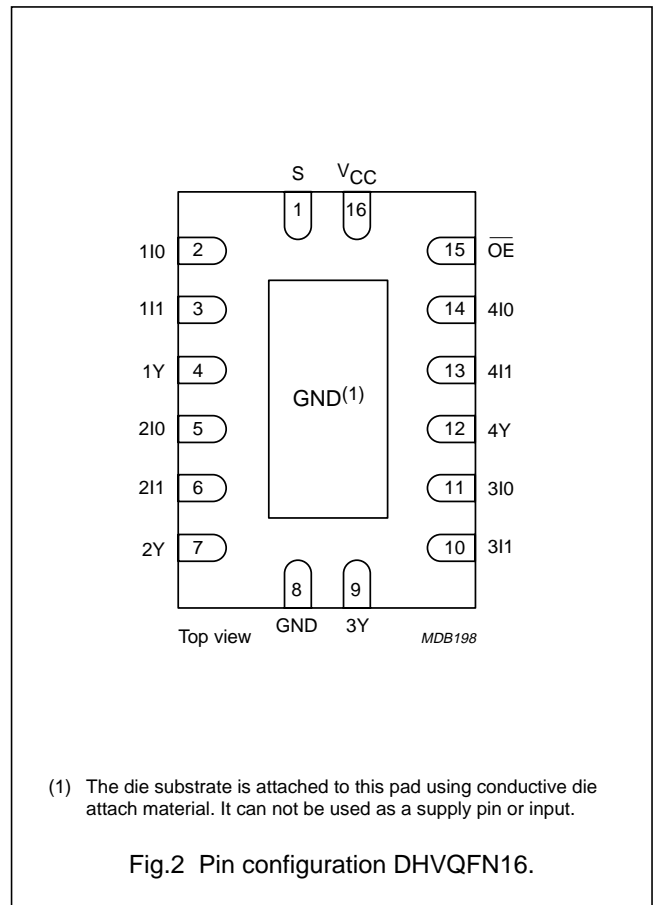
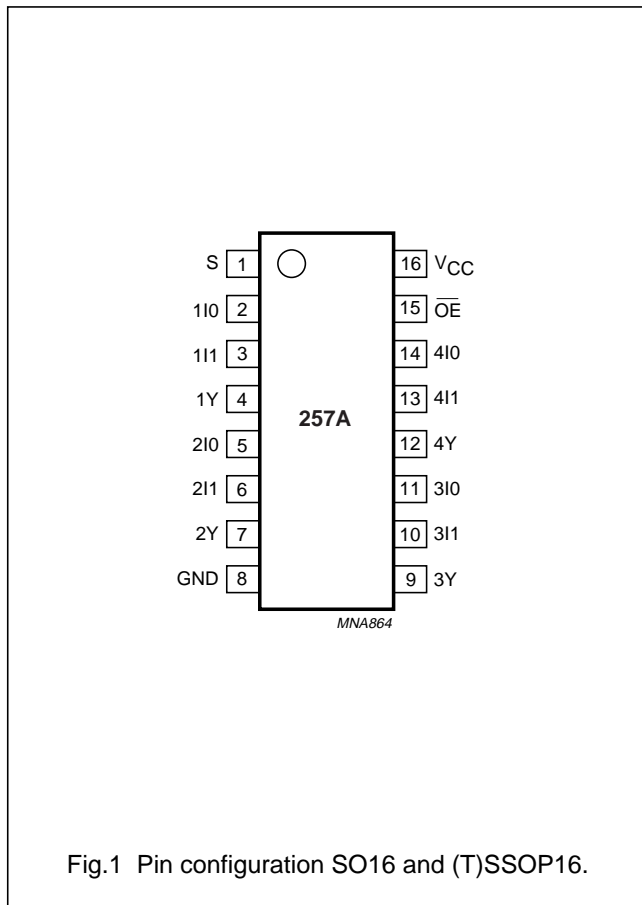
TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC257AD	-40 to +125 °C	16	SO16	plastic	SOT109-1
74LVC257ADB	-40 to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC257APW	-40 to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC257ABQ	-40 to +125 °C	16	DHVQFN16	plastic	SOT763-1

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

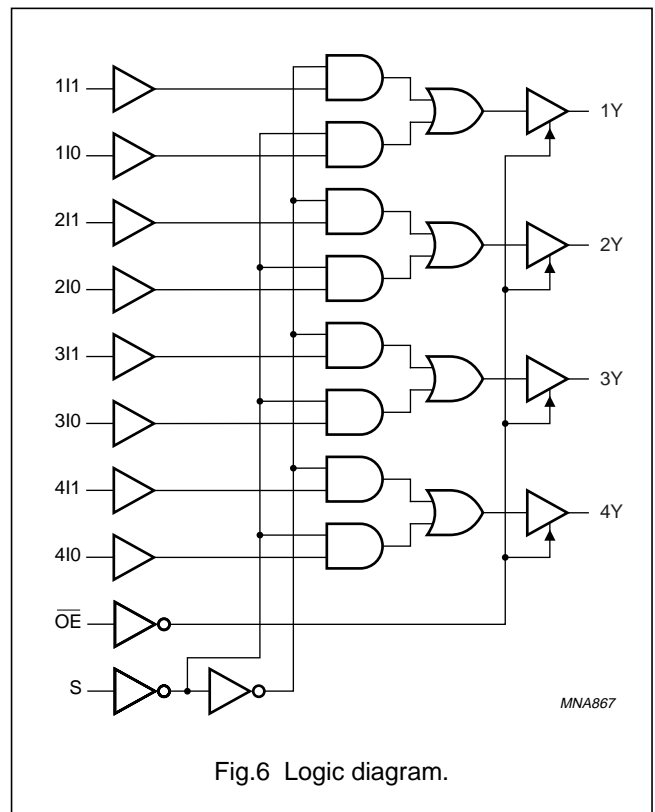
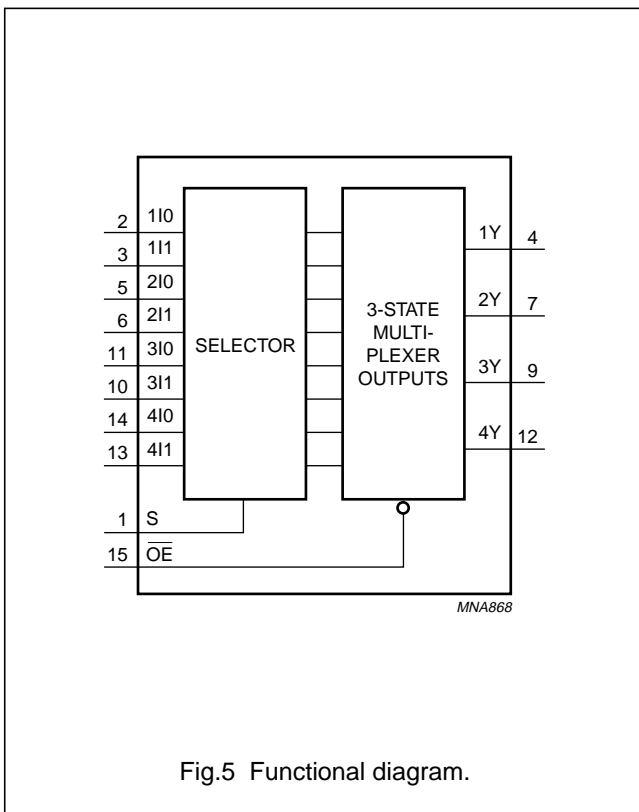
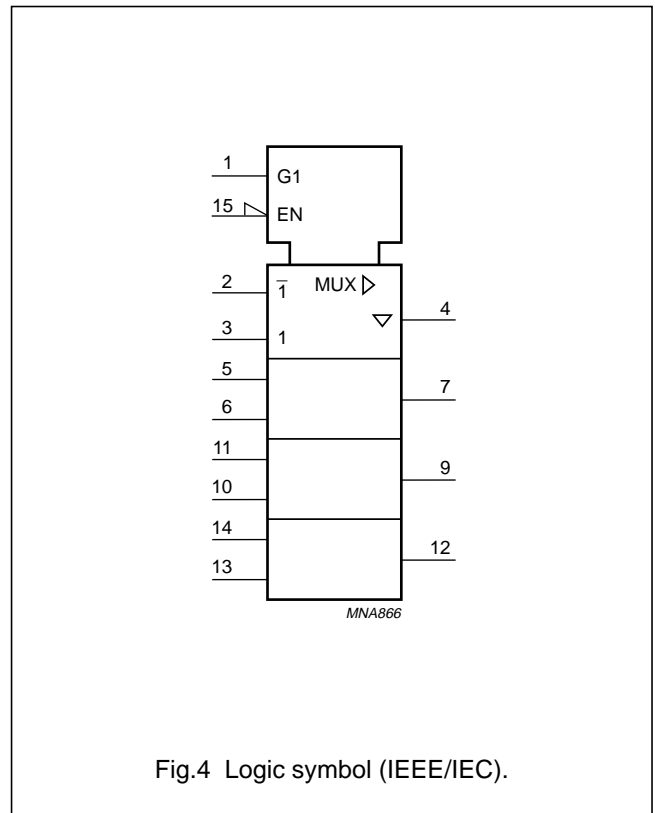
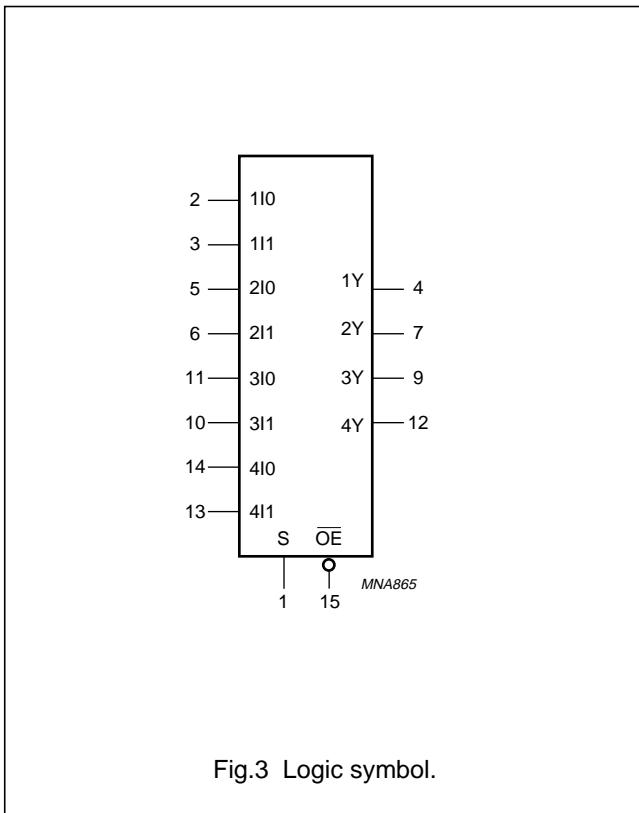
PINNING

PIN	SYMBOL	DESCRIPTION
1	S	common data select input
2	1I0	data input from source 0
3	1I1	data input from source 1
4	1Y	3-state multiplexer output
5	2I0	data input from source 0
6	2I1	data input from source 1
7	2Y	3-state multiplexer output
8	GND	ground (0 V)
9	3Y	3-state multiplexer output
10	3I1	data input from source 1
11	3I0	data input from source 0
12	4Y	3-state multiplexer output
13	4I1	data input from source 1
14	4I0	data input from source 0
15	$\overline{OE}$	3-state output enable input (active LOW)
16	V <sub>CC</sub>	supply voltage



Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A



# Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	HIGH or LOW state	0	V <sub>CC</sub>	V
		3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

## Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO16 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

# Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub> <sup>(2)</sup>	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	–	–	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.6	–	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA	2.7 to 3.6	–	GND <sup>(2)</sup>	0.2	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	–	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	–	0.1	±5	µA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	5 <sup>(2)</sup>	500	µA

Quad 2-input multiplexer with 5 V  
tolerant inputs/outputs; 3-state

74LVC257A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	0	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	2.7 to 3.6	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	2.7 to 3.6	-	-	0.3	V
		I <sub>O</sub> = 12 mA	2.7	-	-	0.6	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	-	±20	μA
I <sub>off</sub>	power-off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	μA

**Notes**

1. All typical values are measured T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V.



# Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nI0, nI1 to nY	see Figs 7 and 9	1.2	–	16	–	ns
			2.7	1.0	3.0	5.4	ns
			3.0 to 3.6	1.0	2.9 <sup>(2)</sup>	4.6	ns
	propagation delay S to nY	see Figs 7 and 9	1.2	–	18	–	ns
			2.7	1.0	3.6	7.5	ns
			3.0 to 3.6	1.0	3.2 <sup>(2)</sup>	6.4	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to nY	see Figs 8 and 9	1.2	–	15	–	ns
			2.7	1.5	3.6	6.7	ns
			3.0 to 3.6	1.0	3.7 <sup>(2)</sup>	5.6	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to nY	see Figs 8 and 9	1.2	–	8	–	ns
			2.7	1.5	3.1	4.7	ns
			3.0 to 3.6	1.0	3.2 <sup>(2)</sup>	4.3	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nI0, nI1 to nY	see Figs 7 and 9	1.2	–	–	–	ns
			2.7	1.0	–	7.0	ns
			3.0 to 3.6	1.0	–	6.0	ns
	propagation delay S to nY	see Figs 7 and 9	1.2	–	–	–	ns
			2.7	1.0	–	9.5	ns
			3.0 to 3.6	1.0	–	8.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.0	–	7.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to nY	see Figs 8 and 9	1.2	–	–	–	ns
			2.7	1.5	–	6.0	ns
			3.0 to 3.6	1.0	–	5.5	ns
t <sub>sk(0)</sub>	skew	note 3	3.0 to 3.6	–	–	1.5	ns

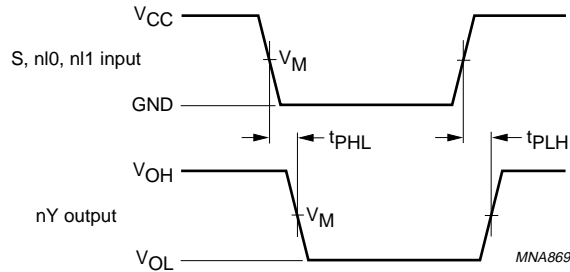
### Notes

1. All typical values are measured T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

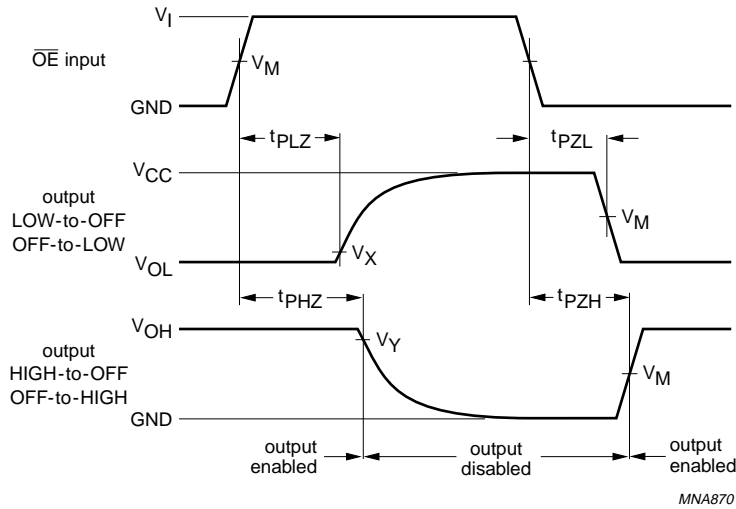
AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 Input (S, nI0 and nI1) to output (nY) propagation delays.



V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

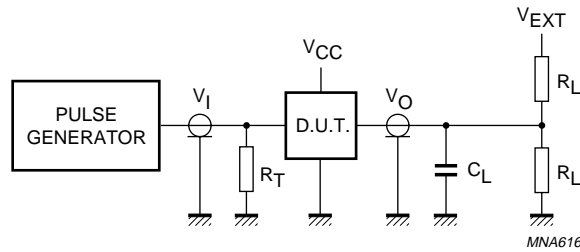
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.1 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.8 3-state enable and disable times.

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A



V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω <sup>(1)</sup>	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

1. The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.9 Load circuitry for switching times.

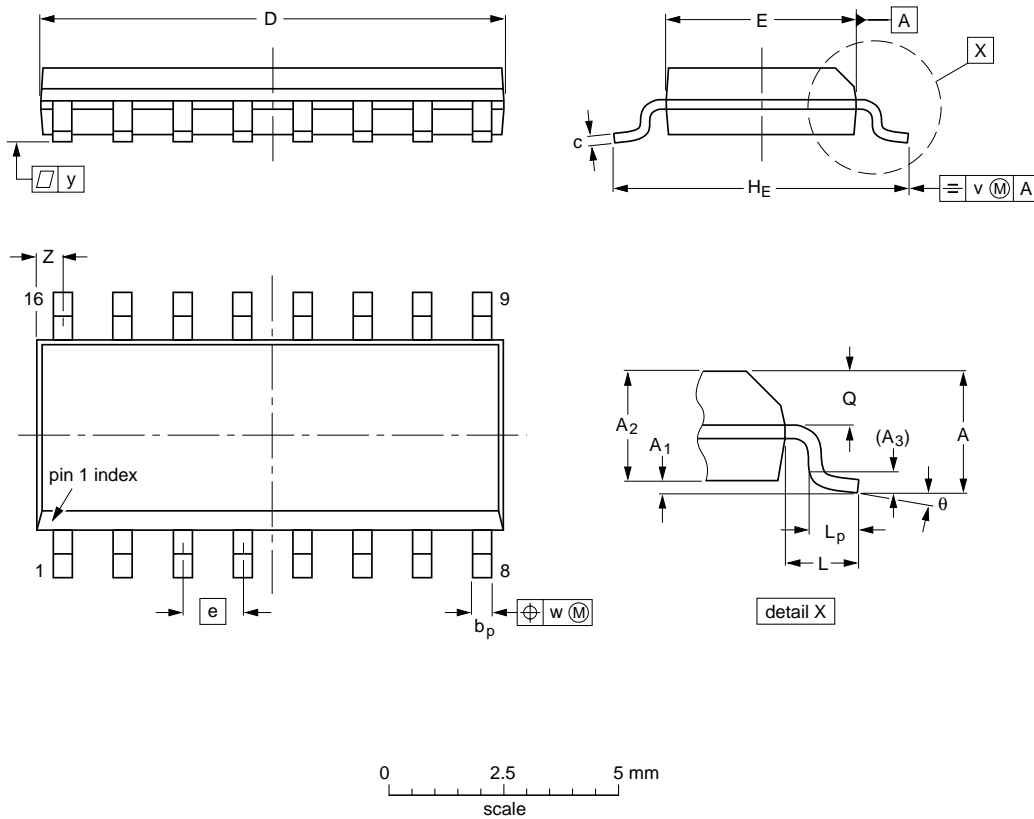
Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

PACKAGE OUTLINES

S016: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

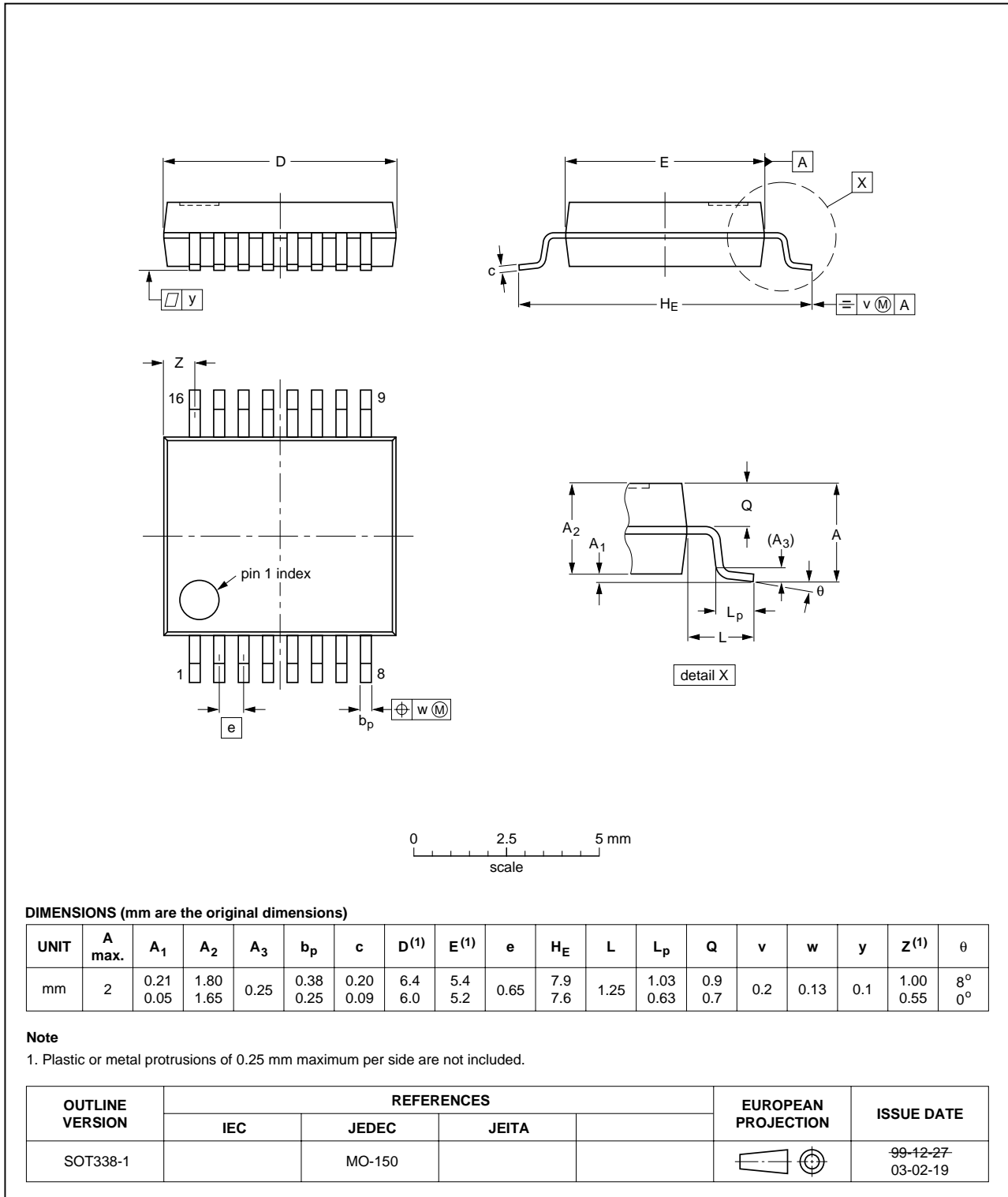
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

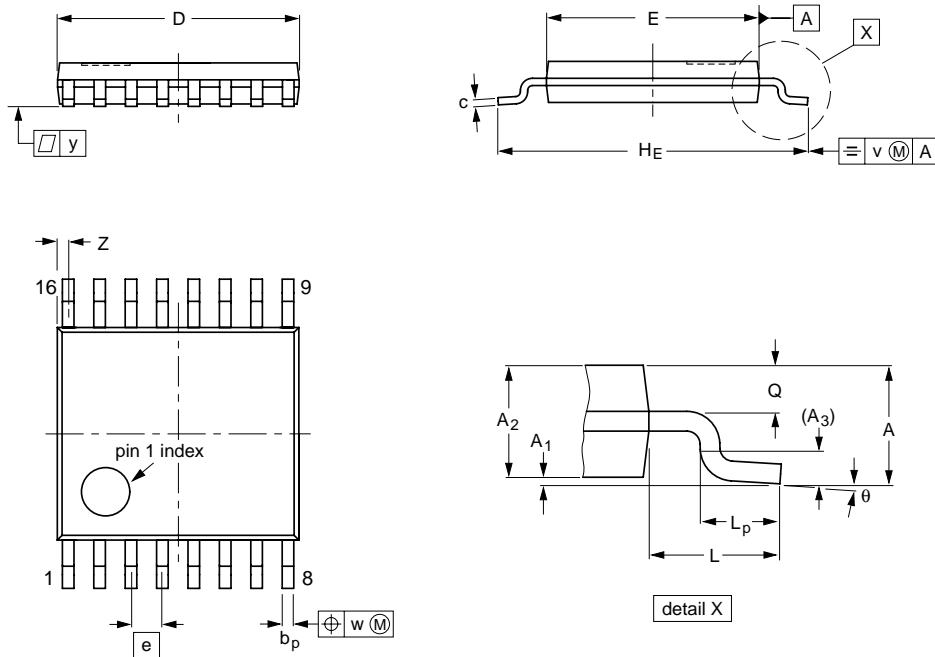


Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

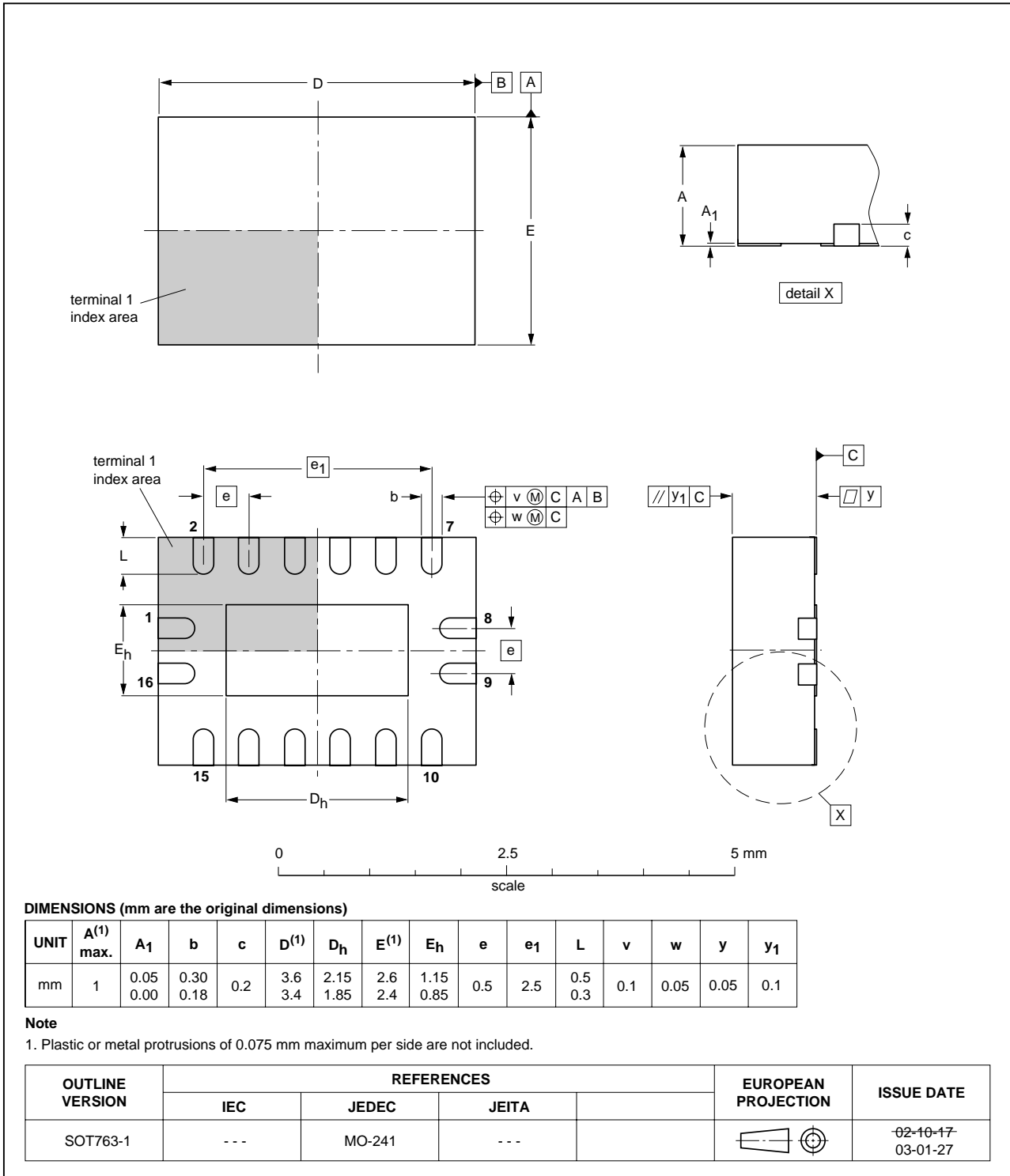
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT403-1		MO-153			99-12-27 03-02-18

Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1



## Quad 2-input multiplexer with 5 V tolerant inputs/outputs; 3-state

74LVC257A

### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

### Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

### DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

### DISCLAIMERS

**Life support applications** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.



# ***Philips Semiconductors – a worldwide company***

## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

© Koninklijke Philips Electronics N.V. 2004

SCA76

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R20/04/pp17

Date of release: 2004 Jan 23

Document order number: 9397 750 12697

*Let's make things better.*

**Philips  
Semiconductors**



**PHILIPS**