

# DATA SHEET

## **74LVC240A**

Octal buffer/line driver with 5 V  
tolerant inputs/outputs; inverting;  
3-state

Product specification  
Supersedes data of 2003 May 14

2003 Dec 02

## Octal buffer/line driver with 5 V tolerant inputs/outputs; inverting; 3-state

## 74LVC240A

### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when  $V_{CC} = 0$  V
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

### DESCRIPTION

The 74LVC240A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC240A is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $1\overline{OE}$  and  $2\overline{OE}$ . A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Schmitt-trigger action at all inputs makes the circuit highly tolerant for slower input rise and fall times.

The 74LVC240A is functionally identical to the 74LVC244A, which has non-inverting outputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay nAn to nYn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.5	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $n\overline{OE}$ to nYn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	4.3	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $n\overline{OE}$ to nYn	$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.7	ns
$C_I$	input capacitance		5.0	pF
$C_{PD}$	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2		
		outputs enabled	10	pF
		outputs disabled	3.0	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

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**FUNCTION TABLE**

See note 1.

INPUT		OUTPUT
$\overline{\text{nOE}}$	nAn	nYn
L	L	H
L	H	L
H	X	Z

**Note**

1. H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC240AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC240ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC240APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC240ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

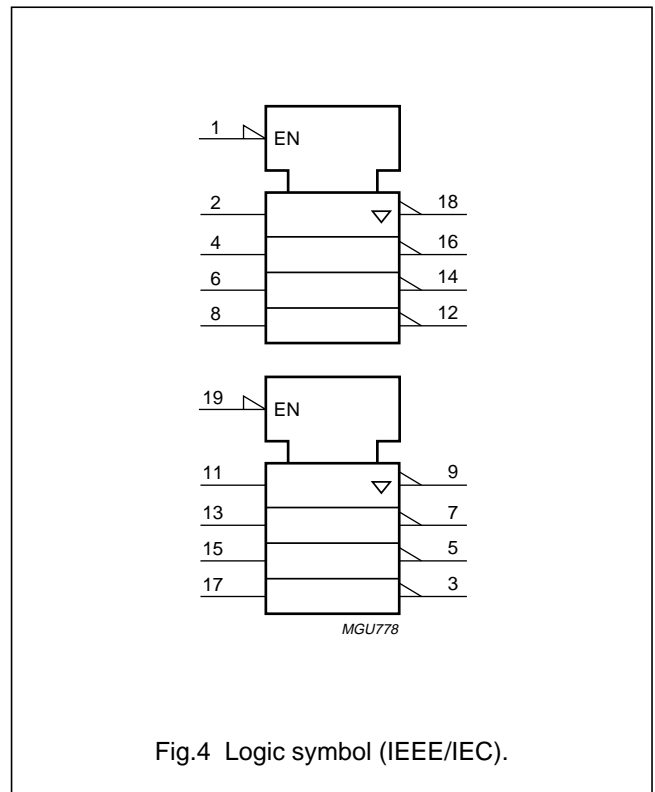
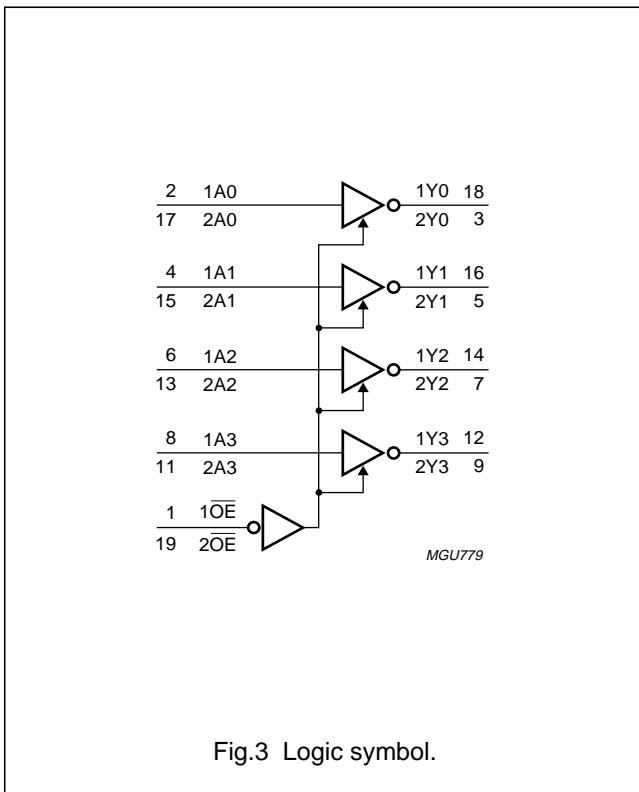
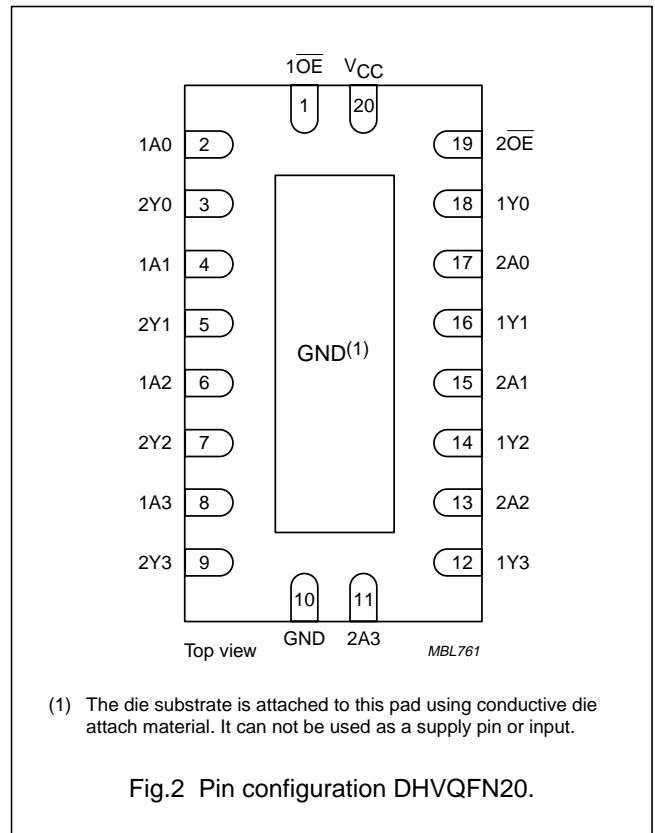
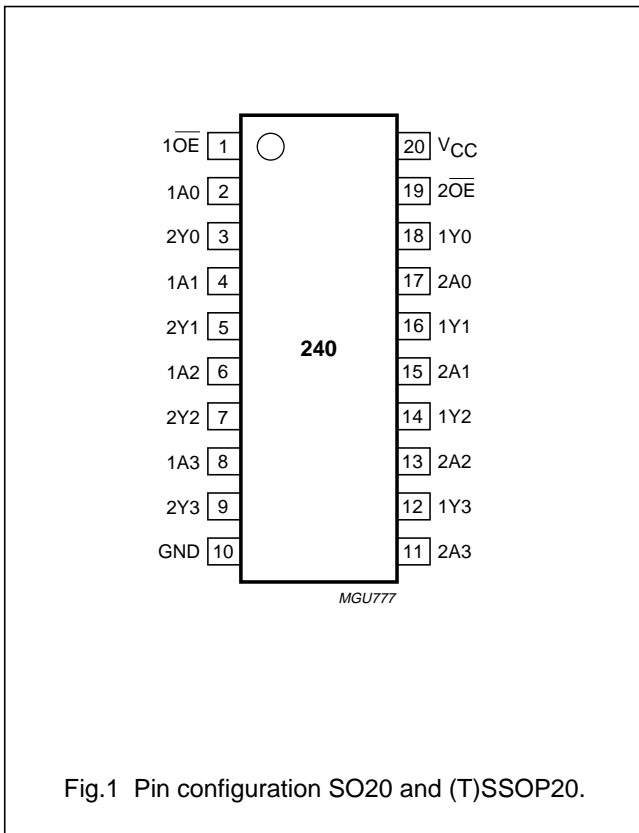
**PINNING**

PIN	SYMBOL	DESCRIPTION
1	$1\overline{\text{OE}}$	output enable input (active LOW)
2	1A0	data input
3	2Y0	data output
4	1A1	data input
5	2Y1	data output
6	1A2	data input
7	2Y2	data output
8	1A3	data input
9	2Y3	data output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	2A3	data input
12	1Y3	data output
13	2A2	data input
14	1Y2	data output
15	2A1	data input
16	1Y1	data output
17	2A0	data input
18	1Y0	data output
19	$2\overline{\text{OE}}$	output enable input (active LOW)
20	V <sub>CC</sub>	power supply

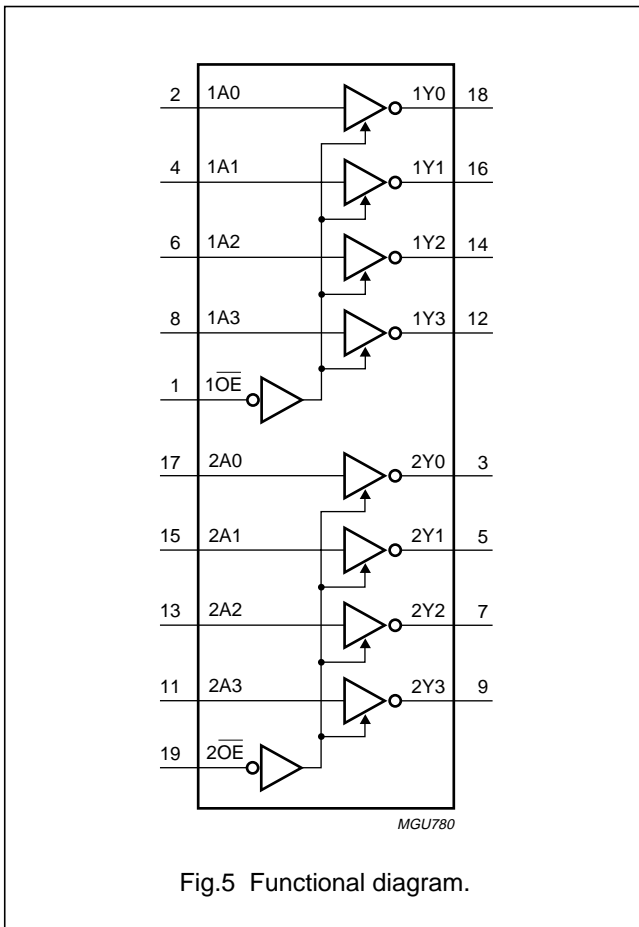
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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state; note 1	-0.5	$V_{CC} + 0.5$	V
		output 3-state; note 1	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	$\pm 100$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	-	500	mW

### Notes

- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	0	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -100 μA	2.7	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.6	-	-	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	0	0.20	V
		I <sub>O</sub> = 100 μA	2.7	-	-	0.40	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	0.1	±10	μA
I <sub>off</sub>	power off leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	0	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -100 µA	2.7	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.75	-	-	V
		I <sub>O</sub> = -18 mA	3.0	V <sub>CC</sub> - 1	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7 to 3.6	-	-	0.3	V
		I <sub>O</sub> = 100 µA	2.7	-	-	0.6	V
		I <sub>O</sub> = 12 mA	3.0	-	-	0.8	V
		I <sub>O</sub> = 24 mA	3.0	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	3.6	-	-	±20	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND	3.6	-	-	±20	µA
I <sub>off</sub>	power-off leakage supply current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	-	±20	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	-	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	-	5000	µA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.



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## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500 \Omega$ .

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C; note 1</b>							
t <sub>PLH</sub> /t <sub>PHL</sub>	propagation delay 1An to 1Yn; 2An to 2Yn	see Figs 6 and 8	1.2	–	16.0	–	ns
			2.7	1.5	–	7.0	ns
			3.0 to 3.6	1.3	3.5 <sup>(2)</sup>	5.5	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time 1OE to 1Yn; 2OE to 2Yn	see Figs 7 and 8	1.2	–	19.0	–	ns
			2.7	1.0	–	8.5	ns
			3.0 to 3.6	1.1	4.3 <sup>(2)</sup>	7.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time 1OE to 1Yn; 2OE to 2Yn	see Figs 7 and 8	1.2	–	17.0	–	ns
			2.7	1.5	–	7.5	ns
			3.0 to 3.6	1.4	3.7 <sup>(2)</sup>	6.0	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PLH</sub> /t <sub>PHL</sub>	propagation delay 1An to 1Yn; 2An to 2Yn	see Figs 6 and 8	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.3	–	7.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time 1OE to 1Yn; 2OE to 2Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.0	–	11.0	ns
			3.0 to 3.6	1.1	–	9.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time 1OE to 1Yn; 2OE to 2Yn	see Figs 7 and 8	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.4	–	7.5	ns
t <sub>sk(0)</sub>	skew	note 3		–	–	1.5	ns

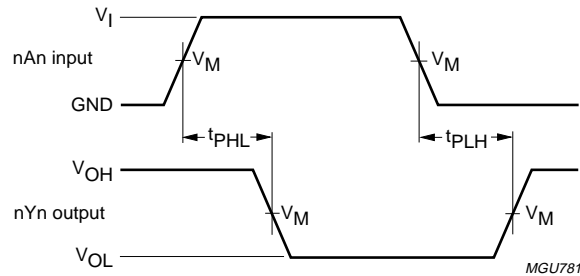
### Notes

1. All typical values are measured at T<sub>amb</sub> = 25 °C.
2. These typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

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AC WAVEFORMS



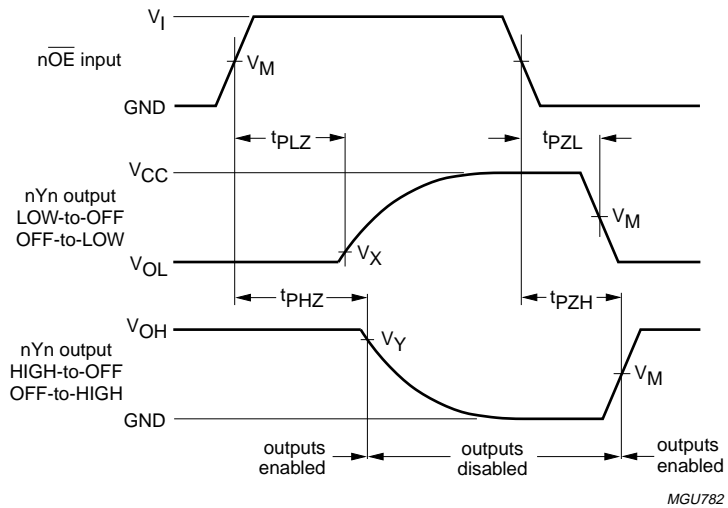
V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 Inputs (1An, 2An) to outputs (1Yn, 2Yn) propagation delays.

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V <sub>CC</sub>	V <sub>M</sub>	INPUT	
		V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.2 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>	≤ 2.5 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns

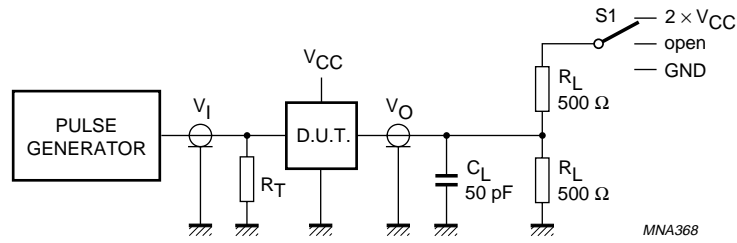
V<sub>X</sub> = V<sub>OL</sub> + 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>X</sub> = V<sub>OL</sub> + 0.1 V at V<sub>CC</sub> < 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.3 V at V<sub>CC</sub> ≥ 2.7 V;  
 V<sub>Y</sub> = V<sub>OH</sub> - 0.1 V at V<sub>CC</sub> < 2.7 V.

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.

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MNA368

V <sub>CC</sub>	V <sub>I</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>EXT</sub>		
				t <sub>PLH</sub> /t <sub>PHL</sub>	t <sub>PZH</sub> /t <sub>PHZ</sub>	t <sub>PZL</sub> /t <sub>PLZ</sub>
1.2 V	V <sub>CC</sub>	50 pF	500 Ω <sup>(1)</sup>	open	GND	2 × V <sub>CC</sub>
2.7 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	2 × V <sub>CC</sub>

**Note**

- The circuit performs better when R<sub>L</sub> = 1000 Ω.

Definitions for test circuits:

R<sub>L</sub> = Load resistor.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to the output impedance Z<sub>o</sub> of the pulse generator.

Fig.8 Load circuitry for switching times.

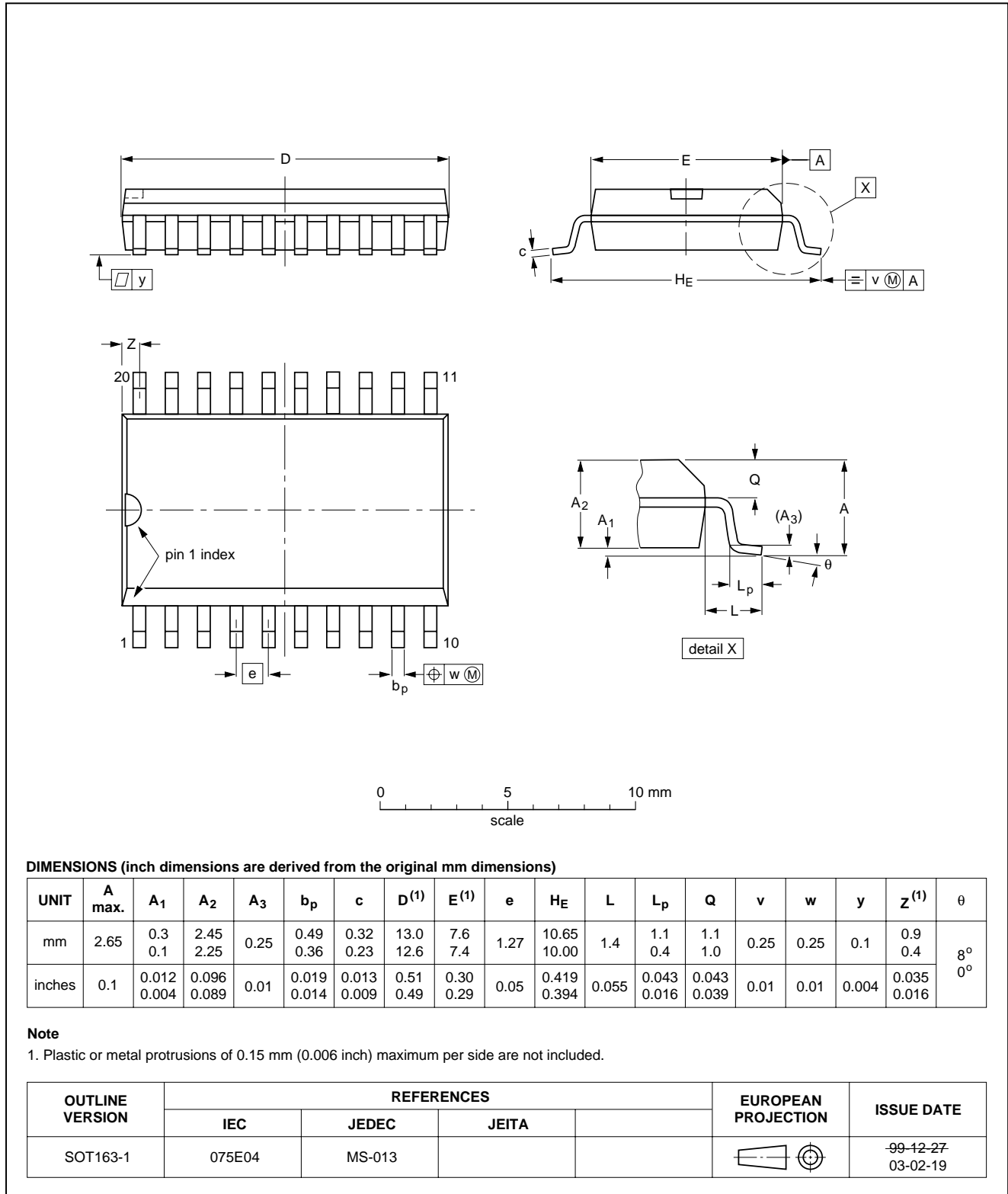
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

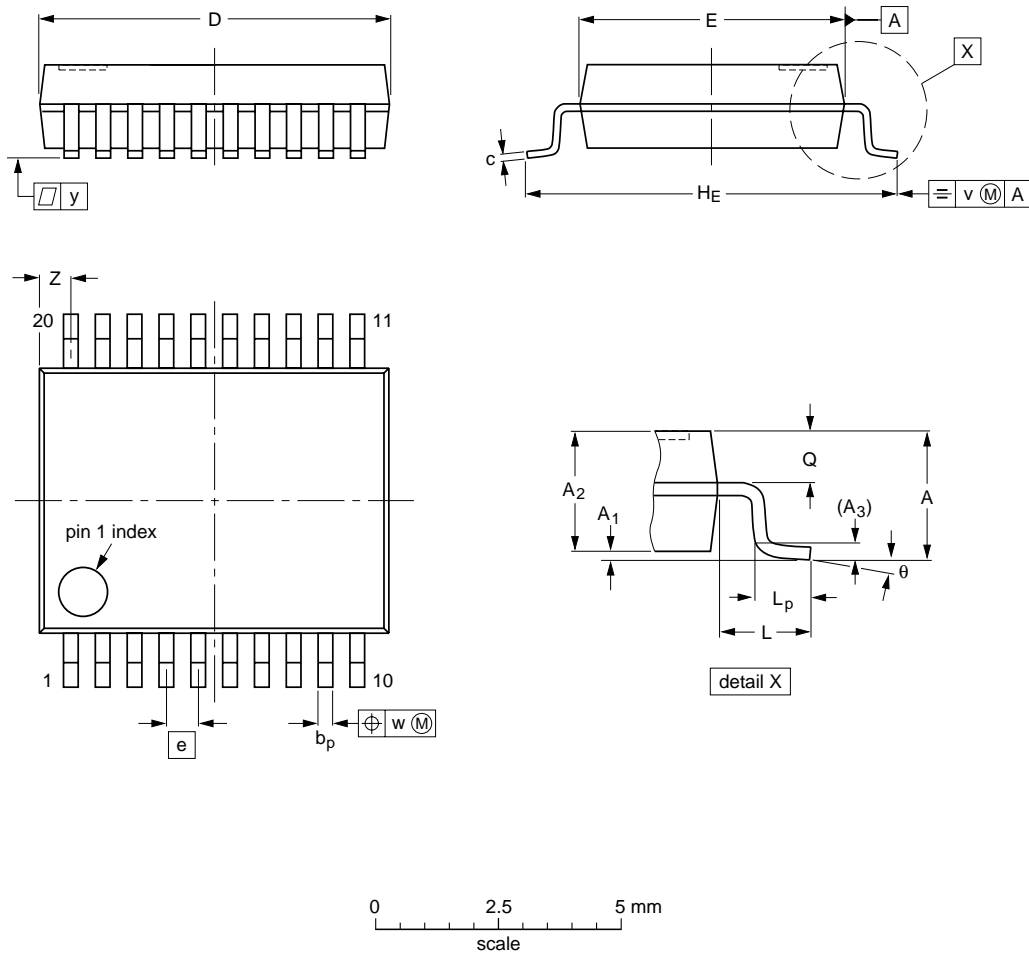


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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

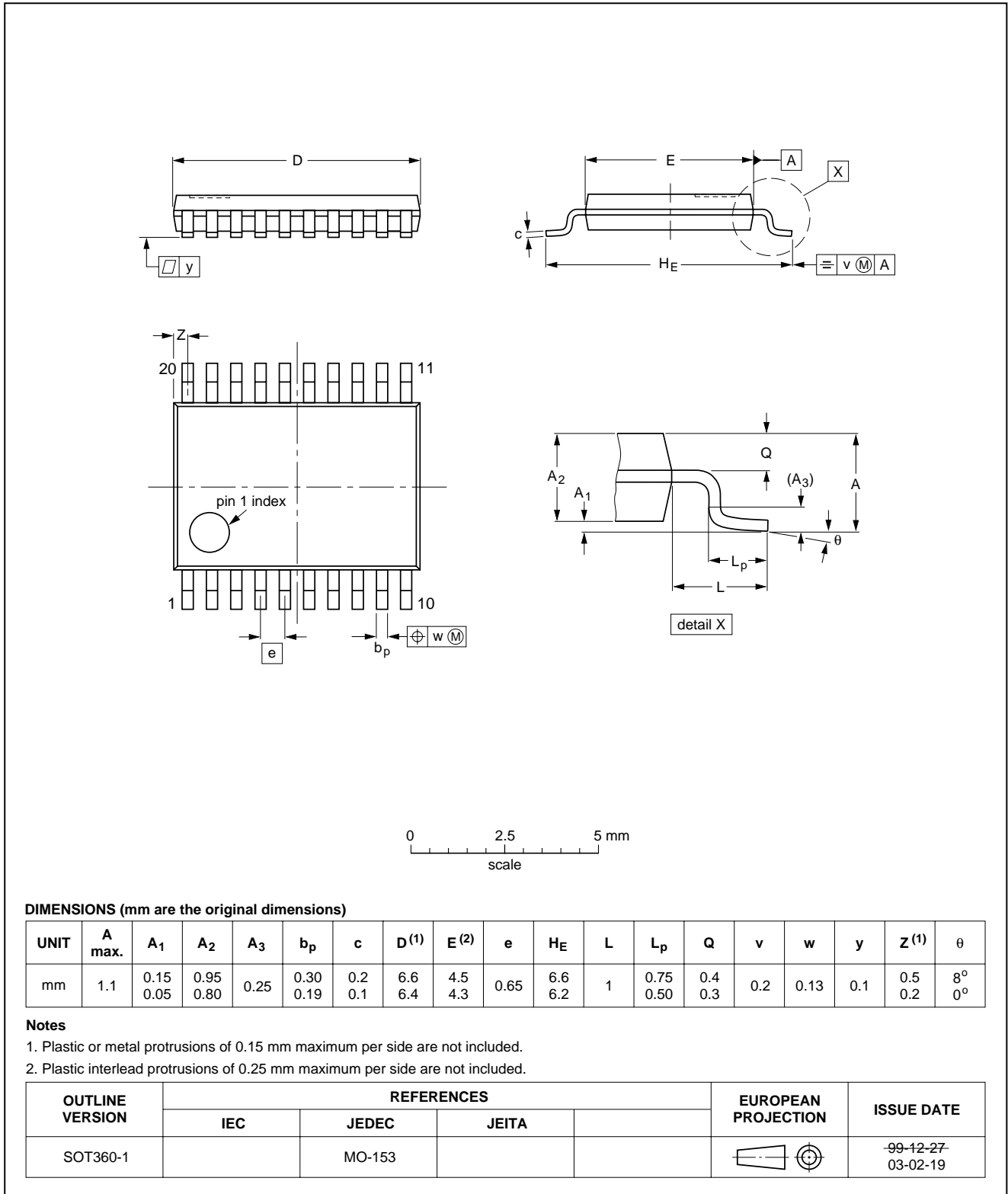
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

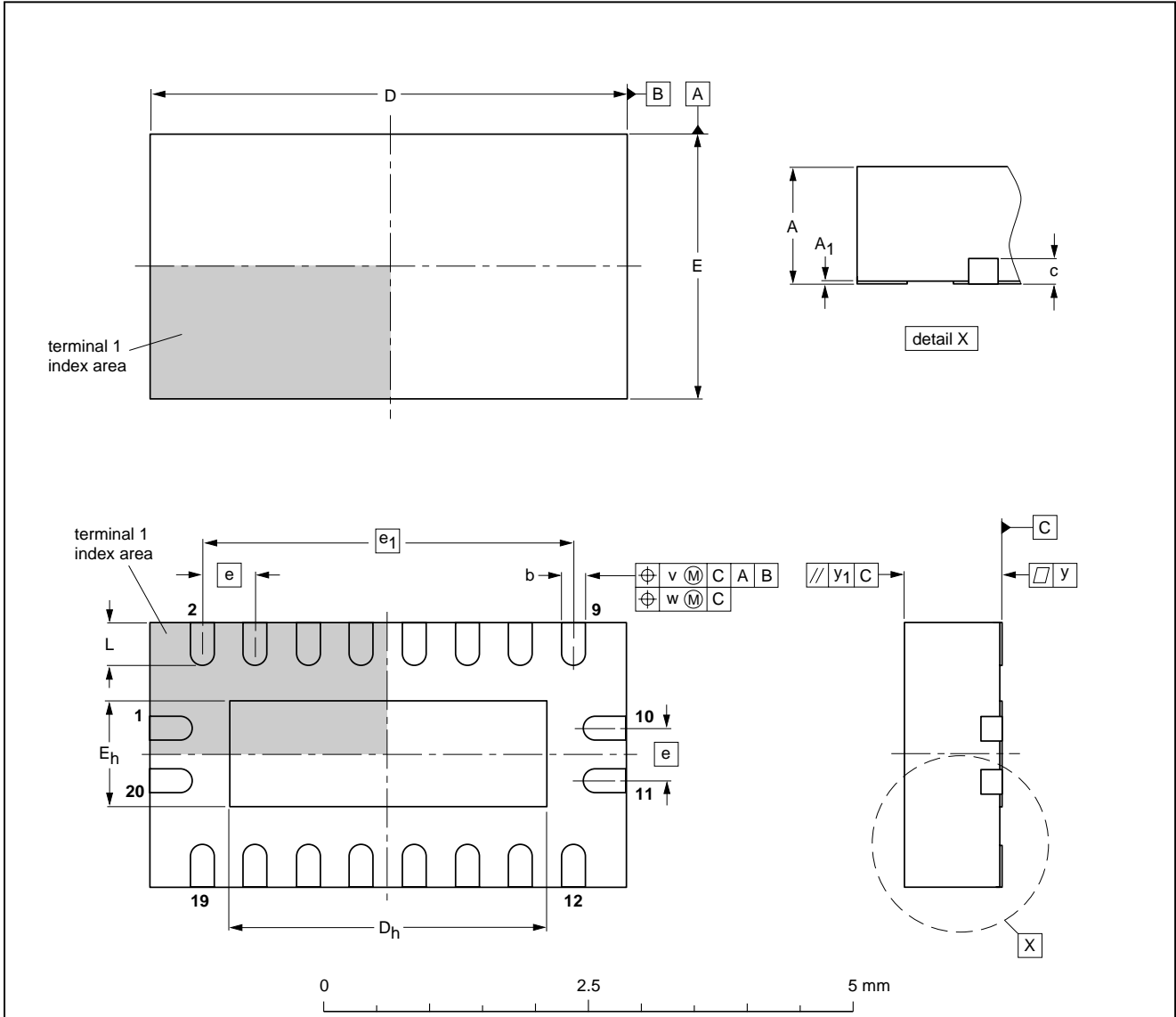


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DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max.	A <sub>1</sub>	b	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	e <sub>1</sub>	L	v	w	y	y <sub>1</sub>
mm	1	0.05 0.00	0.30 0.18	0.2	4.6 4.4	3.15 2.85	2.6 2.4	1.15 0.85	0.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

**Note**  
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT764-1	---	MO-241	---		02-10-17 03-01-27



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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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