74LVC169

Presettable synchronous 4-bit up/down binary counter

Rev. 04 — 14 October 2004 Product data sheet

1. General description

The 74LVC169 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC169 is a synchronous presettable 4-bit binary counter which features an internal look-ahead carry circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the output (pins Q0 to Q3) change coincident with each other when so instructed by the count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock (pin CP) input triggers the four flip-flops on the LOW-to-HIGH transition of the clock. The counter is fully programmable; that is, the outputs may be preset to any number between 0 and it's maximum count. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable (pin $\overline{PE}$) input disables the counter and causes the data at the Dn input to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of the counting is controlled by the up/down (pin U/$\overline{D}$) input. When pin U/$\overline{D}$ is HIGH, the counter counts up, when LOW, it counts down. The look-ahead carry circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs and a terminal count (pin $\overline{TC}$) output. Both count-enable (pins $\overline{CEP}$ and $\overline{CET}$) inputs must be LOW to count. Input pin $\overline{CET}$ is fed forward to enable the terminal count (pin $\overline{TC}$) output. Pin $\overline{TC}$ thus enabled will produce a LOW-level output pulse with a duration approximately equal to a HIGH level portion of pin Q0 output. The LOW level pin $\overline{TC}$ pulse is used to enable successive cascaded stages. The 74LVC169 use edge triggered J-K type flip-flops and have no constraints on changing the control of data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the next LOW-to-HIGH transition of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the mode select table. When pin $\overline{PE}$ is LOW, the data on the input pins D0 to D3 enter the flip-flops on the next LOW-to-HIGH transition of the clock. In order for counting to occur, both pins $\overline{CEP}$ and $\overline{CET}$ must be LOW and pin $\overline{PE}$ must be HIGH. The pin U/$\overline{D}$ input determines the direction of the counting. The terminal count output pin $\overline{TC}$ output is normally HIGH and goes LOW, provided that pin $\overline{CET}$ is LOW, when a counter reaches 15 in the count up mode.The pin $\overline{TC}$ output state is not a function of the count-enable parallel (pin $\overline{CEP}$) input level. Since pin $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on pin $\overline{TC}$. For this reason the use of pin $\overline{TC}$ as a clock signal is not recommended; see the following logic equations:

count enable = $\overline{CEP} \times \overline{CET} \times \overline{PE}$
count up: TC = $Q3 \times Q2 \times Q1 \times Q0 \times CET \times (U/\overline{D})$
count down: TC = $\overline{Q3} \times \overline{Q2} \times \overline{Q1} \times \overline{Q0} \times CET \times (\overline{U}/D)$.

PHILIPS

2. Features

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-B/JESD36
- Up/down counting
- Two count enable inputs for n-bit cascading
- Built-in look-ahead carry capability
- Presettable for programmable operation
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C.

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay	C_L = 50 pF; V_{CC} = 3.3 V				
	CP to Qn		-	4.0	-	ns
	CP to $\overline{TC}$		-	4.8	-	ns
	$\overline{CET}$ to $\overline{TC}$		-	4.1	-	ns
	U/$\overline{D}$ to $\overline{TC}$		-	3.7	-	ns
f_{max}	maximum clock frequency		-	200	-	MHz
C_I	input capacitance		-	5.0	-	pF
C_{PD}	power dissipation capacitance per gate	[1] [2]	-	20	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacity in pF;
V_{CC} = supply voltage in Volts;
N = number of inputs switching;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC169D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC169DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC169PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC169BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body $2.5 \times 3.5 \times 0.85$ mm	SOT763-1

5. Functional diagram

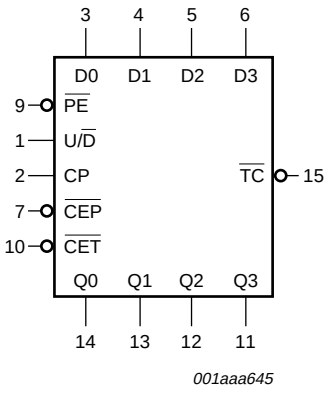


Fig 1. Logic symbol.

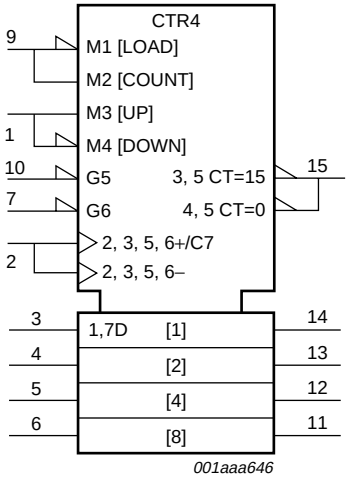


Fig 2. IEC logic symbol.

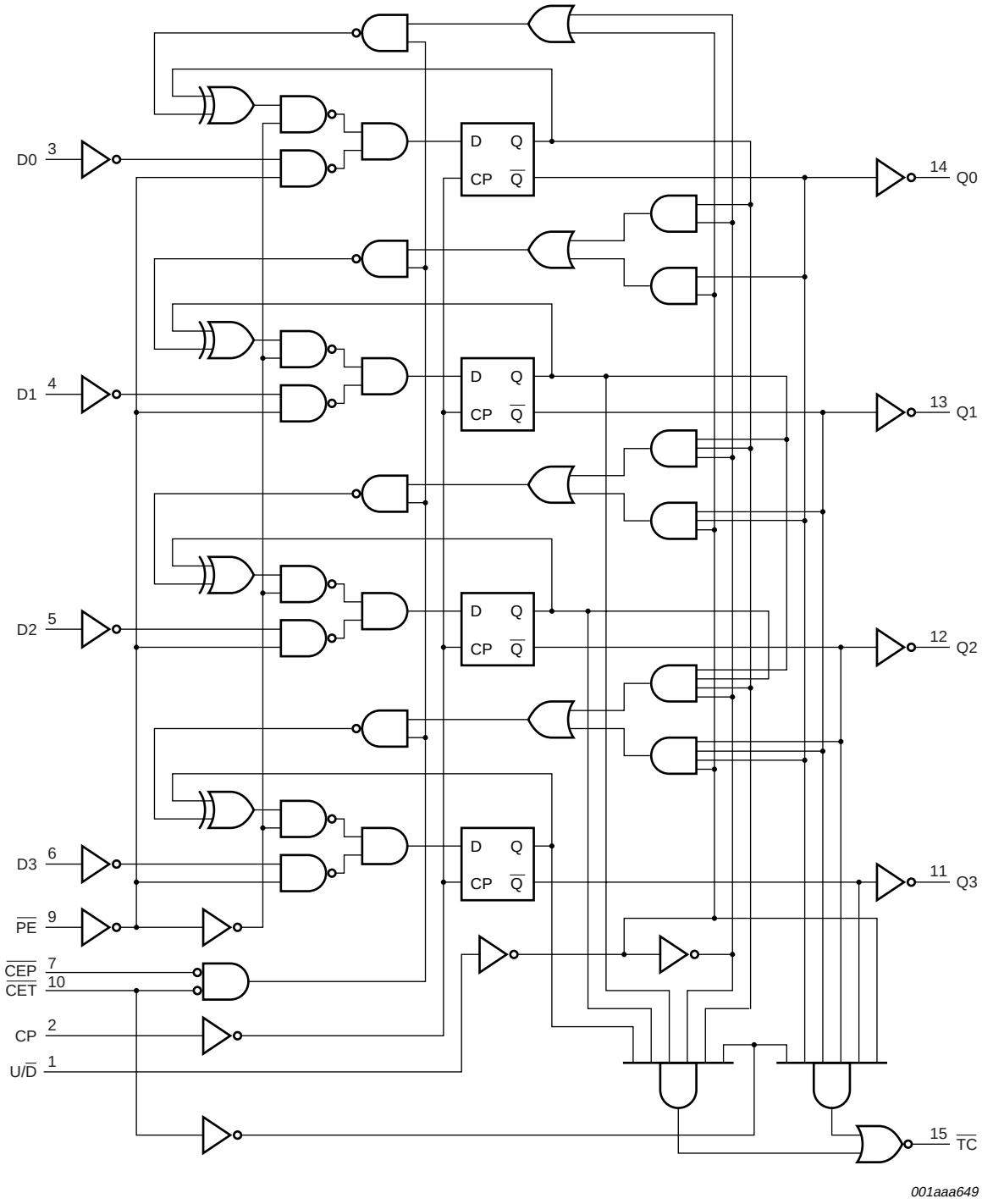


Fig 3. Logic diagram.

6. Pinning information

6.1 Pinning

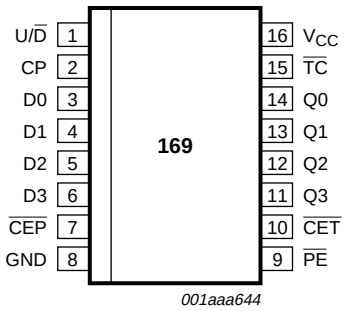
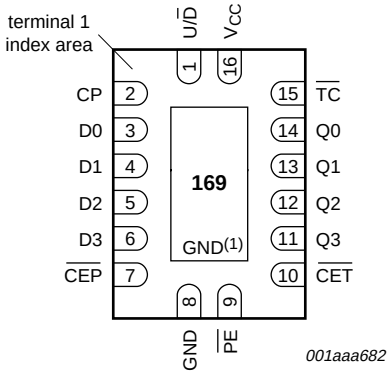


Fig 4. Pin configuration SO16 and (T)SSOP16 package.



Transparent top view

(1) The die substrate is attached to this pad using conductive die material. It can not be used as a supply pin or input.

Fig 5. Pin configuration DHVQFN16 package.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
U/$\overline{D}$	1	up/down control input
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0	3	data input
D1	4	data input
D2	5	data input
D3	6	data input
$\overline{CEP}$	7	count enable input (active LOW)
GND	8	ground (0V)
$\overline{PE}$	9	parallel enable input (active LOW)
$\overline{CET}$	10	count enable carry input (active LOW)
Q3	11	flip-flop output
Q2	12	flip-flop output
Q1	13	flip-flop output
Q0	14	flip-flop output
$\overline{TC}$	15	terminal count output (active LOW)
V_{CC}	16	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating modes	Input						Output	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	Dn	Qn	$\overline{TC}$
Parallel load (Dn → Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	l	h	H	*
Count up (increment)	↑	h	l	l	h	X	count up	*
Count down (decrement)	↑	l	l	l	h	X	count down	*
Hold (do nothing)	↑	X	h	X	h	X	qn	*
	↑	X	X	X	h	X	qn	H

[1] H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
qn = Lower case letters indicate state of referenced output prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
* = The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at terminal count.
Terminal count up is (HHHH) and terminal count down is (LLLL).

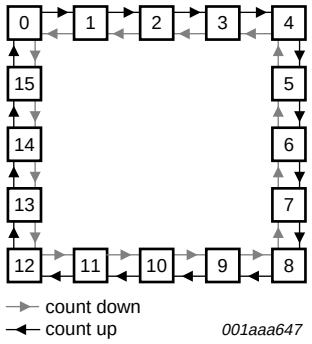
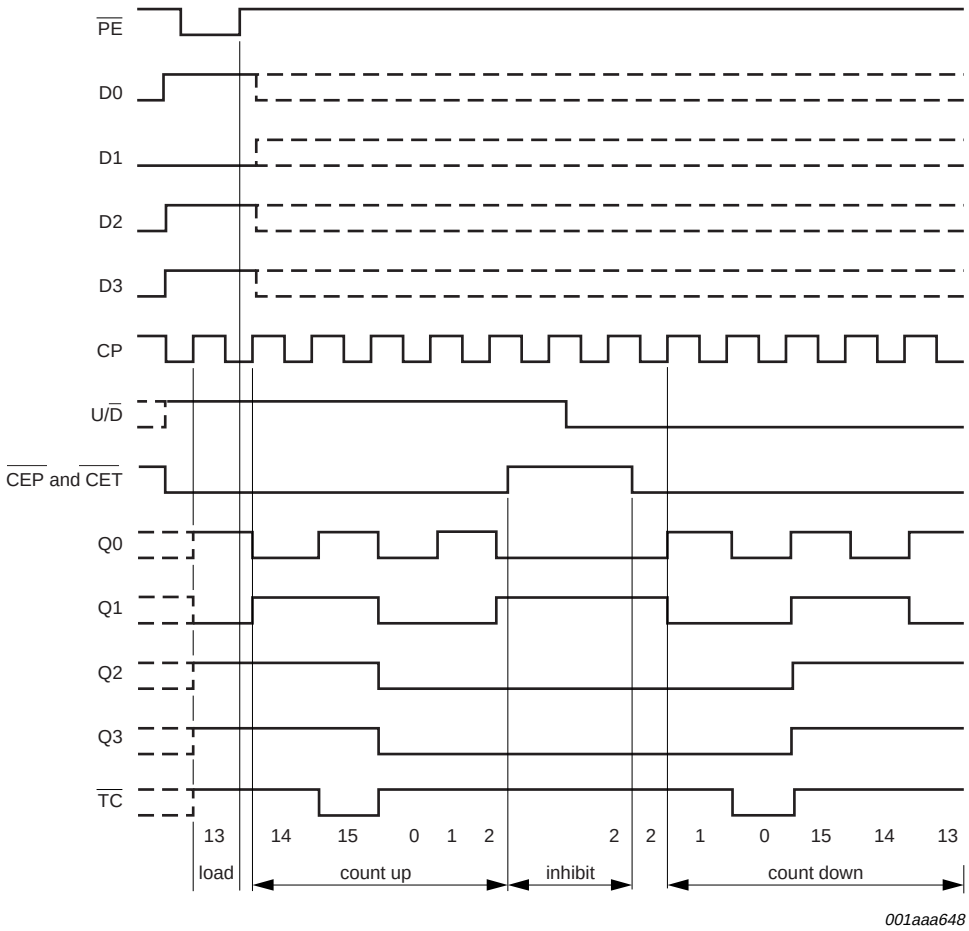


Fig 6. State diagram.



Illustrated is the following sequence:

- Load (preset) to thirteen.
- count up to fourteen, fifteen (maximum), zero, one and two.
- Inhibit.
- Countdown to one, zero (minimum), fifteen, fourteen and thirteen.

Fig 7. Typical timing sequence.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+5.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_O	output source or sink current			-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current	V_O = 0 V to V_{CC}		-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C, P_{tot} derates linearly with 8 mW/K.
For (T)SSOP16 packages: above 60 °C, P_{tot} derates linearly with 5.5 mW/K.
For DHVQFN16 packages: above 60 °C, P_{tot} derates linearly with 4.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating temperature	free-air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V

Table 7: Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\ \mu A$; $V_{CC} = 2.7\ V$ to $3.6\ V$	$V_{CC} - 0.2$	V_{CC}	-	V
		$I_O = -12\ mA$; $V_{CC} = 2.7\ V$	$V_{CC} - 0.5$	-	-	V
		$I_O = -18\ mA$; $V_{CC} = 3.0\ V$	$V_{CC} - 0.6$	-	-	V
		$I_O = -24\ mA$; $V_{CC} = 3.0\ V$	$V_{CC} - 0.8$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\ \mu A$; $V_{CC} = 2.7\ V$ to $3.6\ V$	-	GND	0.2	V
		$I_O = 12\ mA$; $V_{CC} = 2.7\ V$	-	-	0.4	V
		$I_O = 24\ mA$; $V_{CC} = 3.0\ V$	-	-	0.55	V
I_{LI}	input leakage current	$V_{CC} = 3.6\ V$; $V_I = 5.5\ V$ or GND	-	±0.1	±5	µA
I_{CC}	quiescent supply current	$V_{CC} = 3.6\ V$; $V_I = V_{CC}$ or GND; $I_O = 0\ A$	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_{CC} = 2.7\ V$ to $3.6\ V$; $V_I = V_{CC} - 0.6\ V$; $I_O = 0\ A$	-	5	500	µA
C_I	input capacitance		-	5.0	-	pF
$T_{amb} = -40\ °C$ to $+125\ °C$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\ V$	V_{CC}	-	-	V
		$V_{CC} = 2.7\ V$ to $3.6\ V$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\ V$	-	-	GND	V
		$V_{CC} = 2.7\ V$ to $3.6\ V$	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\ \mu A$; $V_{CC} = 2.7\ V$ to $3.6\ V$	$V_{CC} - 0.3$	-	-	V
		$I_O = -12\ mA$; $V_{CC} = 2.7\ V$	$V_{CC} - 0.65$	-	-	V
		$I_O = -18\ mA$; $V_{CC} = 3.0\ V$	$V_{CC} - 0.75$	-	-	V
		$I_O = -24\ mA$; $V_{CC} = 3.0\ V$	$V_{CC} - 1$	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\ \mu A$; $V_{CC} = 2.7\ V$ to $3.6\ V$	-	-	0.3	V
		$I_O = 12\ mA$; $V_{CC} = 2.7\ V$	-	-	0.6	V
		$I_O = 24\ mA$; $V_{CC} = 3.0\ V$	-	-	0.8	V
I_{LI}	input leakage current	$V_{CC} = 3.6\ V$; $V_I = 5.5\ V$ or GND	-	-	±20	µA
I_{CC}	quiescent supply current	$V_{CC} = 3.6\ V$; $V_I = V_{CC}$ or GND; $I_O = 0\ A$	-	-	40	µA
ΔI_{CC}	additional quiescent supply current per input pin	$V_{CC} = 2.7\ V$ to $3.6\ V$; $V_I = V_{CC} - 0.6\ V$; $I_O = 0\ A$	-	-	5000	µA

[1] All typical values are measured at $V_{CC} = 3.3\ V$ and $T_{amb} = 25\ °C$.

11. Dynamic characteristics

Table 8: Dynamic characteristics

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$; see Figure 13.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 8					
		V_{CC} = 1.2 V		-	17	-	ns
		V_{CC} = 2.7 V		1.5	-	7.2	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	4.0	8.0	ns
	propagation delay CP to $\overline{TC}$	see Figure 8					
		V_{CC} = 1.2 V		-	21	-	ns
		V_{CC} = 2.7 V		1.5	-	8.8	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	4.8	6.7	ns
	propagation delay $\overline{CET}$ to $\overline{TC}$	see Figure 9					
		V_{CC} = 1.2 V		-	19	-	ns
		V_{CC} = 2.7 V		1.5	-	7.2	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	4.1	7.2	ns
	propagation delay U/$\overline{D}$ to $\overline{TC}$	see Figure 10					
		V_{CC} = 1.2 V		-	21	-	ns
		V_{CC} = 2.7 V		1.5	-	8.2	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	3.7	7.0	ns
t_W	clock pulse width HIGH or LOW	see Figure 8					
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	4.0	1.2	-	ns
t_{su}	set-up time Dn to CP	see Figure 11					
		V_{CC} = 2.7 V		3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.5	1.0	-	ns
	set-up time $\overline{PE}$ to CP	see Figure 11					
		V_{CC} = 2.7 V		3.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3.0	1.2	-	ns
	set-up time U/$\overline{D}$ to CP	see Figure 12					
		V_{CC} = 2.7 V		6.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	5.5	2.8	-	ns
	set-up time $\overline{CEP}$, $\overline{CET}$ to CP	see Figure 12					
		V_{CC} = 2.7 V		5.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	4.5	2.1	-	ns
t_h	hold time Dn, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$, U/$\overline{D}$ to CP	see Figure 11 and 12					
		V_{CC} = 2.7 V		0.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	0.5	0.0	-	ns
f_{max}	maximum clock pulse frequency	see Figure 8					
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	150	200	-	MHz

Table 8: Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$; see Figure 13.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per gate		[4] [5]	-	20	-	pF
T_{amb} = −40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 8					
		V_{CC} = 2.7 V		1.5	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	10.0	ns
	propagation delay CP to $\overline{TC}$	see Figure 8					
		V_{CC} = 2.7 V		1.5	-	11.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	8.5	ns
	propagation delay $\overline{CET}$ to $\overline{TC}$	see Figure 9					
		V_{CC} = 2.7 V		1.5	-	9.0	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	9.0	ns
	propagation delay U/$\overline{D}$ to $\overline{TC}$	see Figure 10					
		V_{CC} = 2.7 V		1.5	-	10.5	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	9.0	ns
t_W	clock pulse width HIGH or LOW	see Figure 8					
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.0	-	-	ns
t_{su}	set-up time Dn to CP	see Figure 11					
		V_{CC} = 2.7 V		3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.5	-	-	ns
	set-up time $\overline{PE}$ to CP	see Figure 11					
		V_{CC} = 2.7 V		3.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.0	-	-	ns
	set-up time U/$\overline{D}$ to CP	see Figure 12					
		V_{CC} = 2.7 V		6.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		5.5	-	-	ns
	set-up time $\overline{CEP}$, $\overline{CET}$ to CP	see Figure 12					
		V_{CC} = 2.7 V		5.5	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.5	-	-	ns
t_h	hold time Dn, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$, U/$\overline{D}$ to CP	see Figure 11 and 12					
		V_{CC} = 2.7 V		0.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		0.5	-	-	ns
f_{max}	maximum clock pulse frequency	see Figure 8					
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	-	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.5	ns

[1] All typical values are measured at T_{amb} = 25 °C.

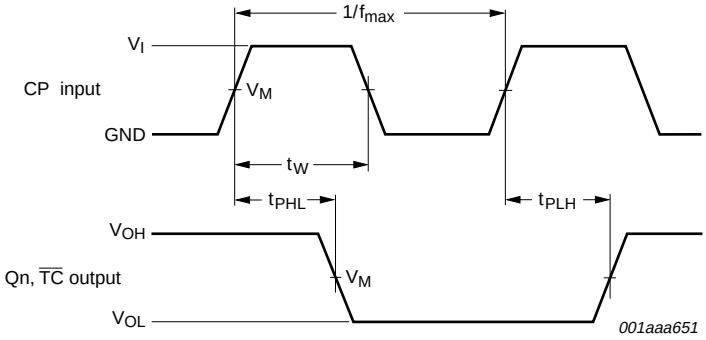
[2] Typical values are measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacity in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

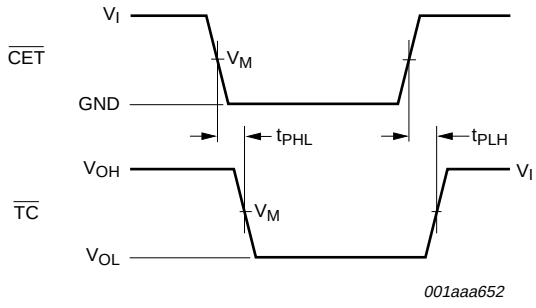
12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

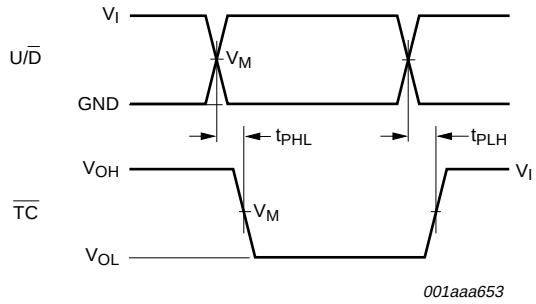
Fig 8. Clock (CP) to outputs (Qn, $\overline{TC}$) propagation delays, the clock pulse width and the maximum clock frequency.



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

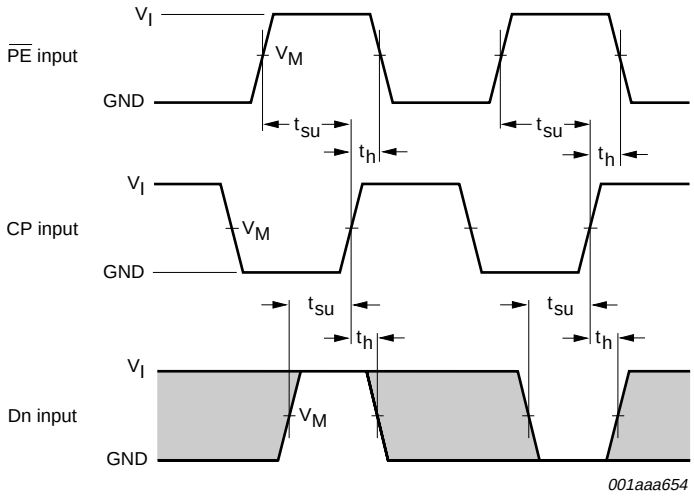
Fig 9. Input ($\overline{CET}$) to output ($\overline{TC}$) propagation delays.



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 10. The up/down control input (U/$\overline{D}$) to output ($\overline{TC}$) propagation delays.

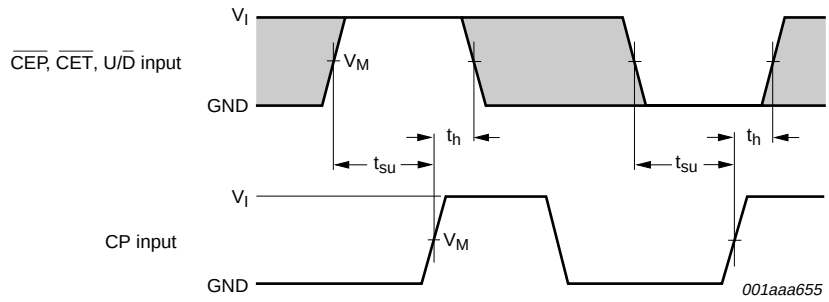


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 11. Set-up and hold times for the input (Dn) and parallel enable input ($\overline{PE}$).



The shaded areas indicate when the input is permitted to change for predictable output performance.

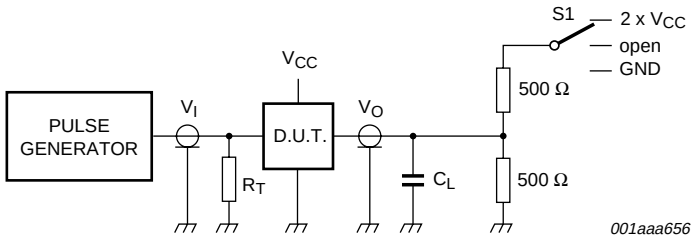
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

Fig 12. Set-up and hold times for count enable inputs ($\overline{CEP}$ and $\overline{CET}$) and control input (U/$\overline{D}$).

Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig 13. Load circuitry for switching times.

Table 10: Measurement points

Supply voltage	Input	Load		Position S1		
V_{CC}	V_I	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when R_L = 1000 Ω.

13. Application information

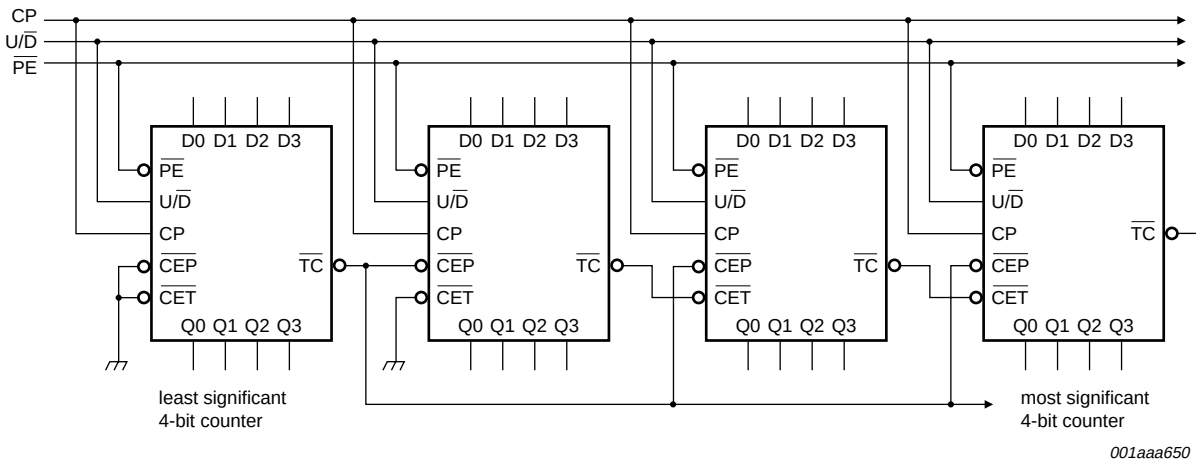
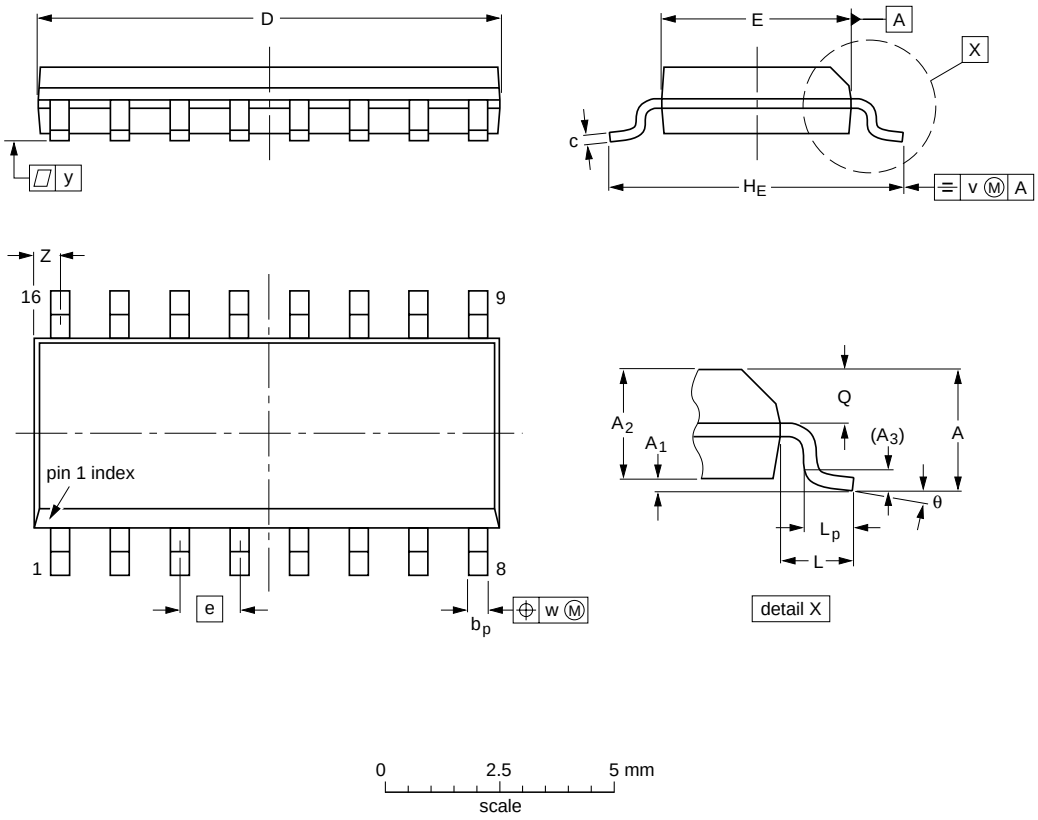


Fig 14. Synchronous multistage counting scheme.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

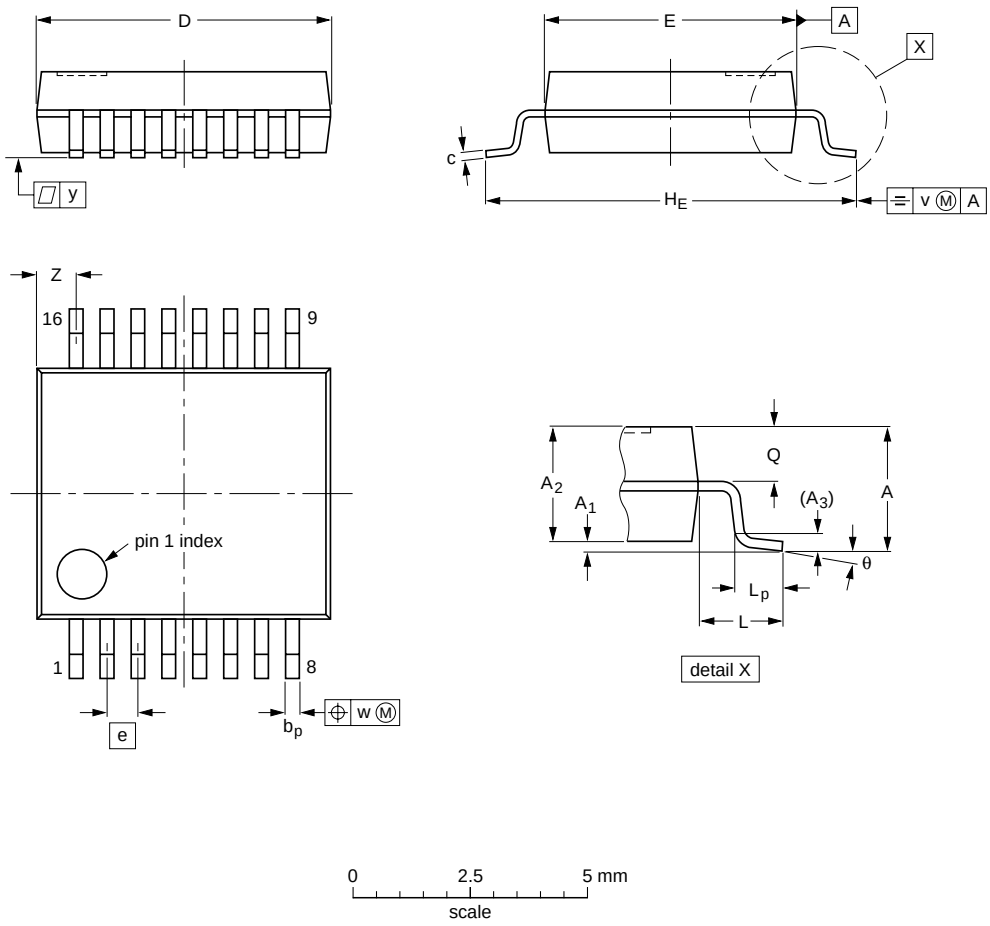
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT109-1 (SO16).

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

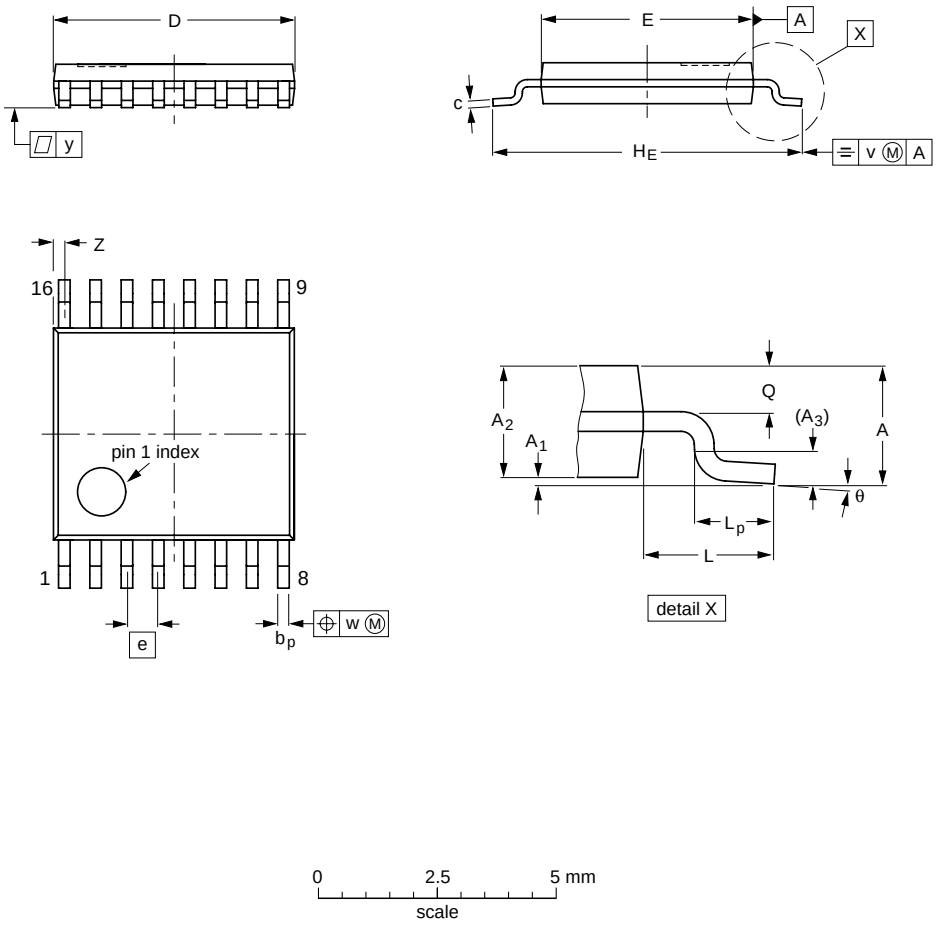
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT338-1 (SSOP16).

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

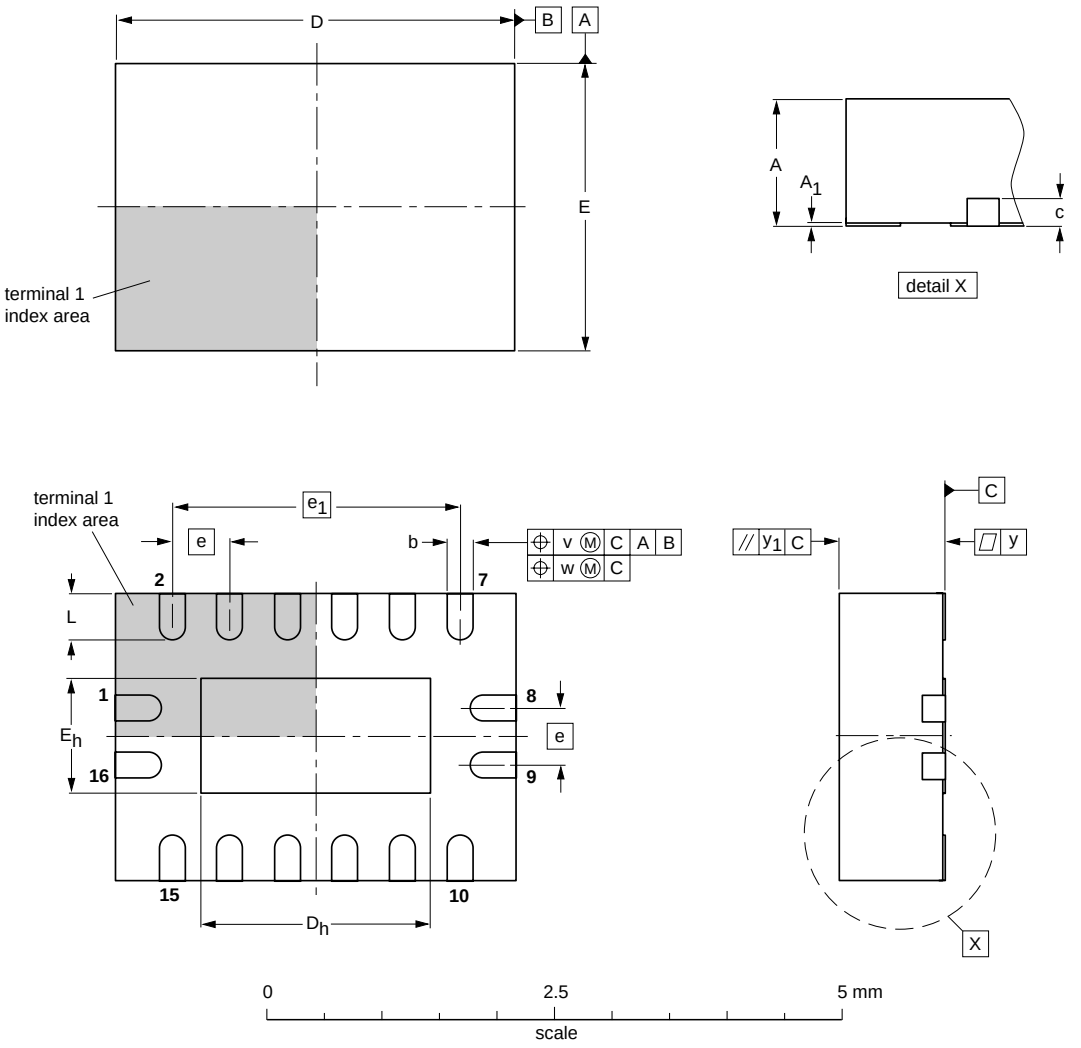
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 17. Package outline SOT403-1 (TSSOP16).

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 18. Package outline SOT763-1 (DHVQFN16).

15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC169_4	14102004	Product data sheet	-	9397 750 13818	74LVC169_3
Modifications:	• Added DHVQFN16 package • Section 1: corrected logic equations • Figure 14: corrected connections between 1st and 2nd counter.				
74LVC169_3	20040512	Product data sheet	-	9397 750 13026	74LVC169_2
74LVC169_2	19980520	Product specification		9397 750 04498	74LVC169_1

16. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

17. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

18. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

19. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

20. Contents

Date of release: 14 October 2004
Document number: 9397 750 13818

Published in The Netherlands