DATA SHEET

74LVC161
Presettable synchronous 4-bit binary counter; asynchronous reset

Product specification
Supersedes data of 1998 May 20

2004 Mar 30

Philips
Semiconductors

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Presettable synchronous 4-bit binary counter; asynchronous reset

74LVC161

FEATURES

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard no. JESD8B/JESD36
- Asynchronous reset
- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC161 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC161 is a synchronous presettable binary counter which features an internal look-head carry and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (pin CP). The outputs (pins Q0 to Q3) of the counters may be preset to a HIGH-level or a LOW-level. A LOW-level at the parallel enable input (pin $\overline{PE}$) disables the counting action and causes the data at the data inputs (pins D0 to D3) to be loaded into the counter on the positive-going edge of the clock (provided that the set-up and hold time requirements for PE are met). Preset takes place regardless of the levels at count enable inputs (pins CEP and CET). A LOW-level at the master reset input (pin $\overline{MR}$) sets all four outputs of the flip-flops (pins Q0 to Q3) to LOW-level regardless of the levels at input pins CP, $\overline{PE}$, CET and CEP (thus providing an asynchronous clear function).

The look-ahead carry simplifies serial cascading of the counters. Both count enable inputs (pins CEP and CET) must be HIGH to count. The CET input is fed forward to enable the terminal count output (pin TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH-level output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by t_{PHL} (propagation delay CP to TC) and t_{su} (set-up time CEP to CP) according to the following formula: $f_{max} = \frac{1}{t_{PHL(max)} + t_{su}}$

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay	C_L = 50 pF; V_{CC} = 3.3 V		
	CP to Qn		3.9	ns
	CP to TC		4.5	ns
	$\overline{MR}$ to Qn		3.5	ns
	$\overline{MR}$ to TC		4.7	ns
	CET to TC		3.3	ns
$f_{clk(max)}$	maximum clock frequency		200	MHz
C_I	input capacitance		5.0	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	18	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74LVC161D	–40 °C to +125 °C	16	SO16	plastic	SOT109-1
74LVC161DB	–40 °C to +125 °C	16	SSOP16	plastic	SOT338-1
74LVC161PW	–40 °C to +125 °C	16	TSSOP16	plastic	SOT403-1
74LVC161BQ	–40 °C to +125 °C	16	DHVQFN16	plastic	SOT763-1

FUNCTION TABLE

See note 1.

OPERATING MODES	INPUT						OUTPUT	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	*
Count	H	↑	h	h	h	X	count	*
Hold (do nothing)	H	X	l	X	h	X	q_n	*
	H	X	X	l	h	X	q_n	L

Note

1. * = The TC output is HIGH when CET is HIGH and the counter is at terminal count (HHHH).

   H = HIGH voltage level.

   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.

   L = LOW voltage level.

   l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.

   q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

   X = don't care.

   ↑ = LOW-to-HIGH clock transition.

PINNING

PIN	SYMBOL	DESCRIPTION
1	$\overline{MR}$	synchronous master reset (active LOW)
2	CP	clock input (LOW-to-HIGH, edge-triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable inputs
8	GND	ground (0 V)
9	$\overline{PE}$	parallel enable input (active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V_{CC}	supply voltage

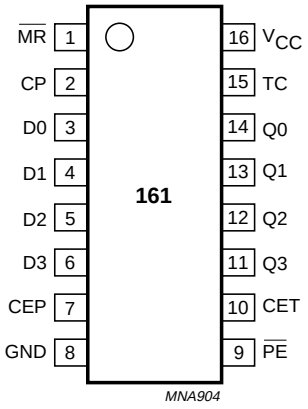
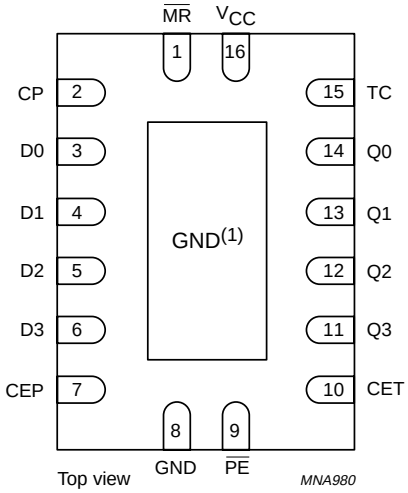


Fig.1 Pin configuration SO16 and (T)SSOP16.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN16.

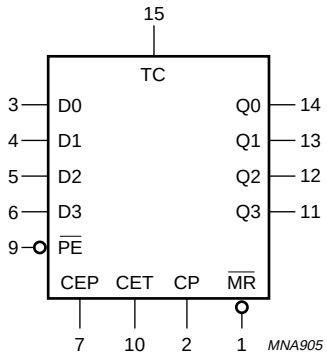


Fig.3 Logic symbol.

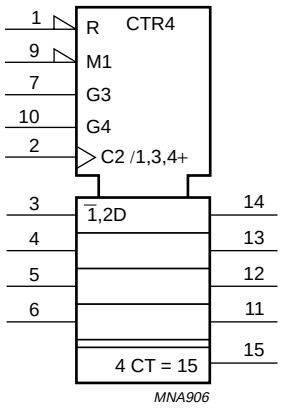


Fig.4 Logic symbol (IEEE/IEC).

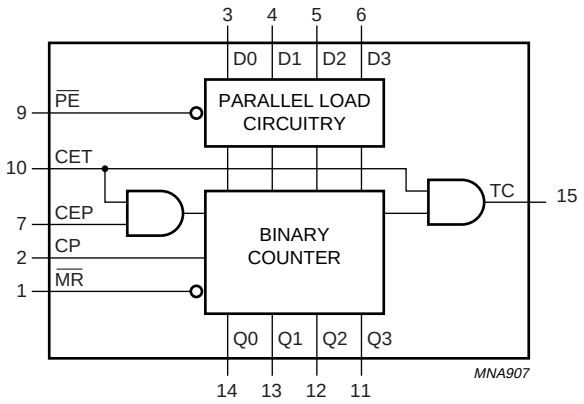


Fig.5 Functional diagram.

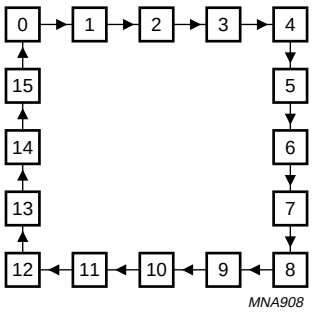
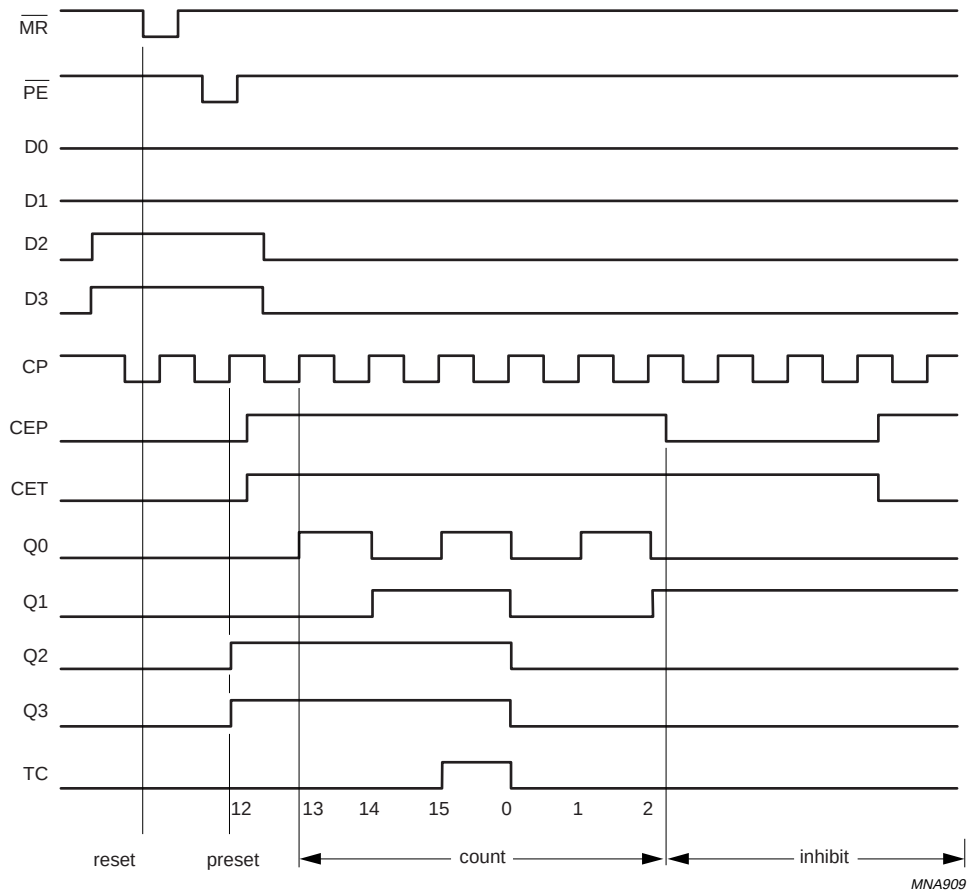


Fig.6 State diagram.



Typical timing sequence: reset outputs to zero; preset to binary twelve; count to thirteen, fourteen, fifteen, zero, one and two; inhibit.

Fig.7 Timing sequence.

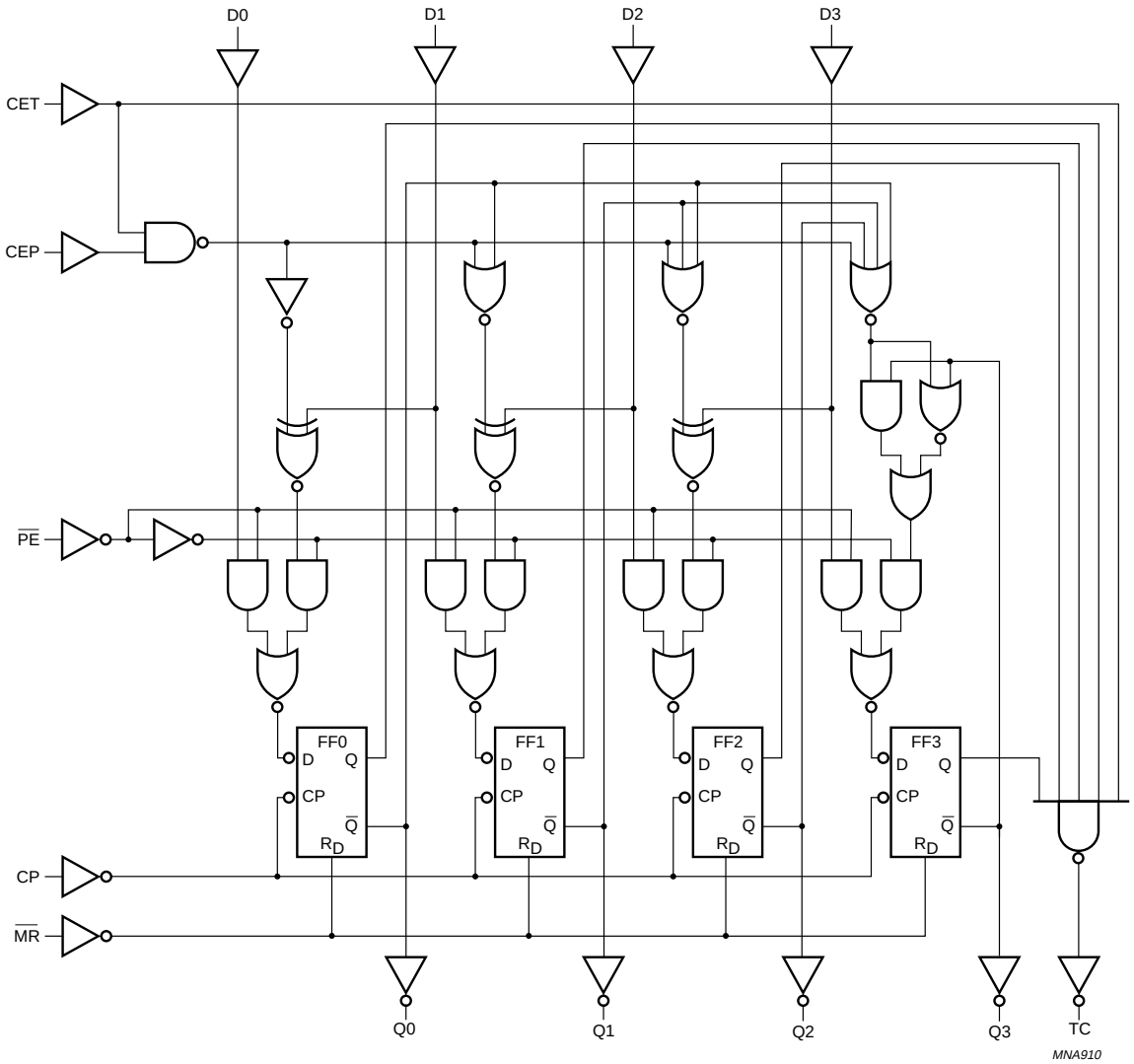


Fig.8 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	for maximum speed performance	2.7	3.6	V
		for low voltage applications	1.2	3.6	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating temperature	in free-air	–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	–	+6.5	V
I_{IK}	input diode current	V_I < 0 V	–	–50	–	mA
V_I	input voltage	note 2	–0.5	–	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V	–	±50	–	mA
V_O	output voltage	note 2	–0.5	–	V_{CC} + 0.5	V
I_O	output source of sink current	V_O = 0 V to V_{CC}	–	±50	–	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	–	mA
T_{stg}	storage temperature		–65	–	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 3	–	500	–	mW

Notes

1. Stresses beyond those listed may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other condition beyond those indicated under “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. For SO16 packages: above 70 °C derate linearly with 8 mW/K.

   For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

   For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.2	V_{CC}	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.5	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.6	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 0.8	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	GND	0.2	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	±0.1	±5	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1)	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.2	V_{CC}	–	–	V
			2.7 to 3.6	2.0	–	–	V
V_{IL}	LOW-level input voltage		1.2	–	–	GND	V
			2.7 to 3.6	–	–	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	2.7 to 3.6	V_{CC} − 0.3	–	–	V
		I_O = −12 mA	2.7	V_{CC} − 0.65	–	–	V
		I_O = −18 mA	3.0	V_{CC} − 0.75	–	–	V
		I_O = −24 mA	3.0	V_{CC} − 1	–	–	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	2.7 to 3.6	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.6	V
		I_O = 24 mA	3.0	–	–	0.8	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	3.6	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0 A	3.6	–	–	40	μA
ΔI_{CC}	additional quiescent supply current per input pin	V_I = V_{CC} − 0.6 V; I_O = 0 A	2.7 to 3.6	–	–	5000	μA

Note

1. Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

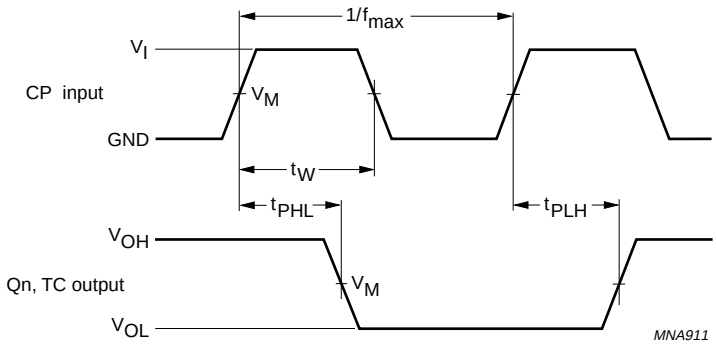
SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 9 and 14	1.2	–	17	–	ns
			2.7	1.5	–	7.2	ns
			3.0 to 3.6	1.5	3.9[2]	7.3	ns
	propagation delay CP to TC	see Figs 9 and 14	1.2	–	20	–	ns
			2.7	1.5	–	7.8	ns
			3.0 to 3.6	1.5	4.5[2]	7.8	ns
	propagation delay CET to TC	see Figs 10 and 14	1.2	–	16	–	ns
			2.7	1.5	–	6.5	ns
			3.0 to 3.6	1.5	3.3[2]	6.0	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 11 and 14	1.2	–	17	–	ns
			2.7	1.5	–	7.1	ns
			3.0 to 3.6	1.5	3.5[2]	6.4	ns
	propagation delay $\overline{MR}$ to TC	see Figs 11 and 14	1.2	–	18	–	ns
			2.7	1.5	–	8.6	ns
			3.0 to 3.6	1.5	4.7[2]	8.0	ns
t_W	clock pulse width HIGH or LOW	see Fig.9	2.7	5.0	–	–	ns
			3.0 to 3.6	4.0	1.2[2]	–	ns
	master reset width LOW	see Fig.11	2.7	4.0	–	–	ns
			3.0 to 3.6	3.0	1.6[2]	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Fig.11	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	0.0[2]	–	ns
t_{su}	set-up time Dn to CP	see Fig.12	2.7	3.0	–	–	ns
			3.0 to 3.6	2.5	1.0[2]	–	ns
	set-up time $\overline{PE}$ to CP	see Fig.12	2.7	3.5	–	–	ns
			3.0 to 3.6	3.0	1.2[2]	–	ns
	set-up time CEP, CET to CP	see Fig.13	2.7	5.5	–	–	ns
			3.0 to 3.6	5.0	2.1[2]	–	ns
t_h	hold time Dn, $\overline{PE}$, CEP, CET to CP	see Figs 12 and 13	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	0.0[2]	–	ns
$f_{clk(max)}$	maximum clock frequency	see Fig.9	2.7	150	–	–	MHz
			3.0 to 3.6	150	200[2]	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.0	ns

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay CP to Qn	see Figs 9 and 14	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	9.5	ns
	propagation delay CP to TC	see Figs 9 and 14	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.5	–	10.0	ns
	propagation delay CET to TC	see Figs 10 and 14	1.2	–	–	–	ns
			2.7	1.5	–	8.5	ns
			3.0 to 3.6	1.5	–	7.5	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	see Figs 11 and 14	1.2	–	–	–	ns
			2.7	1.5	–	9.0	ns
			3.0 to 3.6	1.5	–	8.0	ns
	propagation delay $\overline{MR}$ to TC	see Figs 11 and 14	1.2	–	–	–	ns
			2.7	1.5	–	11.0	ns
			3.0 to 3.6	1.5	–	10.0	ns
t_W	clock pulse width HIGH or LOW	see Fig.9	2.7	5.0	–	–	ns
			3.0 to 3.6	4.0	–	–	ns
	master reset width LOW	see Fig.11	2.7	4.0	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
t_{rem}	removal time $\overline{MR}$ to CP	see Fig.11	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	–	–	ns
t_{su}	set-up time Dn to CP	see Fig.12	2.7	3.0	–	–	ns
			3.0 to 3.6	2.5	–	–	ns
	set-up time $\overline{PE}$ to CP	see Fig.12	2.7	3.5	–	–	ns
			3.0 to 3.6	3.0	–	–	ns
	set-up time CEP, CET to CP	see Fig.13	2.7	5.5	–	–	ns
			3.0 to 3.6	5.0	–	–	ns
t_h	hold time Dn, $\overline{PE}$, CEP, CET to CP	see Figs 12 and 13	2.7	0.0	–	–	ns
			3.0 to 3.6	0.5	–	–	ns
$f_{clk(max)}$	maximum clock frequency	see Fig.9	2.7	150	–	–	MHz
			3.0 to 3.6	150	–	–	MHz
$t_{sk(0)}$	skew	note 3	3.0 to 3.6	–	–	1.5	ns

Notes

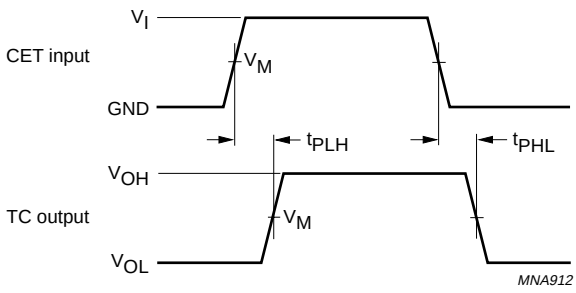
1. All typical values are measured at T_{amb} = 25 °C.
2. Typical values are measured at V_{CC} = 3.3 V.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

AC WAVEFORMS



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.9 Clock (CP) to outputs (Qn, TC) propagation delays, the clock pulse width and the maximum clock frequency.



V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.
$V_M = 0.5V_{CC}$ at V_{CC} < 2.7 V.
V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.10 Input (CET) to output (TC) propagation delays.

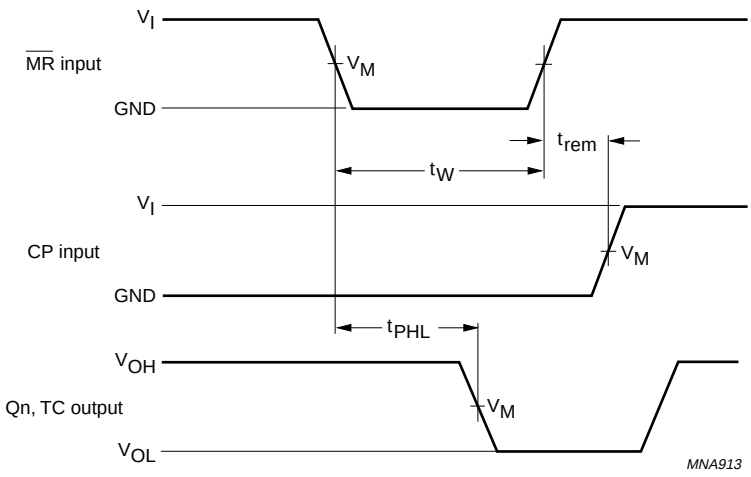
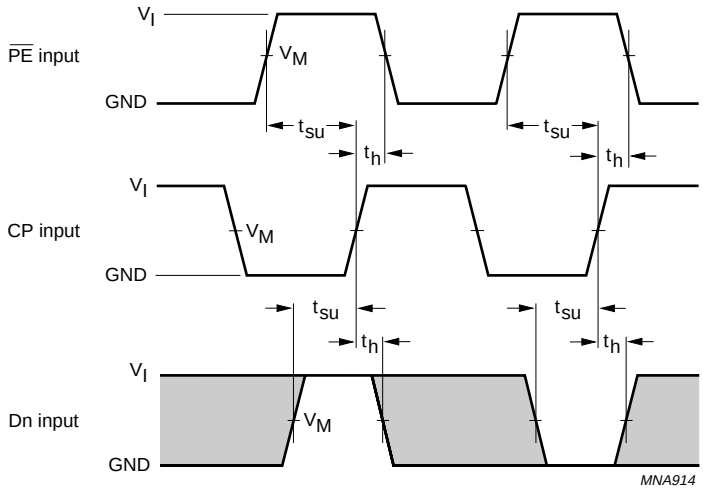
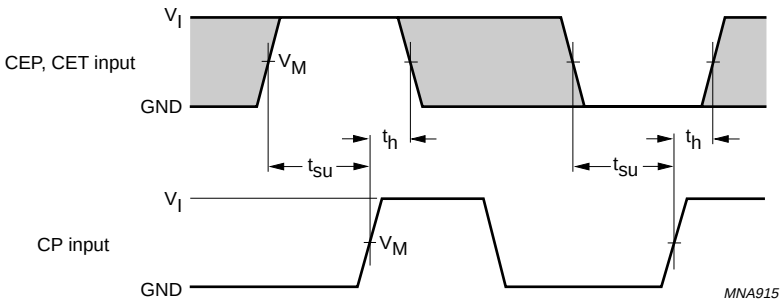


Fig.11 Master reset ($\overline{MR}$) pulse width, the master reset to output (Qn, TC) propagation delays and the master reset to clock (CP) removal times.



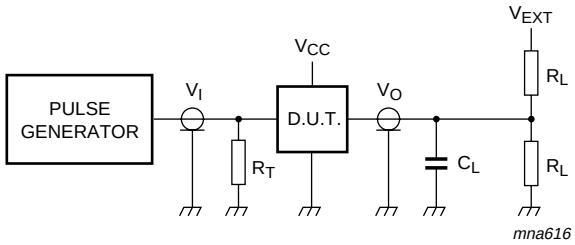
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.12 Set-up and hold times for the input (Dn) and parallel enable input ($\overline{PE}$).



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.13 CEP and CET set-up and hold times.



V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.2 V	V_{CC}	50 pF	500 Ω[1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Note

1. The circuit performs better when R_L = 1000 Ω.

Definitions for test circuit:

R_L = Load resistor.

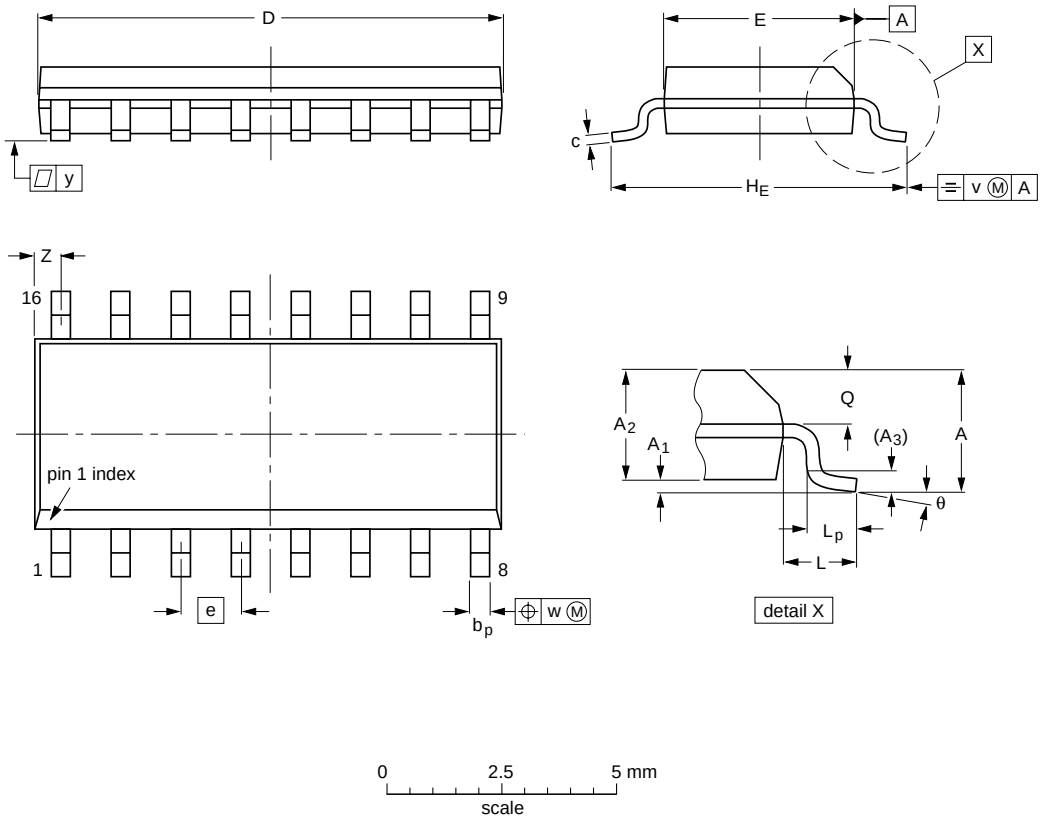
C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.14 Load circuitry for switching times.

PACKAGE OUTLINES

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

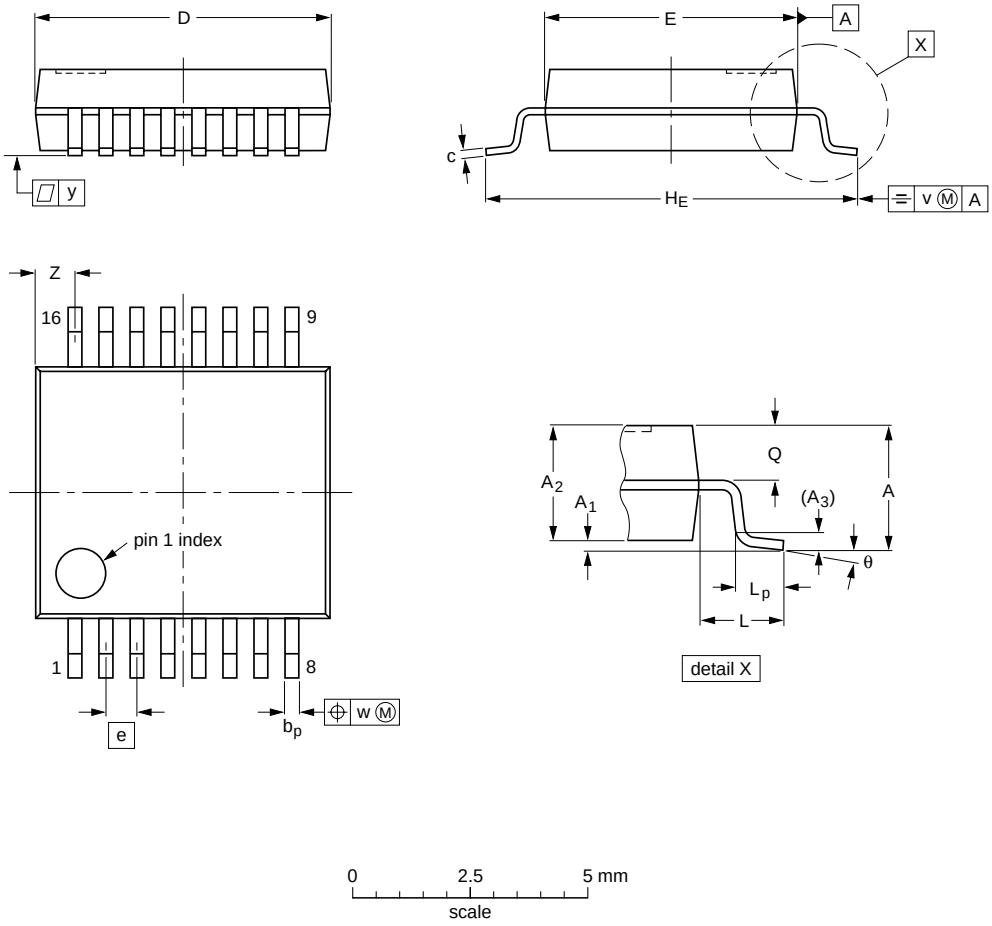
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

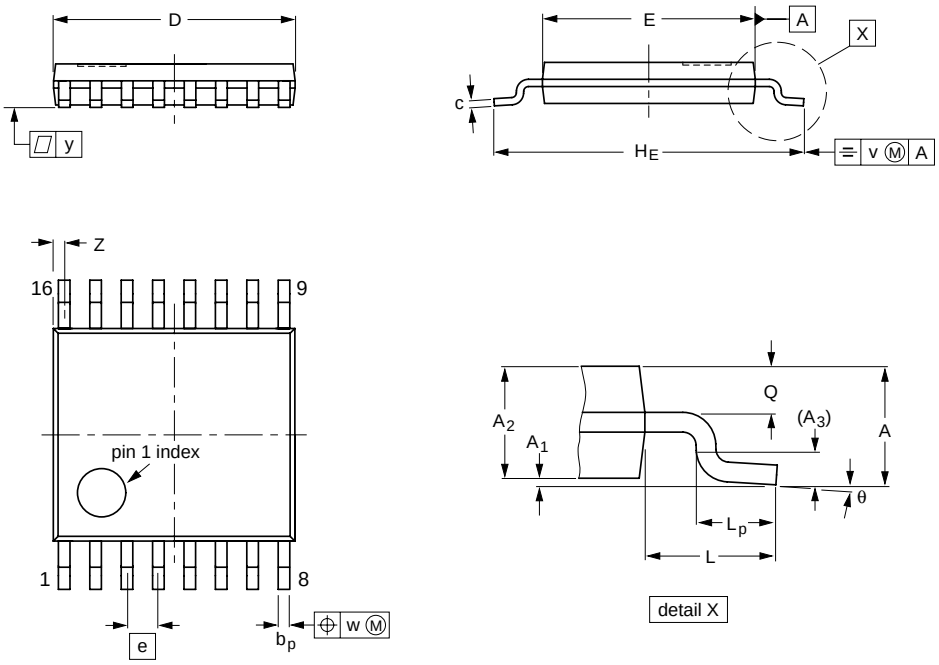
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

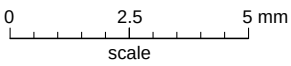
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

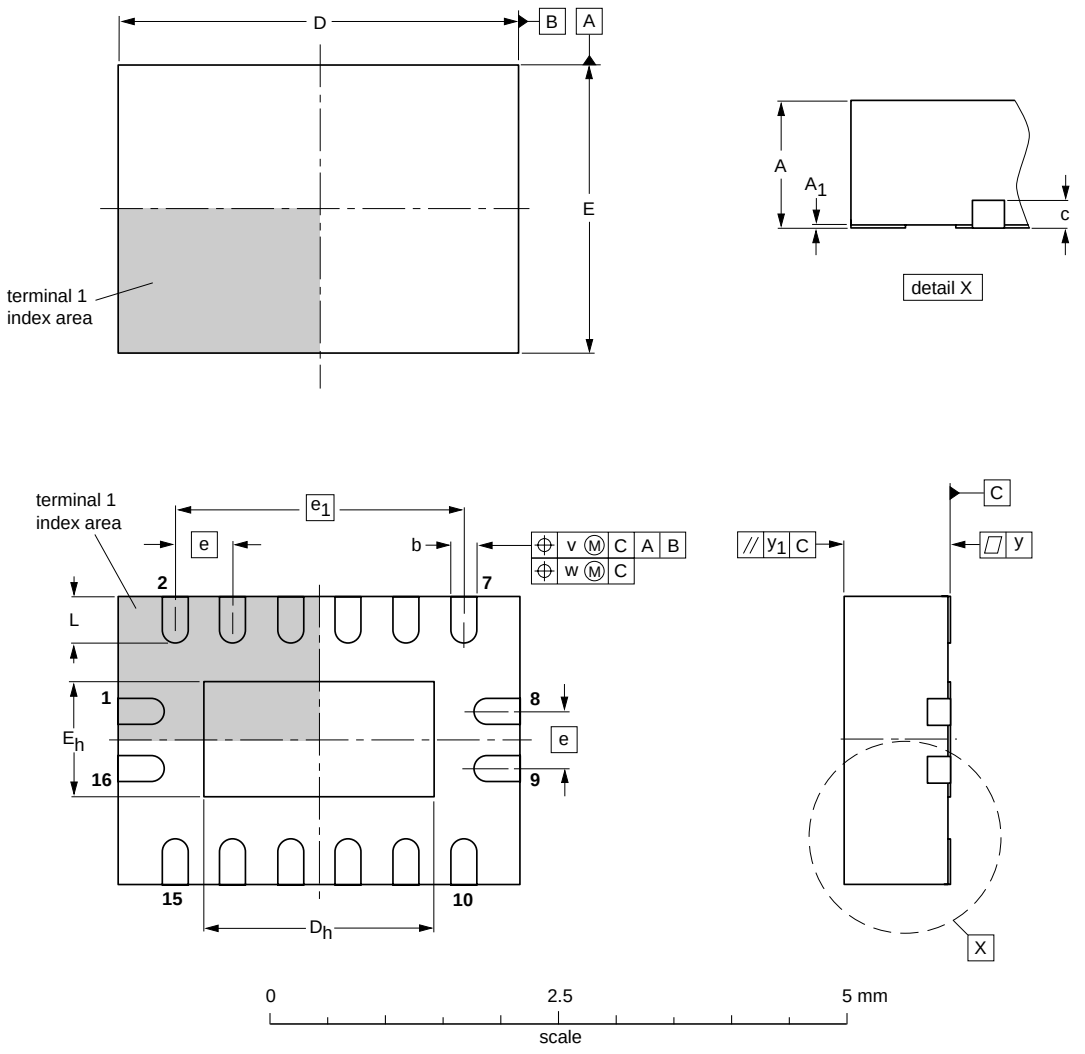
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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