DATA SHEET

74LVC1GX04
X-tal driver

Product specification

2003 Aug 13

Philips
Semiconductors

PHILIPS

X-tal driver 74LVC1GX04

FEATURES

- Wide supply voltage range from 1.65 to 5.5 V
- 5 V tolerant input and a 5 V overvoltage tolerant powered down output.
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 to 1.95 V)
  - JESD8-5 (2.3 to 2.7 V)
  - JESD8B/JESD36 (2.7 to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- SOT363 and SOT457 package
- ESD protection:
  - HBM EIA/JESD22-A114-A exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 to +85 °C and –40 to +125 °C.

DESCRIPTION

The 74LVC1GX04 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 and 5 V environment.

This device is fully specified for partial power-down applications using I_{off} at output Y. The I_{off} circuitry disables the output Y, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1GX04 combines the functions of the 74LVC1GU04 and 74LVC1G04 to provide a device optimized for use in crystal oscillator applications.

The integration of the two devices into the 74LVC1GX04 produces the benefits of a compact footprint, lower power dissipation and stable operation over a wide range of frequency and temperature.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input X1 to output X2	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	2.1	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	1.7	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.5	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.1	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	1.6	ns
	propagation delay input X1 to output Y	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	4.4	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.9	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	3.0	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.8	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	2.3	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance per buffer	output enabled; notes 1 and 2	35	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total load switching outputs;
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT	
X1	X2	Y
H	L	H
L	H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1GX04GW	–40 to +125 °C	6	TSSOP6	plastic	SOT363	VX
74LVC1GX04GV	–40 to +125 °C	6	TSSOP6	plastic	SOT457	VX4

PINNING

PIN	SYMBOL	DESCRIPTION
1	n.c.	not connected
2	GND	ground (0 V)
3	X1	data input
4	X2	data output
5	V_{CC}	supply voltage
6	Y	data output

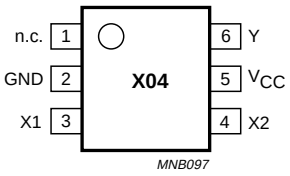


Fig.1 Pin configuration.

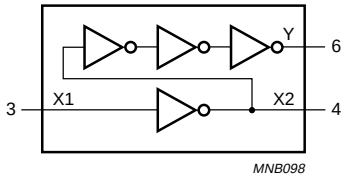


Fig.2 Logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	note 1	1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	note 2			
		active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 to 5.5 V	0	10	ns/V

Notes

1. For use of a regular crystal oscillator, the recommended minimum V_{CC} should be 2.0 V.
2. Only for output Y.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	V_I < 0	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0	–	±50	mA
V_O	output voltage	active mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 to +125 °C	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} Ω (V)				
T_{amb} = −40 to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		1.65 to 5.5	0.75 × V_{CC}	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 5.5	–	–	0.25 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 µA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.45	V
		I_O = 8 mA	2.3	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
		I_O = 32 mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 µA	1.65 to 5.5	V_{CC} − 0.1	–	–	V
		I_O = −4 mA	1.65	1.2	–	–	V
		I_O = −8 mA	2.3	1.9	–	–	V
		I_O = −12 mA	2.7	2.2	–	–	V
		I_O = −24 mA	3.0	2.3	–	–	V
		I_O = −32 mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	µA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; note 2	0	–	±0.1	±10	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	0.1	10	µA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC}Ω (V)				
T_{amb} = −40 to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 5.5	0.8 × V_{CC}	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 5.5	–	–	0.2 × V_{CC}	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.70	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −100 μA	1.65 to 5.5	V_{CC} − 0.1	–	–	V
		I_O = −4 mA	1.65	0.95	–	–	V
		I_O = −8 mA	2.3	1.7	–	–	V
		I_O = −12 mA	2.7	1.9	–	–	V
		I_O = −24 mA	3.0	2.0	–	–	V
		I_O = −32 mA	4.5	3.4	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±20	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V; note 2	0	–	–	±20	μA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; I_O = 0	5.5	–	–	40	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. V_O only for output Y.

AC CHARACTERISTICS

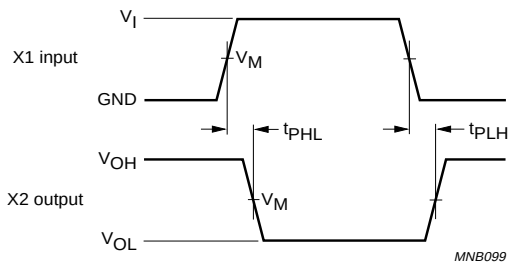
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay input X1 to output X2	see Figs 3 and 5	1.65 to 1.95	0.5	2.1	5.0	ns
			2.3 to 2.7	0.3	1.7	4.0	ns
			2.7	0.3	2.5	4.5	ns
			3.0 to 3.6	0.3	2.1	3.7	ns
			4.5 to 5.5	0.3	1.6	3.0	ns
	propagation delay input X1 to output Y	X2 no external load; see Figs 4 and 5	1.65 to 1.95	1.0	4.4	10.0	ns
			2.3 to 2.7	0.5	2.9	6.0	ns
			2.7	0.5	3.0	6.0	ns
			3.0 to 3.6	0.5	2.8	5.5	ns
			4.5 to 5.5	0.5	2.3	4.5	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay input X1 to output X2	see Figs 3 and 5	1.65 to 1.95	0.5	–	6.5	ns
			2.3 to 2.7	0.3	–	5.0	ns
			2.7	0.3	–	5.6	ns
			3.0 to 3.6	0.3	–	4.5	ns
			4.5 to 5.5	0.3	–	3.8	ns
	propagation delay input X1 to output Y	X2 no external load; see Figs 4 and 5	1.65 to 1.95	1.0	–	12.5	ns
			2.3 to 2.7	0.5	–	7.5	ns
			2.7	0.5	–	7.5	ns
			3.0 to 3.6	0.5	–	6.9	ns
			4.5 to 5.5	0.5	–	5.6	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

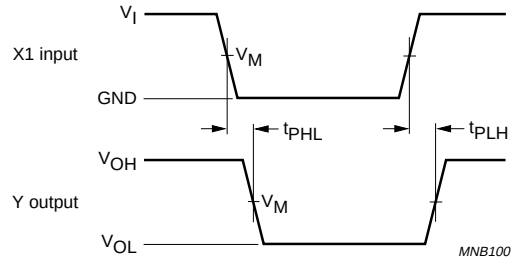
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

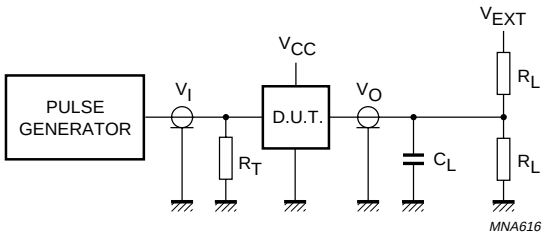
Fig.3 The input X1 to output X2 propagation delay.



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.3 to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 to 5.5 V	$0.5 \times V_{CC}$	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

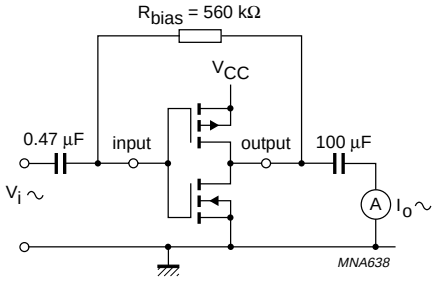
Fig.4 The input X1 to output Y propagation delay.



V_{CC}	V_I	C_L	R_L	V_{EXT}
				t_{PLH}/t_{PHL}
1.65 to 1.95 V	V_{CC}	30 pF	1 kΩ	open
2.3 to 2.7 V	V_{CC}	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 to 5.5 V	V_{CC}	50 pF	500 Ω	open

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

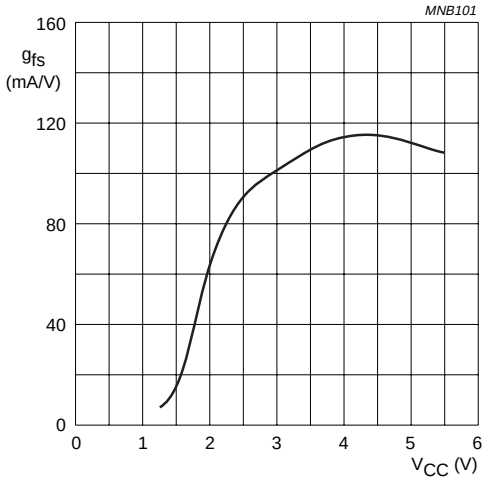
Fig.5 Load circuitry for switching times.



$$g_{fs} = \frac{\Delta I_o}{\Delta V_i}$$

f_i = 1 kHz.
V_O is constant.

Fig.6 Test set-up for measuring forward transconductance.



T_{amb} = 25 °C.

Fig.7 Typical forward transconductance as a function of supply voltage.

APPLICATION INFORMATION

Crystal controlled oscillator circuits are widely used in clock pulse generators because of their excellent frequency stability and wide operating frequency range. The use of the 74LVC1GX04 provides the additional advantages of low power dissipation, stable operation over a wide range of frequency and temperature and a very small footprint. This application information describes crystal characteristics, design and testing of crystal oscillator circuits based on the 74LVC1GX04.

Crystal Characteristics

Figure 8 is the equivalent circuit of a quartz crystal.

The reactive and resistive component of the impedance of the crystal alone and the crystal with a series and a parallel capacitance is shown in Figure 9.

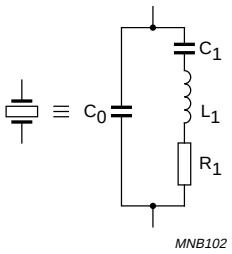
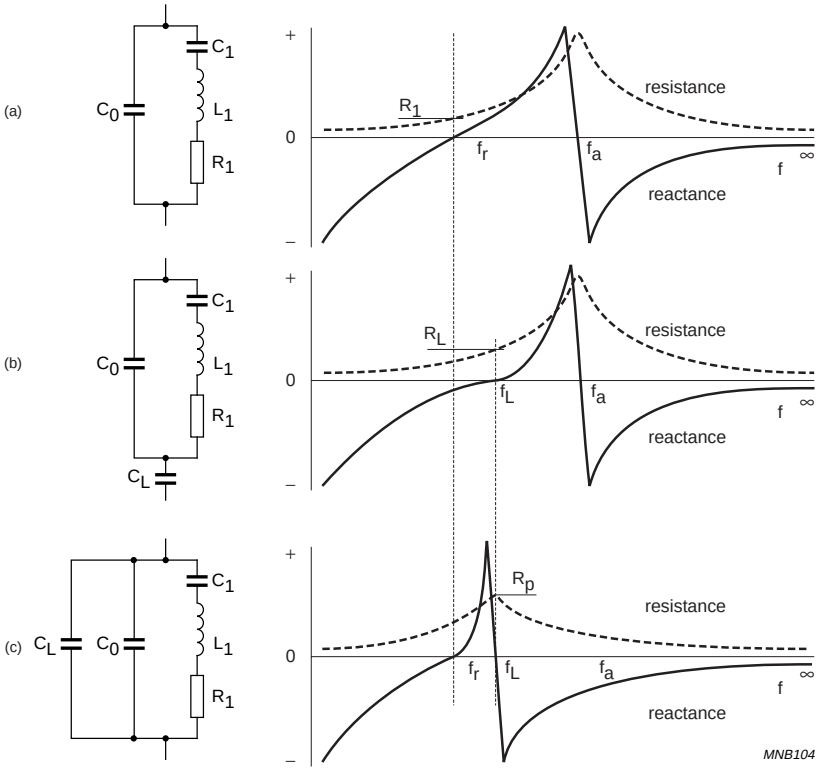


Fig.8 Equivalent circuit of a crystal.

Figure 9 also shows that with a specified load capacitance (C_L), the load resonance frequency (f_L) is the same for a circuit with either a series (b) or parallel (c) capacitance. C_L is specified by crystal manufacturers and is used in determining the value of the external components of the oscillator.



(a) resonance.
(b) anti-resonance.
(c) load resonance.

Fig.9 Reactance and resistance characteristics of a crystal.

Design

Figure 10 shows the recommended way to connect a crystal to the 74LVC1GX04. This circuit is basically a Pierce oscillator circuit in which the crystal is operating at its fundamental frequency and is tuned by the parallel load capacitance of C_1 and C_2. C_1 and C_2 are in series with the crystal. They should be approximately equal. R_1 is the drive-limiting resistor and is set to approximately the same value as the reactance of C_1 at the crystal frequency ($R_1 = X_{C1}$). This will result in an input to the crystal of 50% of the rail-to-rail output of X2. This keeps the drive level into the crystal within drive specifications (the designer should verify this). Overdriving the crystal can cause damage.

The resistor R_f provides negative feedback and sets a bias point of the inverter near mid-supply, operating the 74LVC1GU04 in the high gain linear region. The value of R_f is not critical, typically it is set at 1 MΩ.

To calculate the values of C_1 and C_2, the designer can use the formula: $C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_s$

C_L is the load capacitance as specified by the crystal manufacturer, C_s is the stray capacitance of the circuit (for the LVC1GX04 this is equal to an input capacitance of 5 pf).

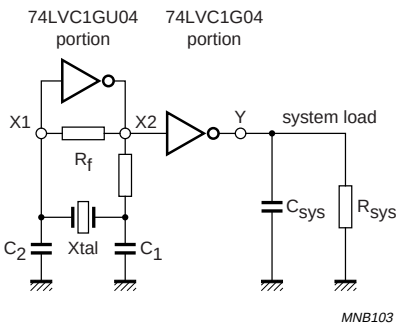


Fig.10 Crystal oscillator configuration.

Testing

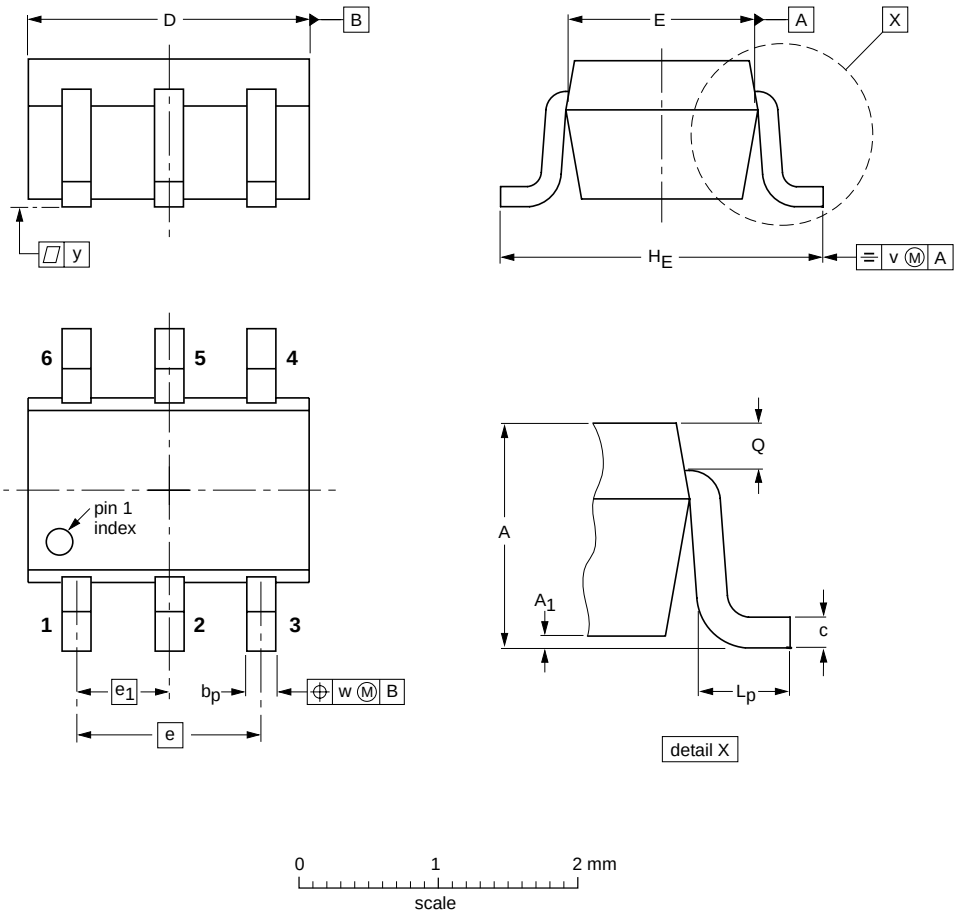
After the calculations are performed for a particular crystal, the oscillator circuit should be tested. The following simple checks will verify the prototype design of a crystal controlled oscillator circuit. Perform them after laying out the board:

- Test the oscillator over worst-case conditions (lowest supply voltage, worst-case crystal and highest operating temperature). Adding series and parallel resistors can simulate a worse case crystal.
- Insure that the circuit does not oscillate without the crystal.
- Check the frequency stability over a supply range greater than that which is likely to occur during normal operation.
- Check that the start up time is within system requirements.

As the 74LVC1GX04 isolates the system loading, once the design is optimized, the single layout may work in multiple applications for any given crystal.

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads **SOT363**

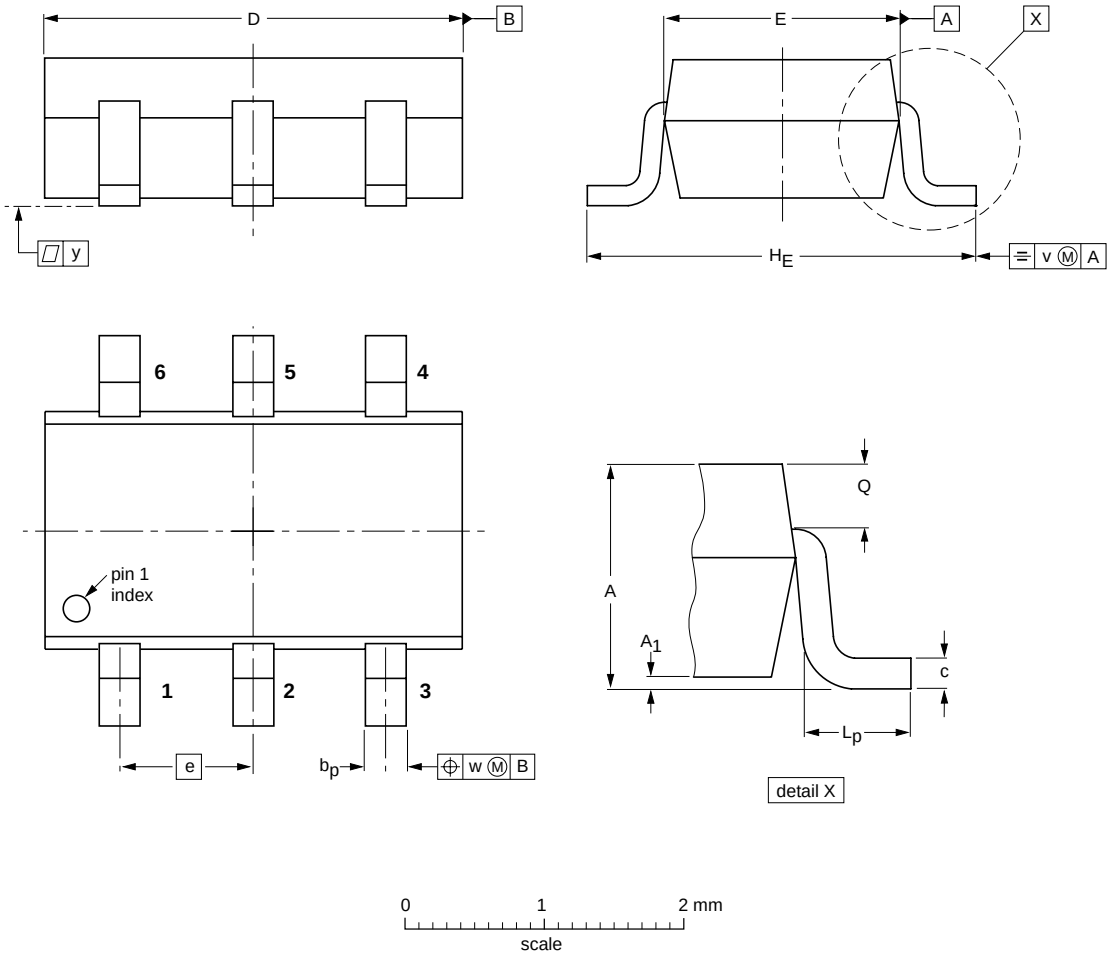


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Plastic surface mounted package; 6 leads **SOT457**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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