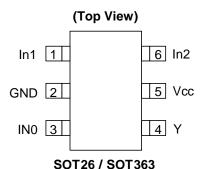
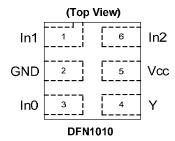


Description

The 74LVC1G98 is a single 3-input positive configurable multiple function gate with a standard totem pole output. The output state is determined by eight patterns of 3-bit input. The user can chose the logic functions MUX, AND, OR, NAND, NOR, inverter or non-inverting buffer. All inputs can be connected to ground or Vcc as required. The device is designed for operation with a power supply range of 1.65V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using IOFF. The IOFF circuitry disables the output preventing damaging current backflow when the device is powered down. The user is reminded that the device can simulate several types of logic gates but may respond differently due to the Schmitt action at the inputs.

Pin Assignments





Features

- Wide Supply Voltage Range from 1.65V to 5.5V
- ± 24mA Output Drive at 3.3V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Exceeds JESD 22
 - o 200-V Machine Model (A115-A)
 - o 2000-V Human Body Model (A114-A)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Range of Package Options
- SOT26, SOT363, and DFN1010: Available in "Green"
 Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Applications

- Voltage Level Shifting
- General Purpose Logic
- Power Down Signal Isolation
- Wide array of products such as:
- o PCs, networking, notebooks, netbooks, PDAs
- Computer peripherals, hard drives, CD/DVD ROM
- o TV, DVD, DVR, set top box
- Cell Phones, Personal Navigation / GPS
- o MP3 players ,Cameras, Video Recorders

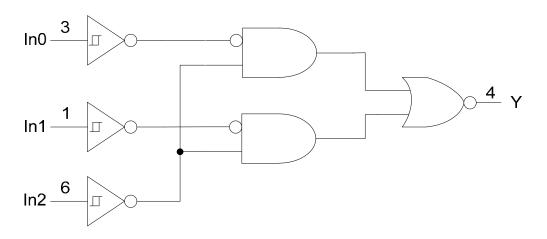
Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.



Pin Descriptions

Pin Name	Description			
ln1	Data Input			
GND	Ground			
In0	Data Input			
Y	Data Output			
Vcc	Supply Voltage			
ln2	Data Input			

Logic Diagram

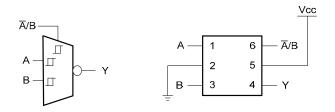


Function Table

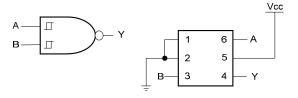
	Inputs		Output
ln2	ln1	In0	Y
L	L	L	Н
L	L	Н	Н
L	Н	L	L
L	Н	Н	L
Н	L	L	Н
Н	L	Н	L
Н	Н	L	Н
Н	Н	Н	L



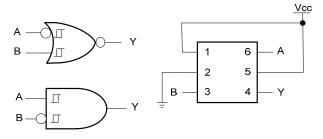
Logic Configurations



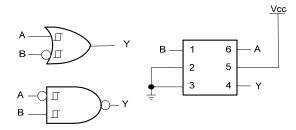
Configuration 1
2 to 1 Data Selector with Inverted Output



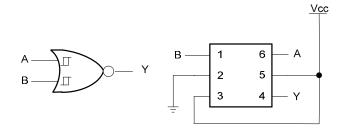
Configuration 2 2-Input NAND Gate 2-Input OR Gate with Both Inputs Inverted



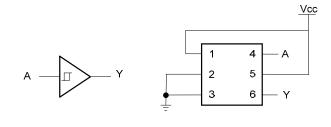
Configuration 3
2-Input NAND Gate with B Input Inverted
2-Input OR Gate with A Input Inverted



Configuration 4
2-Input OR Gate with One Input Inverted
2-Input NAND Gate with One Input Inverted



Configuration 5 2-Input NOR Gate



Configuration 6 Buffer

Function Selection Table						
Logic Function Configuration						
2-to-1 Data Selector with inverted output	1					
2-input NAND gate	2					
2-input AND with inverted input	3					
2-input NOR with inverted input	3					
2-input NAND with one inverted input	4					
2-input OR with one inverted input	4					
2-input NOR	5					
1-input Buffer	6					



Absolute Maximum Ratings (Note 2)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
V _{CC}	Supply Voltage Range	-0.5 to 6.5	V
VI	Input Voltage Range	-0.5 to 6.5	V
Vo	Voltage applied to output in high impedance or I _{OFF} state	-0.5 to 6.5	V
Vo	Voltage applied to output in high or low state	-0.3 to V _{CC} +0.5	V
I _{IK}	Input Clamp Current V _I <0	-50	mA
I _{OK}	Output Clamp Current	-50	mA
lo	Continuous output current	±50	mA
	Continuous current through Vdd or GND	±100	mA
TJ	Operating Junction Temperature	-40 to 150	°C
T _{STG}	Storage Temperature	-65 to 150	°C

Notes: 2. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

Recommended Operating Conditions (Note 3)

Symbol		Parameter	Min	Max	Unit
\/	Operating Voltage	Operating	1.65	5.5	V
V _{CC}	Operating Voltage	Data retention only	1.5		V
Vı	Input Voltage		0	5.5	V
Vo	Output Voltage		0	V _{CC}	V
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
I _{OH}	High-level output current	V _{CC} = 3 V		-16	mA
				-24	
		V _{CC} = 4.5 V		-32	
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
I _{OL}	Low-level output current	V 2V		16	mA
		$V_{CC} = 3 V$		24	
		V _{CC} = 4.5 V		32	
		V _{CC} = 1.8 V ± 0.15V, 2.5 V ± 0.2 V		20	
Δt/ΔV	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature		-40	125	°C

Notes: 3. Unused inputs should be held at Vcc or Ground.



Electrical Characteristics $T_A=-40$ °C to 85 °C (All typical values are at Vcc = 3.3V, $T_A=25$ °C)

Symbol	Parameter	Test Conditions	V _{cc}	Min	Тур.	Max	Unit
			1.65 V	0.70		1.20	
			2.3V	1.11		1.60	
V_{T+}	Positive-going input threshold voltage		3 V	1.50		2.00	
	Tilleshold voltage		4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
			1.65 V	0.30		0.72	
			2.3V	0.58		1.00	
V_{T-}	Negative-going input threshold voltage		3 V	0.80		1.30	
	Tilleshold voltage		4.5 V	1.21		1.95	
			5.5 V	1.45		2.35	
			1.65 V	0.30		0.62	
			2.3V	0.40		0.80	
ΔV_{T}	Hysteresis (V _{T+} - V _{T-)}		3 V	0.35		1.00	
	(VI+- VI-)		4.5 V	0.55		1.10	
			5.5 V	0.60		1.20	
	V High Lovel Output Voltage	$I_{OH} = -100 \mu A$	1.65 V to 5.5V	V _{CC} - 0.1			
		I _{OH} = -4mA	1.65 V	1.2			
\/		I _{OH} = -8mA	2.3V	1.9			V
V_{OH}	High Level Output Voltage	I _{OH} = -16mA	2.1/	2.4			T V
		I _{OH} = -24mA	3 V	2.3			
		I _{OH} = -32mA	4.5 V	3.8			
		$I_{OL} = 100 \mu A$	1.65 V to 5.5V			0.1	
		I _{OL} = 4mA	1.65 V			0.45	
\/	High lovel lanut Voltage	I _{OL} = 8mA	2.3V			0.3	V
V_{OL}	High-level Input Voltage	I _{OL} = 16mA	2.1/			0.4	V
		I _{OL} = 24mA	3 V			0.55	
		$I_{OL} = 32mA$	4.5			0.55	
Ι _Ι	Input Current	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V			± 5	μA
I _{OFF}	Power Down Leakage Current	V_1 or $V_0 = 5.5V$	0			± 10	μA
I _{CC}	Supply Current	$V_1 = 5.5V$ of GND $I_0=0$	1.65 V to 5.5V			10	μA
Δl _{CC}	Additional Supply Current	One input at V _{CC} –0.6 V Other inputs at V _{CC} or GND	3 V to 5.5V			500	μΑ



Electrical Characteristics $T_A = -40 \,^{\circ}\text{C}$ to 125 $^{\circ}\text{C}$ (All typical values are at Vcc = 3.3V, $T_A = 25 \,^{\circ}\text{C}$)

Symbol	Parameter	Test Conditions	Vcc	Min	Тур.	Max	Unit
			1.65 V	0.70		1.20	
			2.3V	1.11		1.60	
V_{T+}	Positive-going input threshold voltage		3 V	1.50		2.00	
	threshold voltage		4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
			1.65 V	0.30		0.75	
			2.3V	0.58		1.03	
V_{T-}	Negative-going input		3 V	0.80		1.33	
	threshold voltage		4.5 V	1.21		1.95	
			5.5 V	1.45		2.35	
			1.65 V	0.30		0.62	
			2.3V	0.37		0.80	
ΔV_T	Hysteresis		3 V	0.32		1.00	
	(V _{T+} - V _{T-)}		4.5 V	0.50		1.20	
			5.5 V	0.55		1.40	
		I _{OH} = -100μA	1.65 V to 5.5V	V _{CC} - 0.1		1110	
		I _{OH} = -4mA	1.65 V	0.95			
		I _{OH} = -8mA	2.3V	1.7			
V_{OH}	High Level Output Voltage	I _{OH} = -16mA		1.9			V
		$I_{OH} = -24\text{mA}$	3 V	2.0			
		$I_{OH} = -32\text{mA}$	4.5 V	3.4			
		$I_{OL} = 100 \mu A$	1.65 V to 5.5V			0.1	
		I _{OL} = 4mA	1.65 V			0.7	
		$I_{OL} = 8mA$	2.3V			0.45	
V_{OL}	High-level Input Voltage	I _{OL} = 16mA				0.6	V
		$I_{OL} = 24\text{mA}$	3 V			0.8	
		$I_{OL} = 32\text{mA}$	4.5			0.8	
l _l	Input Current	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V			± 100	μA
	Power Down Leakage	V_1 or $V_0 = 5.5V$					
I _{OFF}	Current	1, 21, 10	0			± 200	μA
I _{CC}	Supply Current	V _I = 5.5V of GND I _O =0	1.65 V to 5.5V			200	μΑ
ΔI _{CC}	Additional Supply Current	One input at V _{CC} –0.6 V Other inputs at V _{CC} or GND	3 V to 5.5V			5000	μΑ
Ci	Input Capacitance	$V_i = V_{CC} - or GND$	3.3		3.5		pF
		SOT26	(Note 4)		166		
θ_{JA}	Thermal Resistance	SOT363	(Note 4)		333		°C/V
- 77	Junction-to-Ambient	DFN1010	(Note 4)		231		1
		SOT26	(Note 4)		46		
Δ.	Thermal Resistance		` '				°C/V
θ_{JC}	Junction-to-Case	SOT363	(Note 4)		102		L/V
		DFN1010	(Note 4)		TBD		

Notes: 4. Test condition for SOT26, SOT363 and DFN1010 : Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



Switching Characteristics

T_A=-40 °C to 85 °C, CL = 30 or 50pF as noted (see Figure 1)

Parameter	From	то		1.8 V .15V	Vcc = ± 0	2.5 V 0.2V	Vcc = ± 0	3.3 V .3V		= 5 V).5V	Unit
	(Input)	(OUTPUT)	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	Any	Y	1.0	14.4	0.7	8.3	0.7	6.3	0.7	5.1	ns

 T_A =-40 °C to 125 °C, CL = 30 or 50pF as noted (see Figure 1)

Parameter	From	то		: 1.8 V .15V		2.5 V).2V	Vcc = ± 0	3.3 V 3.3 V		= 5 V).5V	Unit
	(Input)	(OUTPUT)	Min	Max	Min	Max	Min	Max	Min	Max	
t _{pd}	Any	Y	1.0	18.0	0.7	10.4	0.7	7.9	0.7	6.4	ns

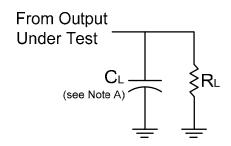
Operating Characteristics

 $T_A = 25$ °C

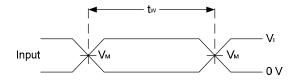
	Parameter	Test Conditions	Vcc = 1.8 V	Vcc = 2.5 V	Vcc = 3.3 V	Vcc = 5 V	Unit
C _{pd}	Power dissipation capacitance	f = 10 MHz	22	22	23	24	pF



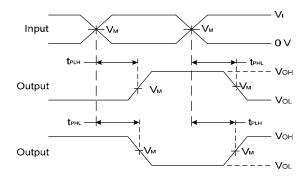
Parameter Measurement Information



Vcc	Inputs		V _M	C _L	RL
	VI	t _r /t _f			
1.8V±0.15V	Vcc	≤2ns	V _{CC} /2	30pF	1ΚΩ
2.5V±0.2V	V _{cc}	≤2ns	V _{CC} /2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	50pF	500Ω



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

Notes: A. Includes test lead and test apparatus capacitance.

B. All pulses are supplied at pulse repetition rate ≤ 10 MHz

- C. Inputs are measured separately one transition per measurement
- D. t_{PLH} and t_{PHL} are the same as t_{PD}

Figure 1. Load Circuit and Voltage Waveforms



Ordering Information

T4LVC1G 98 XXX - 7

Logic Device Function Package Packing

74 : Logic Prefix 98 : 3-Input W6 : SOT26 7 : Tape & Reel

LVC : 1.65 to 5.5V Configurable DW : SOT363
Family Multiple-Function FW4 : DFN1010

1G : One gate Gate

	Dovice	Device Package Packaging		7" Tape and Reel			
	Device	Code	(Note 7)	Quantity	Part Number Suffix		
Pb ,	74LVC1G98W6-7	W6	SOT26	3000/Tape & Reel	-7		
PD ,	74LVC1G98DW-7	DW	SOT363	3000/Tape & Reel	-7		
Pb ,	74LVC1G98FW4-7	FW4	DFN1010	5000/Tape & Reel	-7		

Notes: 7. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.



Marking Information

(1) SOT26, SOT363

6 5 4

XXYWX

3 2

XX: Identification code

Y: Year 0~9

W: Week: A~Z: 1~26 week;

a~z: 27~52 week; z represents

52 and 53 week

X: A~Z: Internal Code

Part Number	Package	Identification Code
74LVC1G98W6	SOT26	TZ
74LVC1G98DW	SOT363	TZ

(2) DFN1010

(Top View)

XX XX: Identification Code

Ÿ: Year : 0~9

\overline{\tilde{W}}: Week: A~Z: 1~26 week; a~z: 27~52 week; z represents

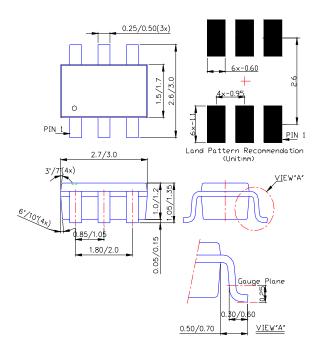
52 and 53 week X: A~Z: Internal code

Part Number	Package	Identification Code
74LVC1G98FW4	DFN1010	TZ

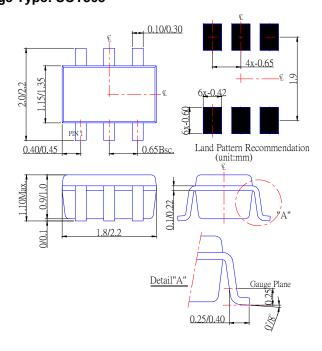


Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT26



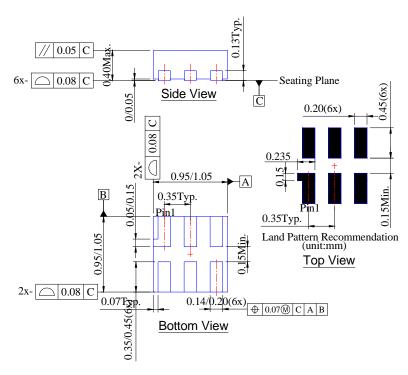
(2) Package Type: SOT363





Package Outline Dimensions (All Dimensions in mm)

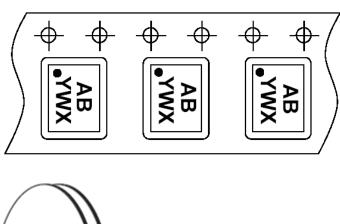
(3) Package Type: DFN1010

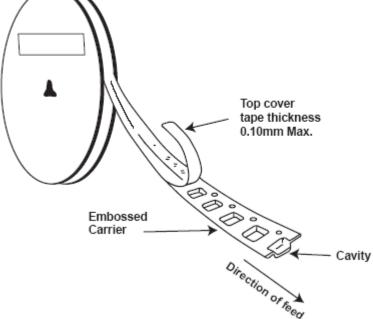




Taping Orientation (Note 8)

For DFN1010





Notes: 8. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf



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