

# DATA SHEET

# NEC

## SILICON POWER MOS FET NE5520379A

### 3.2 V OPERATION SILICON RF POWER LDMOS FET FOR GSM/DCS DUAL-BAND PHONE TRANSMISSION AMPLIFIERS

#### DESCRIPTION

The NE5520379A is an N-channel silicon power MOS FET specially designed as the transmission power amplifier for 3.2 V GSM 900 handsets. Dies are manufactured using our NEWMOS technology and housed in a surface mount package. This device can deliver 34.6 dBm output power with 68% power efficiency at 915 MHz under the 2.8 V supply voltage.

#### FEATURES

- High output power :  $P_{out} = 35.5$  dBm TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 915$  MHz,  $P_{in} = 25$  dBm)  
:  $P_{out} = 33.0$  dBm TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 1785$  MHz,  $P_{in} = 25$  dBm)
- High power added efficiency :  $\eta_{add} = 65\%$  TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 915$  MHz,  $P_{in} = 25$  dBm)  
:  $\eta_{add} = 35\%$  TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 1785$  MHz,  $P_{in} = 25$  dBm)
- High linear gain :  $G_L = 16.0$  dB TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 915$  MHz,  $P_{in} = 10$  dBm)  
:  $G_L = 8.5$  dB TYP. ( $V_{DS} = 3.2$  V,  $V_{GS} = 2.5$  V,  $f = 1785$  MHz,  $P_{in} = 10$  dBm)
- Surface mount package :  $5.7 \times 5.7 \times 1.1$  mm MAX.
- ★ • Single supply :  $V_{DS} = 2.8$  to  $6.0$  V

#### APPLICATIONS

- Digital cellular phones : 3.2 V GSM/DCS Dual-Band handsets
- Others : General purpose amplifiers for 1.6 to 2.0 GHz TDMA applications

#### ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE5520379A-T1	79A	A3	• 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 1 kpcs/reel
NE5520379A-T1A			• 12 mm wide embossed taping • Gate pin face the perforation side of the tape • Qty 5 kpcs/reel

**Remark** To order evaluation samples, contact your nearby sales office.

Part number for sample order: NE5520379A

**Caution** Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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Not all devices/types available in every country. Please check with local NEC Compound Semiconductor Devices representative for availability and additional information.

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C)**

Parameter	Symbol	Ratings	Unit
★ Drain to Source Voltage	V <sub>DS</sub>	15.0	V
Gate to Source Voltage	V <sub>GS</sub>	5.0	V
Drain Current	I <sub>D</sub>	1.5	A
Drain Current (Pulse Test)	I <sub>D</sub> <sup>Note</sup>	3.0	A
Total Power Dissipation	P <sub>tot</sub>	20	W
Channel Temperature	T <sub>ch</sub>	125	°C
Storage Temperature	T <sub>stg</sub>	-65 to +125	°C

**Note** Duty Cycle ≤ 50%, T<sub>on</sub> ≤ 1 s

**RECOMMENDED OPERATING CONDITIONS**

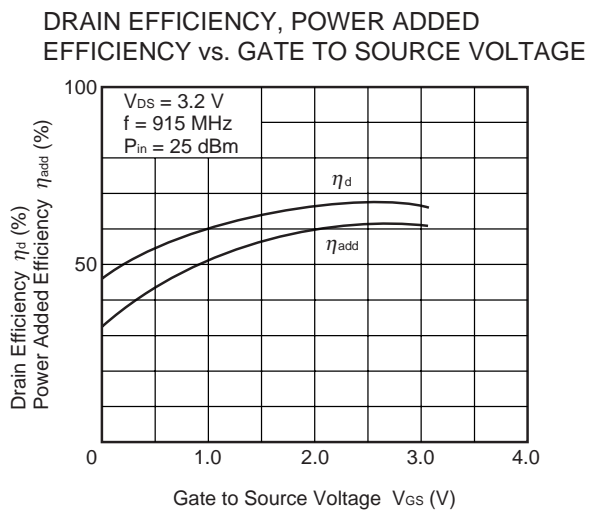
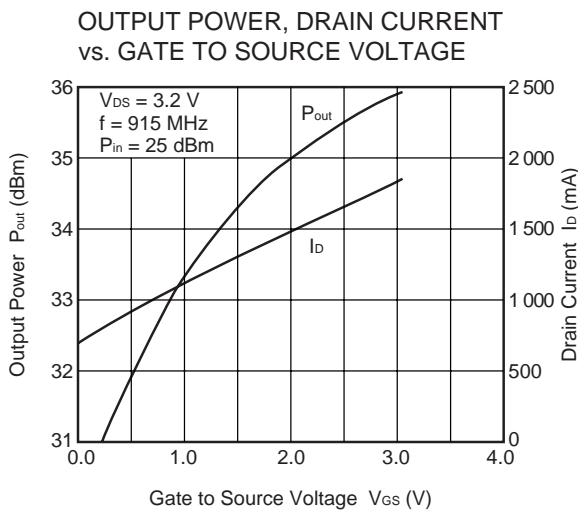
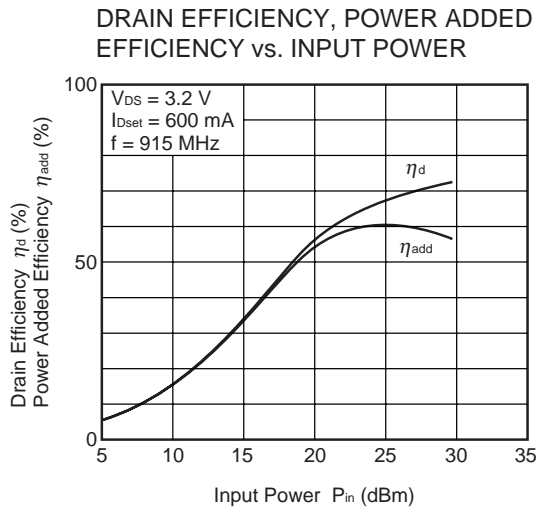
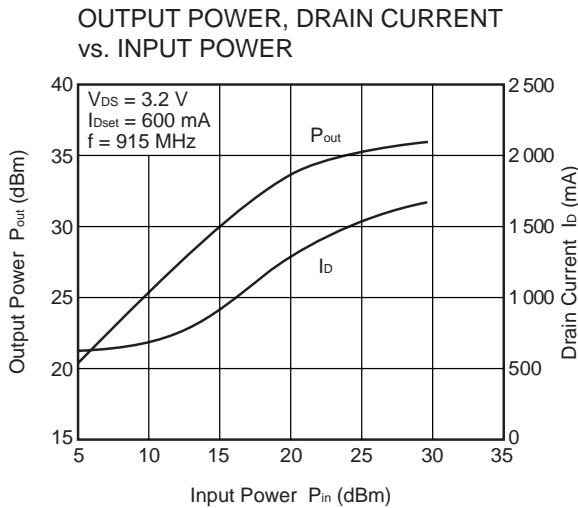
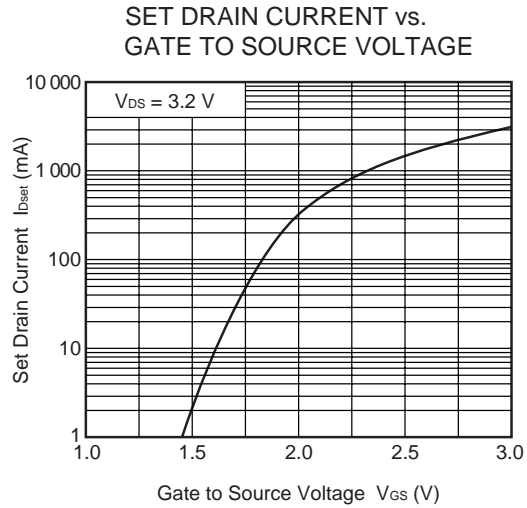
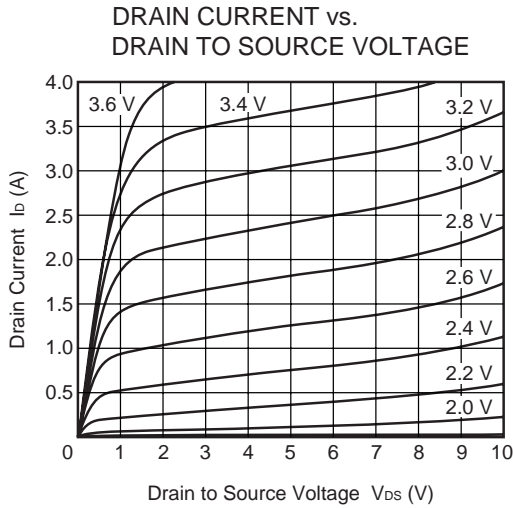
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
★ Drain to Source Voltage	V <sub>DS</sub>		2.8	3.2	6.0	V
Gate to Source Voltage	V <sub>GS</sub>		0	2.5	3.5	V
Drain Current (Pulse Test)	I <sub>D</sub>	Duty Cycle ≤ 50%, T <sub>on</sub> ≤ 1 s	–	1.75	2.0	A
Input Power	P <sub>in</sub>	f = 1.8 GHz, V <sub>DS</sub> = 3.6 V	24	25	26	dBm

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25°C)

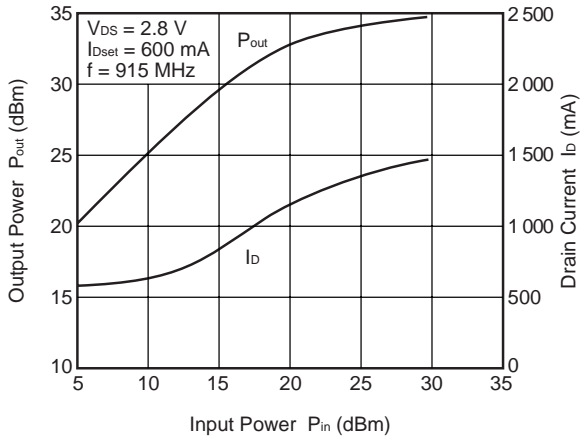
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
★ Gate to Source Leak Current	I <sub>GSS</sub>	V <sub>GS</sub> = 6.0 V	–	–	100	nA
★ Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	I <sub>DSS</sub>	V <sub>DS</sub> = 8.5 V	–	–	100	nA
Gate Threshold Voltage	V <sub>th</sub>	V <sub>DS</sub> = 3.5 V, I <sub>D</sub> = 1 mA	1.0	1.35	2.0	V
Transconductance	G <sub>m</sub>	V <sub>DS</sub> = 3.5 V, I <sub>D</sub> = 0.8 to 1.0 A	–	2.5	–	S
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>DSS</sub> = 10 μA	15	20	–	V
Thermal Resistance	R <sub>th</sub>	Channel to Case	–	–	5	°C/W
Linear Gain	G <sub>L</sub>	f = 915 MHz, P <sub>in</sub> = 10 dBm, V <sub>DS</sub> = 3.2 V, V <sub>GS</sub> = 2.5 V, <b>Note</b>	–	16.0	–	dB
Output Power	P <sub>out</sub>	f = 915 MHz, P <sub>in</sub> = 25 dBm, V <sub>DS</sub> = 3.2 V, V <sub>GS</sub> = 2.5 V, <b>Note</b>	–	35.5	–	dBm
Drain Efficiency	η <sub>d</sub>		–	68	–	%
Power Added Efficiency	η <sub>add</sub>		–	65	–	%
Linear Gain	G <sub>L</sub>	f = 1 785 MHz, P <sub>in</sub> = 10 dBm, V <sub>DS</sub> = 3.2 V, V <sub>GS</sub> = 2.5 V, <b>Note</b>	–	8.5	–	dB
Output Power	P <sub>out</sub>	f = 1 785 MHz, P <sub>in</sub> = 25 dBm, V <sub>DS</sub> = 3.2 V, V <sub>GS</sub> = 2.5 V, <b>Note</b>	31.0	33.0	–	dBm
Drain Efficiency	η <sub>d</sub>		29	38	–	%
Power Added Efficiency	η <sub>add</sub>		–	35	–	%

**Note** DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

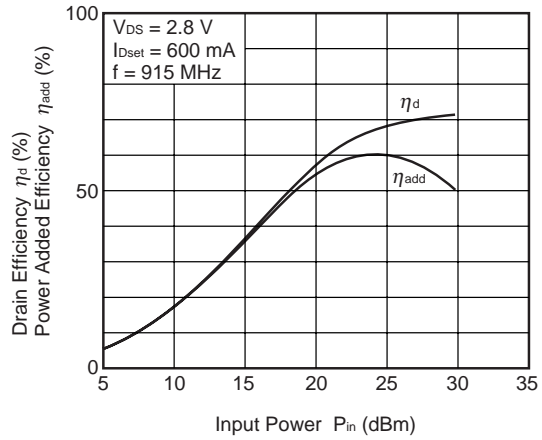
★ TYPICAL CHARACTERISTICS (T<sub>A</sub> = +25°C)



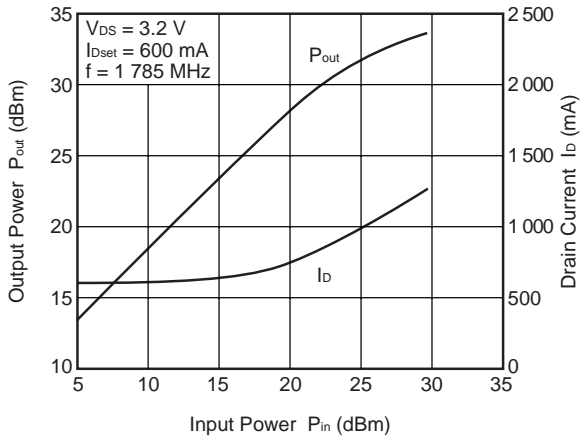
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER (915 MHz)



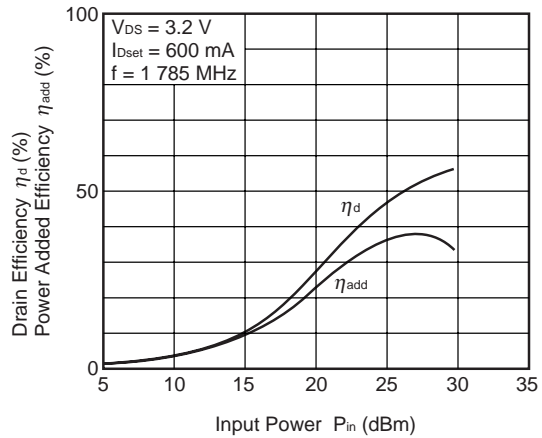
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



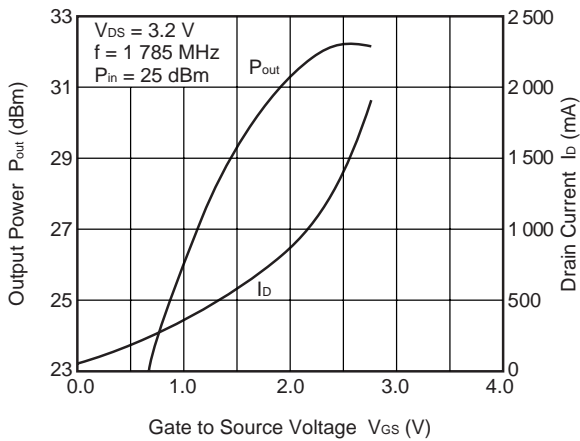
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER (1 785 MHz)



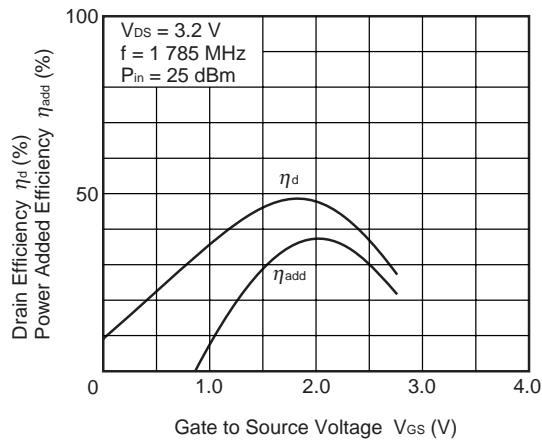
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



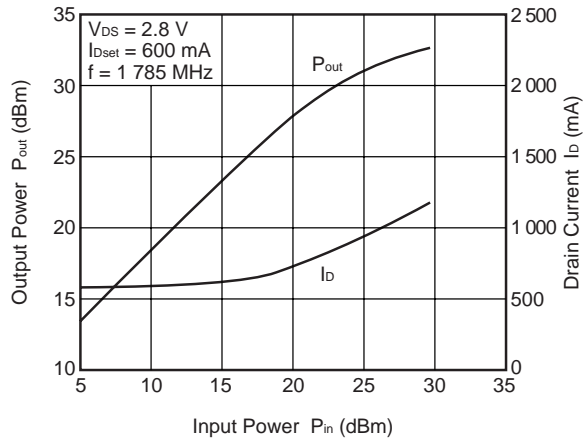
OUTPUT POWER, DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE



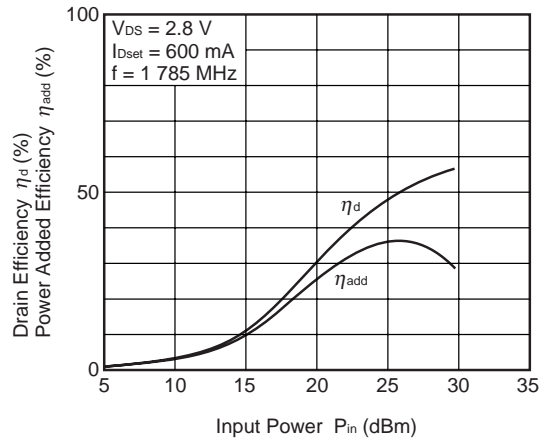
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. GATE TO SOURCE VOLTAGE



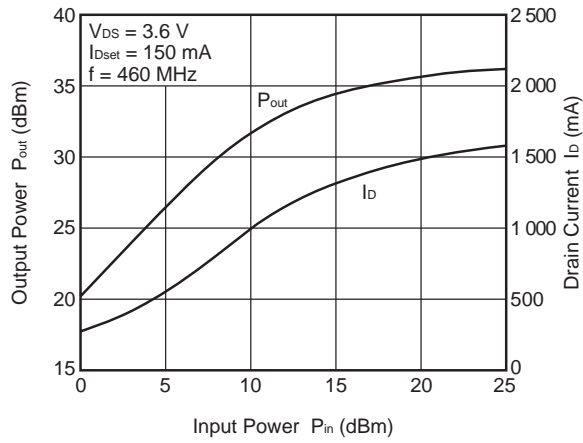
OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER (1 785 MHz)



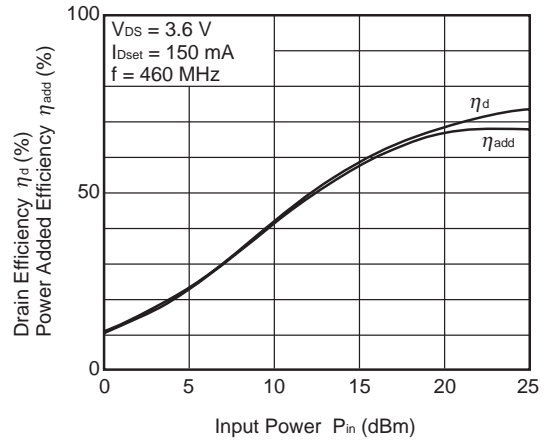
DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER (460 MHz)



DRAIN EFFICIENCY, POWER ADDED EFFICIENCY vs. INPUT POWER



**Remark** The graphs indicate nominal characteristics.

**S-PARAMETERS**

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

[RF and Microwave] → [Device Parameters]

URL <http://www.csd-nec.com/>

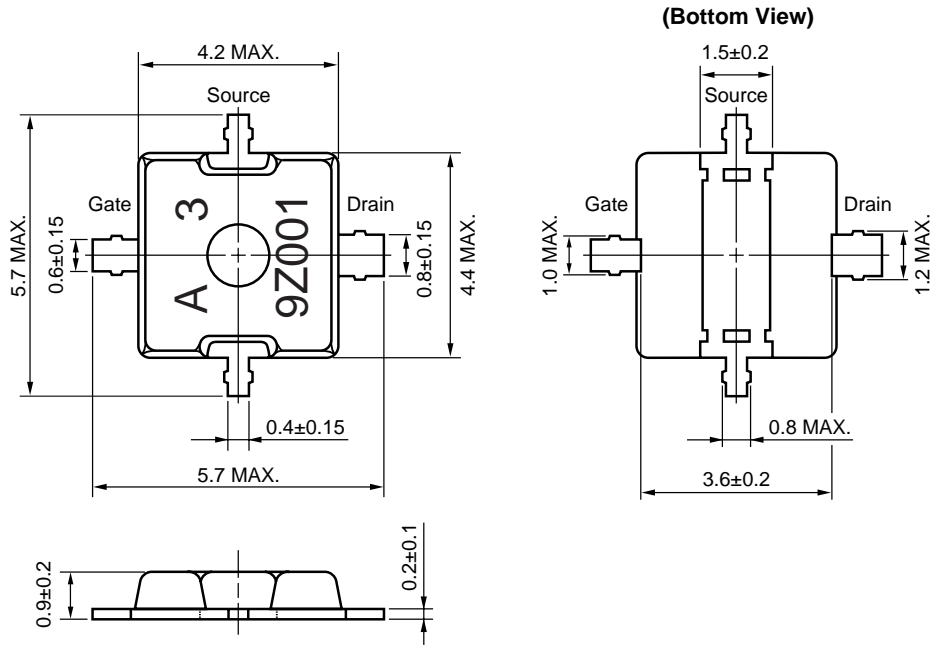
**LARGE SIGNAL IMPEDANCE ( $V_{DS} = 3.2\text{ V}$ ,  $I_{Dset} = 600\text{ mA}$ ,  $P_{in} = 25\text{ dBm}$ )**

f (MHz)	$Z_{in}$ ( $\Omega$ )	$Z_{OL}$ ( $\Omega$ ) <sup>Note</sup>
1 785	TBD	TBD

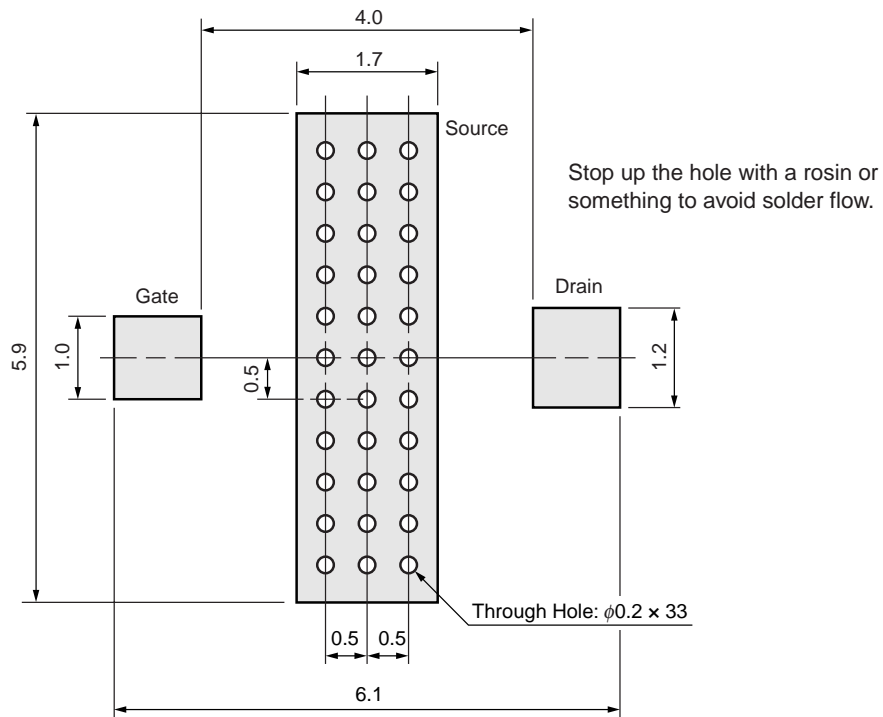
**Note**  $Z_{OL}$  is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.

★ PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)





**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol
Infrared Reflow	Peak temperature (package surface temperature) : 260°C or below Time at peak temperature : 10 seconds or less Time at temperature of 220°C or higher : 60 seconds or less Preheating time at 120 to 180°C : 120±30 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) : 215°C or below Time at temperature of 200°C or higher : 25 to 40 seconds Preheating time at 120 to 150°C : 30 to 60 seconds Maximum number of reflow processes : 3 times Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) : 260°C or below Time at peak temperature : 10 seconds or less Preheating temperature (package surface temperature) : 120°C or below Maximum number of flow processes : 1 time Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) : 350°C or below Soldering time (per pin of device) : 3 seconds or less Maximum chlorine content of rosin flux (% mass) : 0.2%(Wt.) or below	HS350-P3

**Caution Do not use different soldering methods together (except for partial heating).**

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