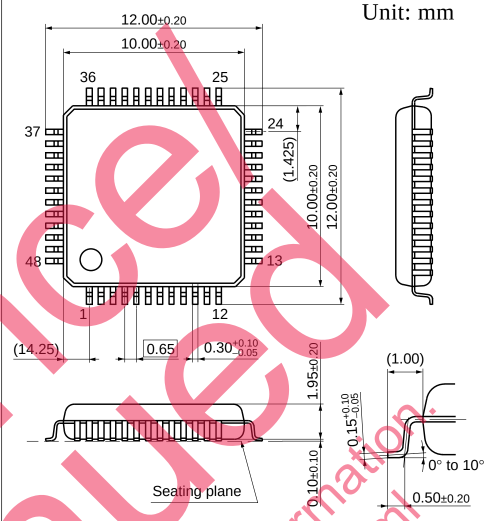
AN8934FA

Video signal processing and QPSK demodulation IC for BS/CS broadcasting

■ Overview

The AN8934FA is a single chip IC integrating video signal processing, QPSK demodulation, changeover switches of detection and bit-stream signals for BS/CS broadcasting.



QFP048-P-1010C

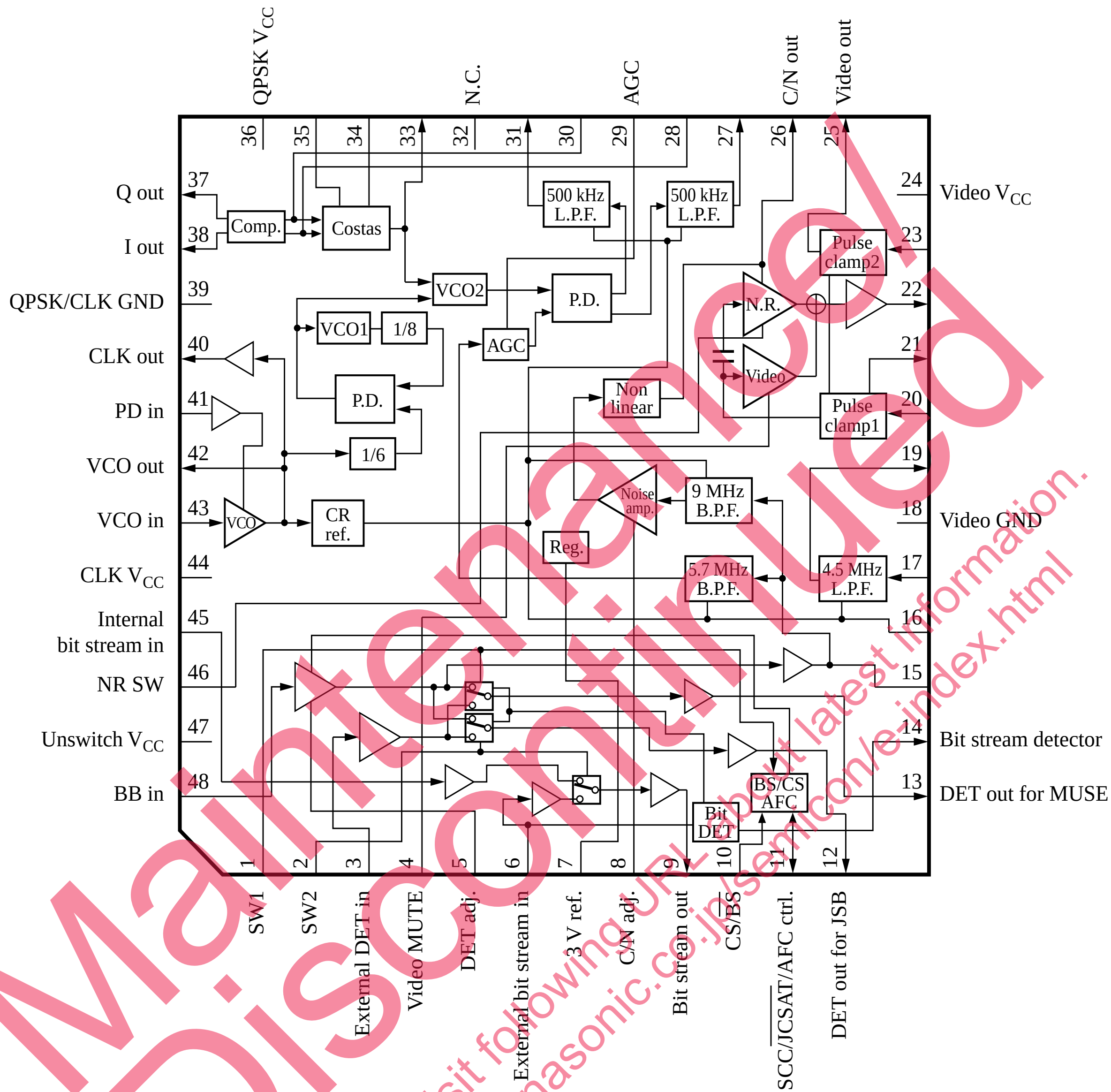
■ Features

- 4.5 MHz L.P.F. for video and 5.7 MHz B.P.F. for sound built-in
- C/N detection circuit built-in
- Changeover between external input and internal signal of detection and bit-stream signals
- 2 systems of detection output (capable of 75 Ω drive) and 1 system of bit-stream output (capable of 75 Ω drive)
- Bit-stream signal detection circuit of external input built-in
- One crystal for base band signal processing block due to a joint use with PCM processing IC MN88831. (18.432 MHz)

■ Applications

- BS/CS tuner built-in TV and VCR

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Detection output changeover 1	10	BS/CS mode changeover
2	Detection output changeover 2	11	CS mode changeover / AFC control
3	External detection signal input	12	Detection output 1
4	Video output mute	13	Detection output 2
5	Input amp. gain adjustment	14	Bit-stream detection
6	External bit-stream input	15	Detection output 3
7	Reference voltage	16	Filter reference
8	C/N detection voltage adjustment	17	4.5 MHz L.P.F. input
9	Bit-stream output	18	GND (Video system)

■ Pin Descriptions (continued)

Pin No.	Description	Pin No.	Description
19	4.5 MHz L.P.F. output	34	Costus output (+)
20	Pulse clamp input 1	35	Costus output (−)
21	Pulse clamp reference	36	Supply voltage (QPSK)
22	Video amp. output	37	Data output Q
23	Pulse clamp input 2	38	Data output I
24	Supply voltage (Video system)	39	GND (QPSK·clock)
25	Video signal output	40	Data clock output
26	C/N detection voltage output	41	Data lock phase error voltage input
27	Eye-pattern output Q	42	Data clock VCO output
28	Eye-pattern input Q	43	Data clock VCO input
29	QPSK AGC	44	Supply voltage (clock)
30	Eye-pattern input I	45	Internal bit-stream input
31	Eye-pattern output I	46	Noise reduction switch
32	N.C.	47	Supply voltage (input amp.)
33	VCO phase error voltage output	48	Internal detection signal input

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.7	V
Supply current	I_{CC}	136	mA
Power dissipation *2	P_D	431	mW
Operating ambient temperature *1	T_{opr}	−20 to +85	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: The power dissipation shown is the value for T_a = 80°C. For the independent IC without a heat sink.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.5 to 5.5	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{TOT}	No signal, all of V_{CC} are 5 V	60	92	120	mA
Standby current	I_{STD}	No signal, V_{CC} (pin 47) = 5 V, other V_{CC} (pin 24, 36, 44) = 0 V	20	33	41	mA
Input amp. gain Int.1	G_{12A1}	Input is pin 48 (V_{IN48} = 0.7 V[p-p], 1 MHz) Output is pin 12 (V_{IN6} = 0.5 V[p-p], 2 MHz square-wave)	7	8.5	10	dB
Input amp. gain Int.2	ΔG_{12A2}	V_{IN48} = 0.7 V[p-p], 8.5 MHz Difference from G_{12A1} (V_{IN6} = 0.5 V[p-p], 2 MHz square-wave)	– 0.8	– 0.3	0.2	dB
Input amp. gain Int.3	ΔG_{12A3}	V_{IN48} = 0.7 V[p-p], 1 MHz (18 MHz) Difference from G_{12A1} (V_{IN6} = 0.5 V[p-p], 2 MHz square-wave)	– 0.8	– 0.5	– 0.2	dB
Input amp. gain Int.4	ΔG_{12A4}	V_{IN48} = 0.7 V[p-p], 1 MHz (15.8 MHz) Difference from G_{12A1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	0.34	0.64	0.94	dB
Input amp. gain Int.5	ΔG_{12A5}	V_{IN48} = 0.7 V[p-p], 1 MHz (min.) Difference from G_{12A1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	—	–30	–10	dB
Input amp. gain Int.6	ΔG_{12A6}	V_{IN48} = 0.7 V[p-p], 1 MHz Difference from G_{12A1} (V_{IN6} = no input)	–1	0	1	dB
Input amp. gain Int.7	ΔG_{13A1}	V_{IN48} = 0.7 V[p-p], 1 MHz, Output is pin 13 Difference from G_{12A1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	–1	0	1	dB
Input amp. gain Int.8	ΔG_{13A2}	V_{IN48} = 0.7 V[p-p], 1 MHz, Output is pin 13 Difference from G_{12A1} (V_{IN6} = no input)	–1	0	1	dB
Input amp. gain Int.9	$\Delta G_{15(1)}$	V_{IN48} = 0.7 V[p-p], 1 MHz, Output is pin 15 Difference from G_{12A1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	–1	0	1	dB
Input amp. gain Ext.1	G_{12B1}	Input is pin 3 (V_{IN3} = 0.7 V[p-p], 1 MHz) Output is pin 12 (V_{IN6} = 0.5 V[p-p], 2 MHz square-wave)	5	6	7	dB
Input amp. gain Ext.2	ΔG_{12B2}	V_{IN3} = 0.7 V[p-p], 8.5 MHz Difference from G_{12B1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	– 0.8	– 0.3	0.2	dB
Input amp. gain Ext.3	ΔG_{13B1}	V_{IN3} = 0.7 V[p-p], 1 MHz, Output is pin 13 Difference from G_{12B1} (V_{IN6} = 0.5V[p-p], 2 MHz square-wave)	–1	0	1	dB
4.5MHz L.P.F. gain 1	$G_{19(1)}$	V_{IN17} = 0.4 V[p-p], 0.1 MHz	–1	– 0.3	0.4	dB
4.5MHz L.P.F. frequency characteristic 1	$\Delta G_{19(1)}$	V_{IN17} = 0.4 V[p-p], 2.5 MHz Difference from $G_{19(1)}$	–2.2	–1.5	– 0.8	dB
4.5MHz L.P.F. frequency characteristic 2	$\Delta G_{19(2)}$	V_{IN17} = 0.4 V[p-p], 4.2 MHz Difference from $G_{19(1)}$	–5.5	–3.5	–1	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
4.5MHz L.P.F. frequency characteristic 3	$\Delta G_{19(3)}$	V_{IN17} = 0.4 V[p-p], 4.5 MHz Difference from $G_{19(1)}$	–8.5	–4	–1	dB
4.5MHz L.P.F. frequency characteristic 4	$\Delta G_{19(4)}$	V_{IN17} = 0.4 V[p-p], 5.73 MHz Difference from $G_{19(1)}$	—	–50	–35	dB
4.5MHz L.P.F. group delay	ΔGD_{19}	V_{IN17} = 0.4 V[p-p], Difference of group delay from 0.1 MHz to 3.58 MHz	–70	0	70	ns
Video amp. gain 1	$G_{22(1)}$	V_{IN20} = 0.4 V[p-p], 0.1 MHz	13.4	14	14.6	dB
Video amp. gain 2	$\Delta G_{22(2)}$	V_{IN20} = 0.4 V[p-p], 4.5 MHz Difference from $G_{22(1)}$	– 0.6	– 0.2	0.2	dB
Video amp. gain 3	$G_{22(3)}$	V_{IN20} = 0.4 V[p-p], 0.1 MHz	—	–40	–35	dB
Video amp. N.R. characteristic	$\Delta G_{22(4)}$	V_{IN20} = 0.02 V[p-p], 4.5 MHz Difference from $G_{22(2)}$	–6.5	–4.5	–2.5	dB
C/N detection voltage 1	$V_{26(1)}$	When V_{IN48} = 63.4 mV and 8.9 MHz, adjust V_8 so as to get V_{26} = 2.5 ± 0.05 V and measure at V_{IN48} = 0.2 mV[p-p] and 8.9 MHz	—	0.5	1.8	V
C/N detection voltage 2	$V_{26(2)}$	When V_{IN48} = 63.4 mV and 8.9 MHz, adjust V_8 so as to get V_{26} = 2.5 ± 0.05 V and measure at V_{IN48} = 31.8 mV[p-p] and 8.9 MHz	3.7	4.3	—	V
Video system total check	V_{25}	Input signal (pin 48) is BS signal of white 100% and input amp. gain is 6 dB	1.8	2	2.2	V[p-p]
Bit-stream output voltage Int.	V_{9A1}	V_{IN45} = 0.5 V[p-p], 2 MHz square-wave	0.84	1	1.16	V[p-p]
Bit-stream output voltage Ext.	ΔV_{9B1}	V_{IN6} = 0.5 V[p-p], 2 MHz square-wave	0.84	1	1.16	V[p-p]
Bit-stream detection voltage 1	$V_{14(1)}$	V_{IN6} = 0.1 V[p-p], 2 MHz square-wave	—	0.1	1	V
Bit-stream detection voltage 2	$V_{14(2)}$	V_{IN6} = 0.3 V[p-p], 2 MHz square-wave	4	4.9	—	V
AFC control 1	$V_{11(1)}$	V_{IN6} = 0.5 V[p-p], 2 MHz square-wave	—	0.1	1	V
AFC control 2	$V_{11(2)}$	V_{IN6} = 0.5 V[p-p], 2 MHz square-wave	4	4.9	—	V
AFC control 3	$V_{11(3)}$	V_{IN6} = no input	4	4.9	—	V
QPSK phase detection output 1	V_{27}	V_{IN48} = 0.4 V[p-p], 5.7273MHz + 0.05MHz	0.45	0.6	0.75	V[p-p]
QPSK phase detection output 2	ΔV_{31}	V_{IN48} = 0.4 V[p-p], 5.7273MHz + 0.05MHz Difference between measured V_{31} and V_{27}	– 0.8	0	0.8	dB
QPSK B.P.F./L.P.F. frequency characteristic 1	ΔV_{27B}	Difference between V_{27} at V_{IN48} = 0.4 V[p-p], 6.2273 MHz, f_{27} = 0.5 MHz and that at f_{IN48} = 5.7773 MHz	–3.7	–2	– 0.2	dB
QPSK B.P.F./L.P.F. frequency characteristic 2	ΔV_{27C}	Difference between V_{27} at V_{IN48} = 0.4 V[p-p], 6.7273 MHz, f_{27} = 0.5 MHz and that at f_{IN48} = 5.7773 MHz	—	–18	–10	dB
QPSK B.P.F./L.P.F. frequency characteristic 3	ΔV_{27D}	Difference between V_{27} at V_{IN48} = 0.4 V[p-p], 5.2273 MHz, f_{27} = 0.5 MHz and that at f_{IN48} = 5.7773 MHz	–6	–4	–1.8	dB

■ Electrical Characteristics T_a = 25°C (continued)

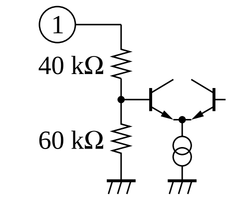
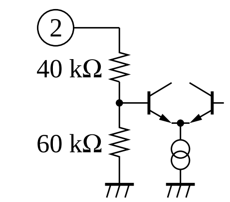
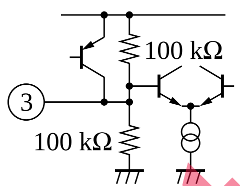
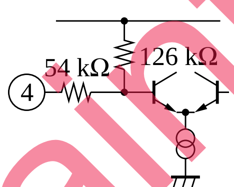
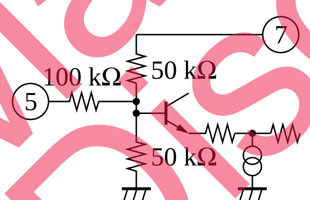
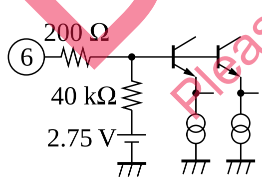
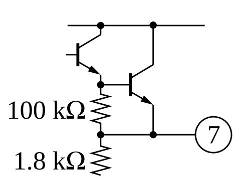
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QPSK B.P.F./L.P.F. frequency characteristic 4	ΔV_{27E}	Difference between V_{27} at V_{IN48} = 0.4 V[p-p], 4.7273 MHz, f_{27} = 0.5 MHz and that at f_{IN48} = 5.7773 MHz	—	–20	–15	dB
QPSK B.P.F./L.P.F. frequency characteristic 5	ΔV_{27F}	Difference between V_{27} at V_{IN48} = 0.4 V[p-p], 3.58 MHz, $f_{27} \approx$ 2.15 MHz and that at f_{IN48} = 5.7773 MHz	—	–40	–36	dB
Capture range 1	CR+	Input signal (pin 48) is QPSK	20	115	—	kHz
Capture range 2	CR–	Input signal (pin 48) is QPSK	—	–115	–20	kHz
Data output H	V_H	V_{37} and V_{38} voltages at V_{28} and V_{30} = 3.5 V	3.5	4.1	—	V
Data output L	V_L	V_{37} and V_{38} voltages at V_{28} and V_{30} = 2.9 V	—	0.9	1.5	V
Clock free-run frequency	Δf_{40}	Difference between f_{40} at V_{41} = 1/2 V_{CC} (=2.5 V) and 18.432 MHz	–0.35	0.55	1.45	kHz
Clock output	V_{40}	V_{41} = 1/2 V_{CC} (=2.5 V)	1.1	1.5	—	V[p-p]
Clock Frequency adjustment (+)	$\Delta f_{40(+)}$	Difference between $f_{40(+)}$ at V_{41} = 4 V and 18.432 MHz	3.2	3.7	—	kHz
Clock Frequency adjustment (–)	$\Delta f_{40(-)}$	Difference between $f_{40(-)}$ at V_{41} = 1 V and 18.432 MHz	—	–6.3	–4	kHz
Switch changeover voltage H	V_{SW-H}	Changeover voltage to set pin 1, pin 2, pin 4, pin 10, pin 11, pin 46 to high-level	4	5	—	V
Switch changeover voltage L	V_{SW-L}	Changeover voltage to set pin 1, pin 2, pin 4, pin 10, pin 11, pin 46 to low-level	—	0	1	V

• Design reference data

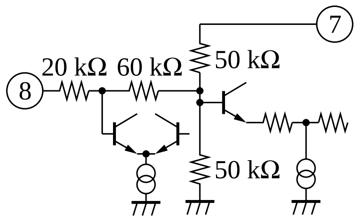
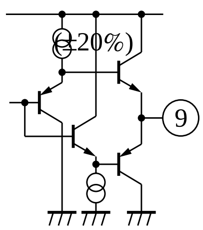
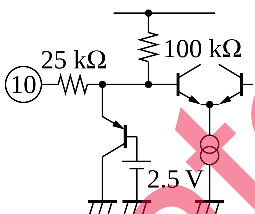
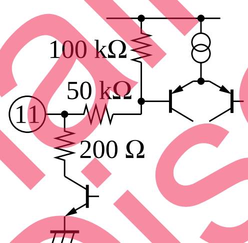
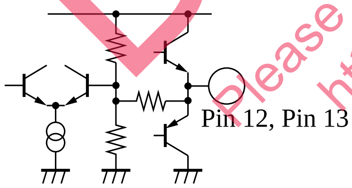
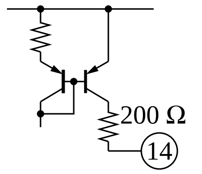
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DG	DG	2 V[p-p] at V_{O23} and APL = 10, 50, 90%		1.8	3	%
DP	DP	2 V[p-p] at V_{O23} and APL = 10, 50, 90%		1.8	3	°C
Dispersal rejection factor	R_{DIS}	Δf = 3 MHz, f_{DIS} = 30 Hz		–50	–45	dB
Video luminance S/N	S/N	Using H.P.F. 10 kHz and L.P.F. 4.2 MHz unweighted		56	50	dB
Input amp. separation 1	ΔG_{12}	Difference between V_{12} at inputting (1 MHz) to V_{IN48} for V_2 = low or inputting to V_{IN3} for V_2 = high and $G_{12A1.}$ (75 ohm termination)		–55	–45	dB
Input amp. separation 2	ΔG_{13}	Difference between V_{13} at inputting (1 MHz) to V_{IN48} for V_2 = low or inputting to V_{IN3} for V_2 = high and $G_{13A1.}$ (75 ohm termination)		–55	–45	dB
Bit-stream separation 1	$\Delta G_{9(1)}$	V_2 = 1 V, V_6 = 3.5 V input is pin 45 (V_{IN45} = 0.5 V[p-p], f_{IN45} = 2 MHz square-wave)		–55	–45	dB
Bit-stream separation 2	$\Delta G_{9(2)}$	V_2 = 4 V, input is pin 6 (V_{IN6} = 0.5 V[p-p], f_{IN6} = 2 MHz square-wave)		–55	–45	dB

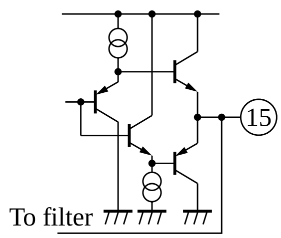
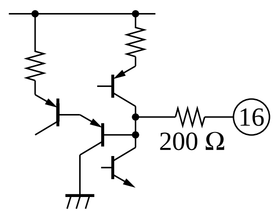
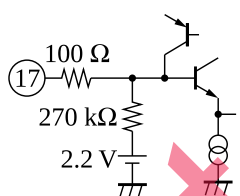
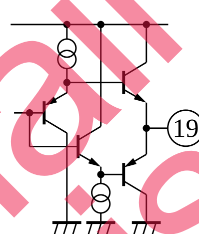
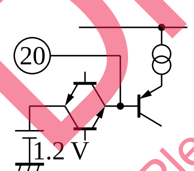
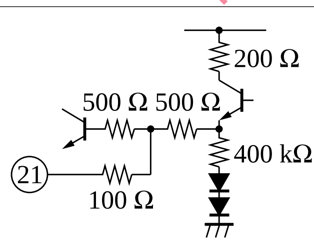
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
1		100 k	Switches output of pin 13 (detection output 2). • Pin 13 outputs the input signal from pin 3 at low-level and pin 48 at high-level. Open will do for low-level.	0
2		100 k	Switches output of pin 12 (detection output 1) and pin 9 (bit-stream output) • Pin 12 and pin 9 output the input signal from pin 3, pin6 at low-level and pin 48, pin 45 at high-level respectively. Open will do for low-level.	0
3		50 k (±10%)	External input pin of base-band signal to input amp. • Input level min. 0.62, typ. 0.67, max. 0.72 V[p-p]	2.5
4		180 k	Mute switch of video signal • Low-level: normal operation high-level: video signal mute Open will do for high-level.	5
5		125 k	Adjusts the gain of input amp. with this pin from 0 V to 3 V. Possible to adjust only the signal inputted from pin 48.	1.5
6		40 k (±10%)	Input pin of bit-stream • Input level min. 0.4, typ. 0.5, max. 0.6 V[p-p]	2.75
7		0	Reference voltage pin for gain adjustment volume	3

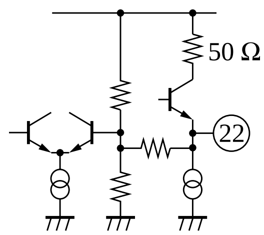
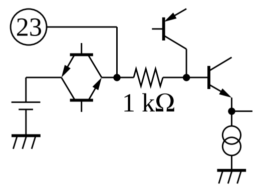
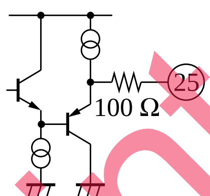
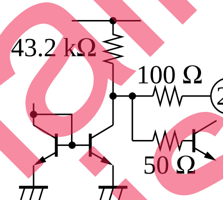
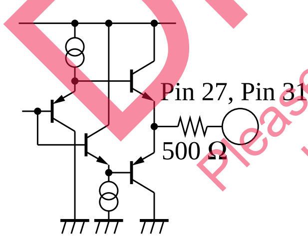
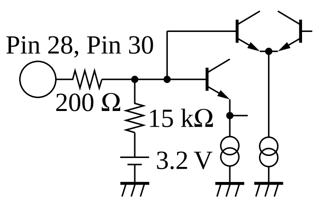
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
8		105 k	Adjustment pin of C/N detection voltage (to be adjusted in 0 V to 3 V)	1.5
9		13	Output pin of bit-stream signal • Capable of 75 Ω drive • Output level min. 0.8, typ. 1, max. 1.2 V[p-p]	2.6
10		125 k	Gain switch between BS and CS • Low-level: BS high-level: CS Open will do for high-level.	3.3
11		150 k	Switch to CS broadcasting satellite (gain) at pin 10 high-level • Low-level: 18 MHz[p-p] (SCC) high-level: 15.8 MHz[p-p] (JCSAT) Open will do for high-level. • This pin becomes AFC control pin at pin 10 low-level and low-level at pin 1 low-level and high-level at pin 1 high-level.	3.3
12 13		0 (10 Ω or less)	Output pin of input amp. • Capable of 75 Ω drive • Output level min. 0, typ. 1.34, max. 2 V[p-p]	2.5
14		—	When a bit-stream signal is inputted to pin 6, current flows. (Open collector) • Use this pin by connecting a resistor of 5 kΩ or more between this pin and GND.	—

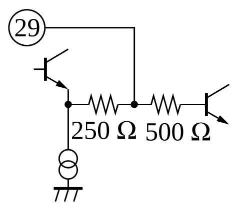
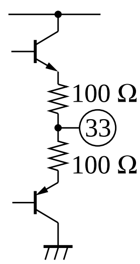
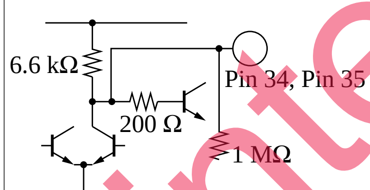
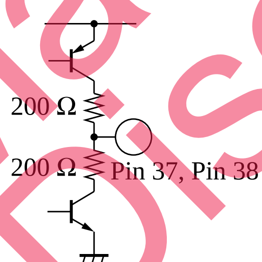
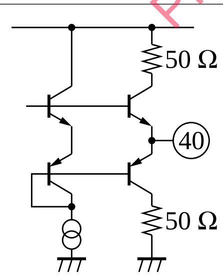
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
15		20 (±20%)	Output pin of input amp. • Output level min. 0, typ. 1.34, max. 2 V[p-p] • The signal which is inputted from pin 48 is always outputted from this pin.	2.5
16		200	Reference pin for automatic adjustment of each filter	3.3
17		270 k	Input pin of 4.5 MHz L.P.F • Input level min. 0.35, typ. 0.4, max. 0.6 V[p-p]	2.2
18	—	—	—	—
19		20	Output pin of 4.5 MHz L.P.F • Output level min. 0.35, typ. 0.4, max. 0.42 V[p-p]	2.2
20		∞	Input pin for clamp circuit of first stage and video amp. • Input level (luminance signal level) min. 0, typ. 0.4, max. 0.6 V[p-p]	1.2
21		600	Reference pin for pulse sampling in pulse clamp circuit	3.2

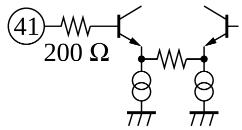
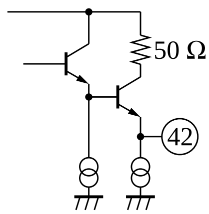
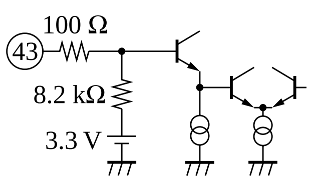
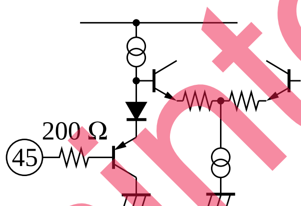
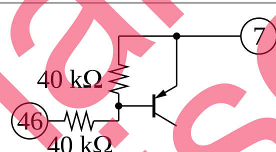
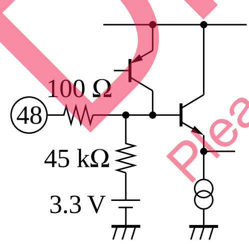
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
22		30 (±20%)	Output pin of video amp. • Capacitance coupling with pin 23. • Output level (luminance signal level) min. 1.6 , typ. 2, max. 2.35 V[p-p]	0.6
23		∞	Input pin to second stage clamp circuit • Input level (luminance signal level) min. 0, typ. 2, max. 2.35 V[p-p]	1.3
24	—	—	Should be same potential as pin 36 (QPSK supply voltage).	—
25		130 (±20%)	Output pin of video signal • Output level (luminance signal level) min. 1.65, typ. 2, max. 2.35 V[p-p]	1.3
26		43.2 k (±20%)	Taking out a noise level of 8.9 MHz and proximity as C/N det. voltage.	5
27 31		400	Output pin of eye pattern • Make a.c. coupling between pin 27 and pin 28, and pin 31 and pin30 • Output level min. 0.5, typ. 0.65, max. 0.8 V[p-p]	2.7
28 30		15 k	Input pin of eye pattern • Input to comparator and carrier phase comparator. • Input level min. 0.5, typ. 0.65, max. 0.8 V[p-p]	3.2

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
29		250	Peak-hold pin of QPSK AGC	2.4
32	—	—	No connection inside the IC	—
33		50	Output pin of VCO phase error voltage • Connect a lag-lead filter between this pin and pin34, pin 35.	2.5
34 35		6.6 k	Output pin of QPSK costus loop	4.7
36	—	—	—	—
37 38		100 (±20%)	Output pin of I, Q data • Connect to PCM decoder. • Output level min. 2, typ. 3.2, max. 5 V[p-p]	—
39	—	—	—	—
40		20 (±20%)	Output pin of data clock (18.4 MHz) • Output level min. 1.1, typ. 1.5, max. 2 V[p-p]	3.3

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Impedance (Ω)	Description	DC voltage (V)
41		100 k	Input phase error (PD signal) of PCM decoder through a lag-lead filter • Enables input voltage 0 V to V_{CC}	2.5
42		20	Output pin of data clock VCO (18.4 MHz) • Insert a crystal resonator between this pin and pin 42 • Output level min. 0.5, typ. 1, max. 1.5 V[p-p]	1.8
43		8.3 k	Input pin of data clock VCO • Input level min. 0.4, typ. 0.6, max. 0.8 V[p-p]	3.3
44	—	—	—	—
45		52 k (±10%)	Input pin of bit-stream • Input level min. 0.4, typ. 0.5, max. 0.6 V[p-p]	—
46		80 k	Switch of noise reduction (NR) • Low-level: NR off high-level: NR on Open will do for high-level.	3.2
47	—	—	—	—
48		45 k	Internal input pin of base-band signal to input amp. • Input level min. 0.5, typ. 0.67, max. 2.2 V[p-p]	3.3

■ Technical Data

• On the frequency characteristics of 4.5 MHz L.P.F.

Frequency characteristics of 4.5 MHz L.P.F. (frequency characteristics from pin 17 to pin 19 of this IC) is shown roughly in figure 1.

Shown in figure 3 is the frequency characteristics to be obtained when de-emphasis filter is connected in front of this L.P.F. (figure 2).

Shown in figure 4 is the frequency characteristics to be obtained when resistor of de-emphasis filter is changed from 390 Ω to 470 Ω.

Thus, frequency characteristics of 4.5 MHz L.P.F. can be changed, resulting from changing the frequency characteristics of de-emphasis.

Figure 1. 4.5 MHz L.P.F. frequency characteristics (pin 17 → pin 19)

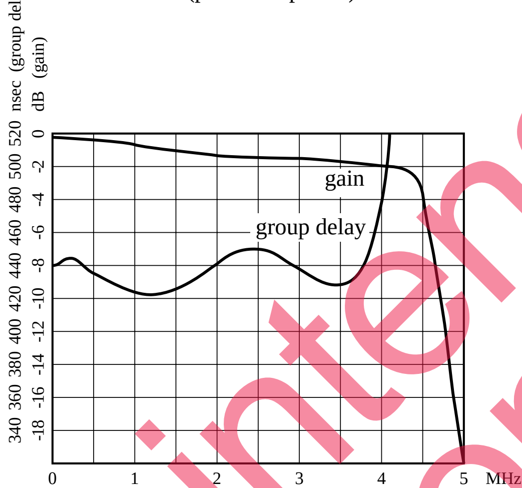


Figure 2. De-emphasis filter connection circuit

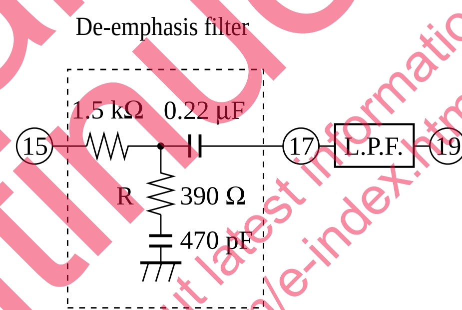


Figure 3. Frequency characteristics of figure 2. (R = 390 Ω)

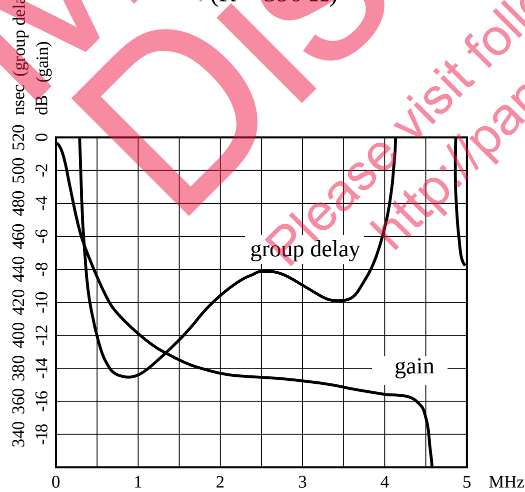
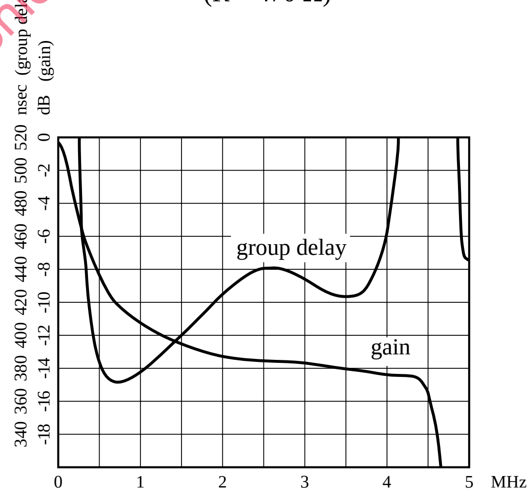
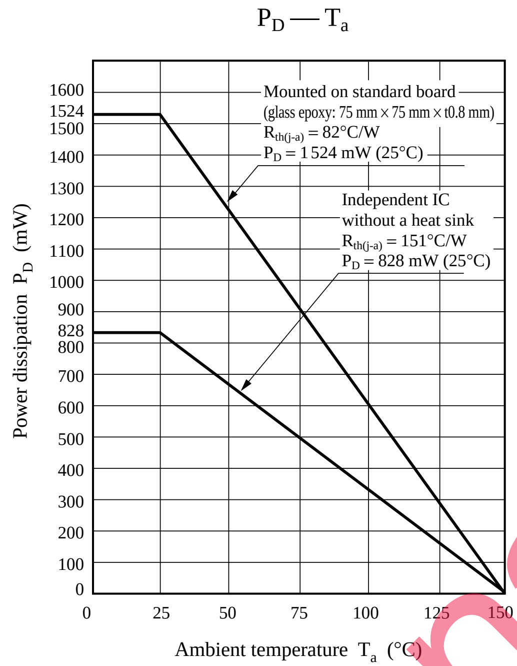


Figure 4. Frequency characteristics of figure 2. (R = 470 Ω)



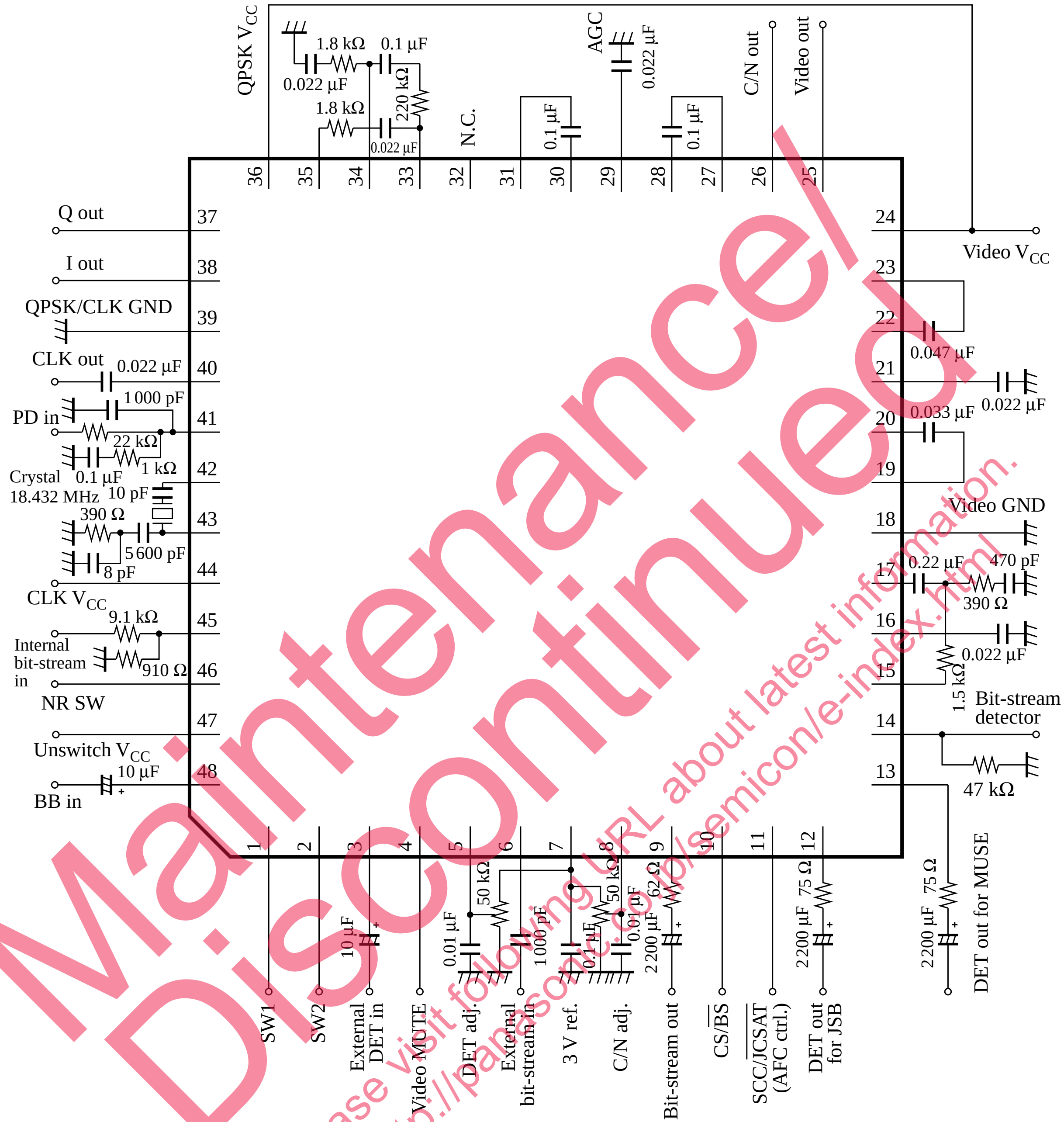
■ P_D — T_a curves of QFP048-P-1010C



■ Precaution on handling

Supply voltage pins of this IC are pin 24, pin 36, pin 44 and pin 47.
Use with same potential for pin 24 and pin 36 out of these pins.

■ Application Circuit Example



Changeover between detection output (pin 12) and bit-stream output (pin 9)

	When bit-stream is inputted on pin 6		When pin 6 is no input	
V_2	V_{O12}	V_{O9}	V_{O12}	V_{O9}
Low-level or open	V_{IN3}	V_{IN6}	V_{IN48}	V_{IN45}
High-level	V_{IN48}	V_{IN45}		

Changeover between detection output (pin 13) and pin 11 level (at pin10 low-level)

	When bit-stream is inputted on pin 6		When pin 6 is no input	
V_1	V_{O13}	V_{11}	V_{O13}	V_{11}
Low-level or open	V_{IN3}	High-level	V_{IN48}	High-level
High-level	V_{IN48}	Low-level		

Bit-stream detection (pin 14) level

	V_{14}
When pin 6 is no input	Low-level
When bit-stream is inputted on pin 6	High-level

Changeover between BS and CS mode

V_{10} \ V_{11}	Low-level	High-level or open
Low-level	BS (17 MHz[p-p])	
High-level or open	SCC (18 MHz[p-p])	JCSAT (15.8 MHz[p-p])

Video output

V_4	
Low-level	Output
High-level or open	Mute

Video NR

V_{46}	
Low-level	NR off
High-level or open	NR on

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