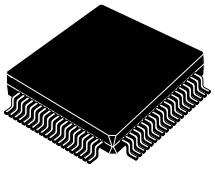
TDA7513T

Single chip FM/AM tuner with stereo decoder and audio processor

Features

- AM/FM tuner for car radio
- Integrated tuning PLL
- Variable bandwith FM IF filter (ISS)
- Fully integrated FM stereo decoder
- fully integrated FM noise blanker
- Highly integrated audio processor



LQFP80

Description

The TDA7513T is the first device for car-radio applications that combines full RF front end functions with audio-processing capabilities.

As far as FM and AM functions are concerned , the TDA7513T features front end processing, including the digital tuning PLL, IF processing with demodulation and variable bandwidth IF filtering (ISS), stop station and quality detection functions, FM stereo decoding by means of a fully integrated, adjustment free, dedicated PLL and, finally, FM noise blanking. The FM stereo decoder and noise blanker functions are realized entirely without external components.

The audio processor section comprises input selectors for two quasi-differential external sources, volume control, tone control (bass, mid and treble), balance and fading control to drive four output channels. A soft mute function and an RDS mute function are included to handle source change as well as RDS AF search without abrupt changes in the audio level.

Most of the parameters in the front-end section are I^2C bus-driven and therefore under the control of the car radio maker. The I^2C bus allows furthermore the user to realize the full electric alignment of all the external coils, therefore removing the need for hand-made or mechanical adjustments.

Table 1. Device summary

Part number	Package	Packing
TDA7513T	LQFP80	Tray
E-TDA7513T	LQFP80	Tray

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1 Block diagrams

Figure 1. Tuner section

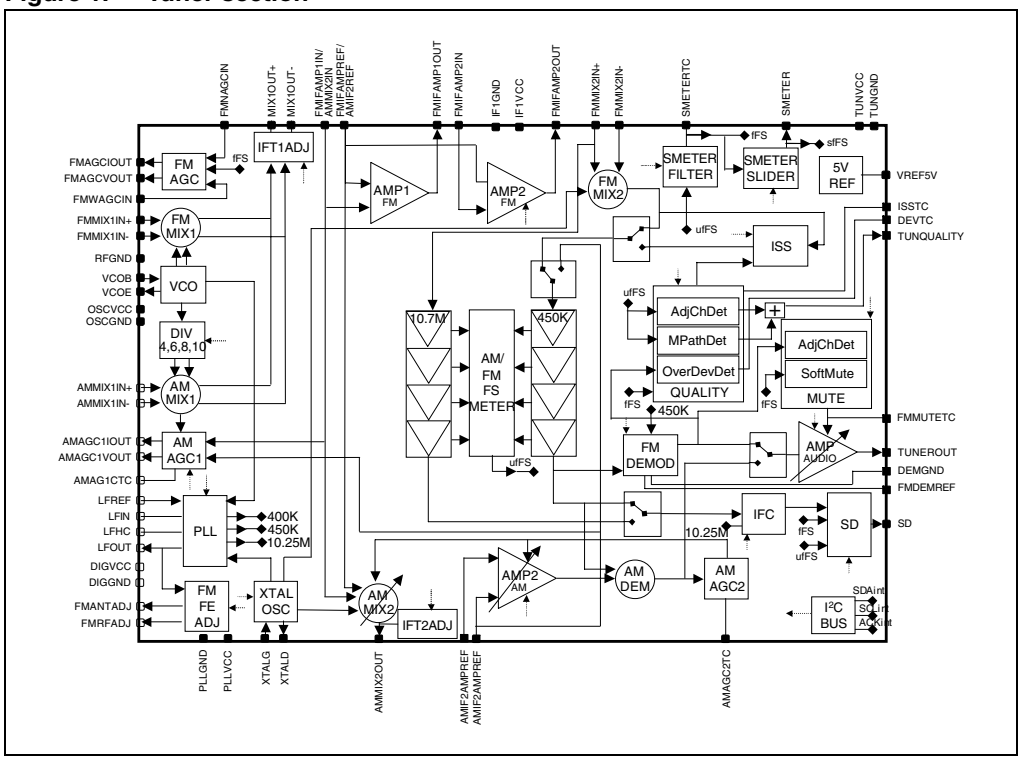


Figure 2. Stereo decoder / audio processor section

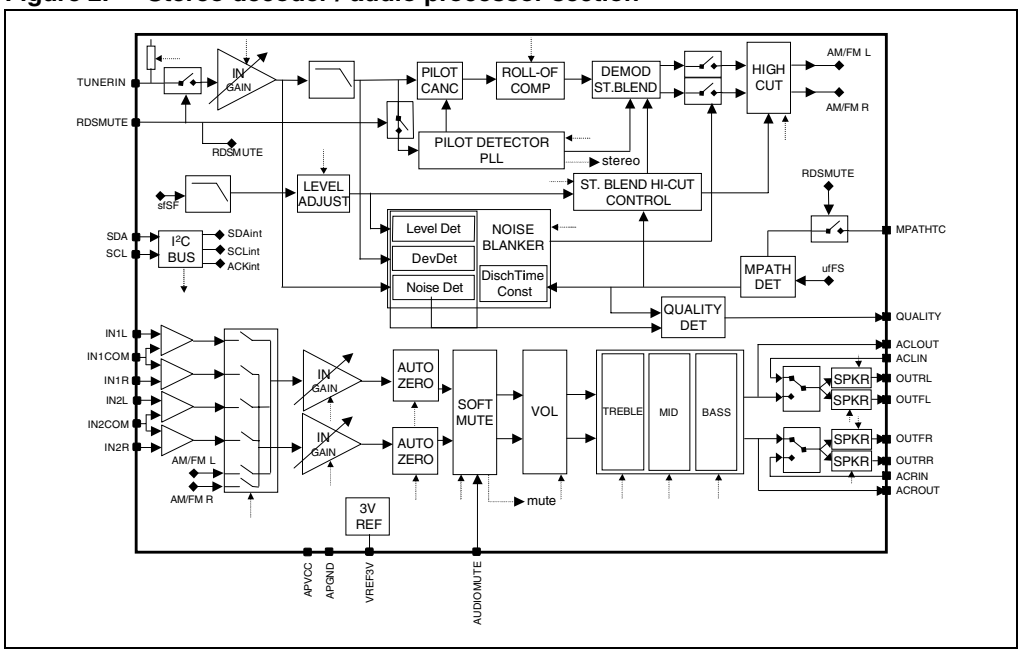


Figure 3. Pin connections

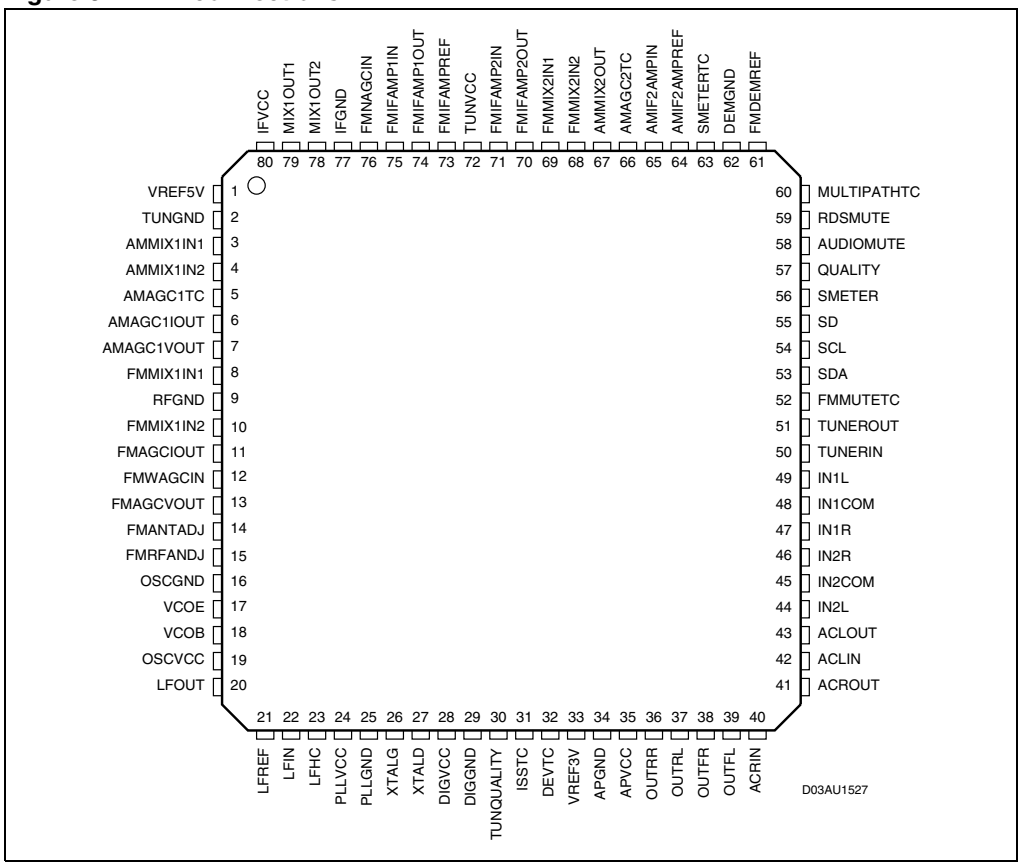


Table 2. Pin description

Pin	Pin name	Pin function
1	VREF5V	5V reference
2	TUNGND	tuner general ground
3	AMMIX1IN1	am mix1 input
4	AMMIX1IN2	am mix1 input
5	AMAGC1TC	am agc1 filter capacitor
6	AMAGC1IOUT	am agc1 current output
7	AMAGC1VOUT	am agc1 voltage output
8	FMMIX1IN1	fm mix1 input
9	RFGND	rf ground
10	FMMIX1IN2	fm mix1 input
11	FMAGCIOUT	fm agc current output
12	FMWAGCIN	fm agc RF input
13	FMAGCVOUT	fm agc voltage output

Table 2. Pin description (continued)

Pin	Pin name	Pin function
14	FMANTADJ	fm antenna filter adjustment
15	FMRFANDJ	fm rf filter adjustment
16	OSCGND	vco ground
17	VCOE	am/fm vco emitter
18	VCOB	am/fm vco base
19	OSCVCC	vco supply (8V)
20	LFOUT	PLL loop filter output
21	LFREF	PLL loop filter reference
22	LFIN	PLL loop filter input
23	LFHC	PLL loop filter high-current input
24	PLLVCC	PLL back-end supply
25	PLLGND	PLL back-end ground
26	XTALG	ref osc gate
27	XTALD	ref osc drain
28	DIGVCC	digital dirty supply (8V)
29	DIGGND	digital ground
30	TUNQUALITY	tuner combined output of multipath and adjacent channel detectors
31	ISSTC	ISS time constant
32	DEVTC	deviation detector time constant
33	VREF3V	3V reference
34	APGND	audio processor/stereo decoder ground
35	APVCC	audio processor/stereo decoder supply (8V)
36	OUTRR	audio out
37	OUTRL	audio out
38	OUTFR	audio out
39	OUTFL	audio out
40	ACRIN	ac coupling right input
41	ACROUT	ac coupling right output
42	ACLIN	ac coupling left input
43	ACLOUT	ac coupling left output
44	IN2L	audio in2 left
45	IN2COM	audio in2 common
46	IN2R	audio in2 right
47	IN1R	audio in1 right

Table 2. Pin description (continued)

Pin	Pin name	Pin function
48	IN1COM	audio in1 common
49	IN1L	audio in1 left
50	TUNERIN	am audio/fm mpx input
51	TUNEROUT	am audio/fm mpx output
52	FMMUTETC	fm muting time constant capacitor
53	SDA	I2C bus data
54	SCL	I2C bus clock
55	SD	am/fm station detector output
56	SMETER	am/fm smeter output
57	QUALITY	quality output
58	AUDIOMUTE	audio mute control
59	RDSMUTE	rds mute control
60	MULTIPATHTC	multipath detector time constant
61	FMDEMREF	fm demodulator reference capacitor
62	DEMGND	fm demodulator ground
63	SMETERTC	am/fm smeter filtering capacitor
64	AMIF2AMPREF	am if2 amp feedback capacitor
65	AMIF2AMPIN	am if2 amp input
66	AMAGC2TC	am agc2 filter capacitor
67	AMMIX2OUT	am mix2 single-ended output
68	FMMIX2IN2	fm mix2 input
69	FMMIX2IN1	fm mix2 input
70	FMIFAMP2OUT	fm if1 amp2 output
71	FMIFAMP2IN	fm if1 amp2 input
72	TUNVCC	tuner general supply (8V)
73	FMIFAMPREF	fm if1 amps reference capacitor
74	FMIFAMP1OUT	fm if1 amp1 output
75	FMIFAMP1IN	fm if1 amp1 input
76	FMNAGCIN	fm agc IF input
77	IFGND	if1 ground
78	MIX1OUT2	am/fm mix1 output
79	MIX1OUT1	am/fm mix1 output
80	IFVCC	if1 supply (8V)

2 Electrical characteristcs

2.1 FM

(V_{CC} = 8V; T_{amb} = 25°C; V_{sg} = 60dBµV; fc = 98.1MHz; f_{dev} = 40kHz; f_{mod} = 1kHz unless otherwise specified)

Table 3. General

(audioprocessor all flat and stereo decoder input gain = 4dB)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
US	Useable sensitivity		SNR = 40dB		0		dBµV
SNR	Signal to Noise ratio				66		dB
LS	Limiting Sensitivity		Soft Mute OFF; @ ΔVout = -3dB		-4		dBmV
THD	Total Harmonic Distortion		fdev = 40kHz		0.1	0.3	%
			fdev = 75kHz		0.15	0.5	%
Vout	Audio output level		rms		375		mV
ISN	Interstation noise		ΔVout @ RF OFF; Soft Mute OFF		-13		dB
IFCS	IF Counter sensitivity				2	10	dBµV
Icc	DC current	OSCVcc			5.7		mA
		PLLVcc			1.9		mA
		DIGVcc			9.8		mA
		TUNVcc			50		mA
		IF1Vcc			13.4		mA
		APVcc			27.3		mA

Table 4. Mixer1

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Gv	conversion gain		from RFT secondary to IFT1 secondary loaded with 330Ω		9		dB
IIP3	3rd order intercept point		referred to RFT secondary				dBµV
CIFT1	IFT1 adjustment capacitor	min	Between MIXOUT+ and MIXOUT-		0		pF
		max			8.25		pF
		step			0.55		pF
Rin	input resistance (single ended)		FMMIX1IN+ and FMMIX1IN- w.r.t. gnd		10		W

Table 5. Front end adjustment

(VRFadj and VANTadj referred to VLFOUT)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vantadj	min			-40		%
	max			40		%
	step			1.29		%
VRFadj	min			-40		%
	max			40		%
	step			1.29		%

Table 6. AGC

(wide AGC input connected to RFT primary through 10pF and 1KΩ)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
WAGCsp	Wide AGC starting point		VRFTprimary @ I(FMAGCOUT) = 5µA		84		dBµV
WAGCRin	FMWAGCIN input resistance				125		W
NAGCsp	Narrow AGC starting point (max sensitivity)		VRFTprimary @ I(FMAGCOUT) = 5µA; Keyed AGC OFF		95		dBµV
KNAGCsp	Keyed narrow AGC starting point (min sensitivity)		VRFTprimary @ I(FMAGCOUT) = 5µA; Keyed AGC ON; V(SMETERTC)<0.9V		109		dBµV
NAGCRin	FMNAGCIN input resistance				10		KΩ
KAGCTH high	Smeter for Keyed narrow AGC maximum sensitivity	minimum programming	V(SMETERTC) @ narrow AGC starting point = NAGCsp		0.9		V
		maximum programming			2.5		V
KAGCTH low	Smeter for Keyed narrow AGC minimum sensitivity	minimum programming	V(SMETERTC) @ narrow AGC starting point = KNAGCsp		1.6		V
		maximum programming			3.2		V
Iout	min		AGC OFF			0.1	µA
	max		AGC ON	8			mA
Vout	min		AGC ON		0.1	0.5	V
	max		AGC OFF	Vcc-0.5			V
AGCVRout	FMAGCVOUT output resistance				100		KΩ

Table 7. IF Amplifier 1

(Input at FMIFAMP1IN, fc = 10.7MHz, no mod)
(Output at FMIFAMP1OUT loaded with 330Ω)
(antenna level = FMIFAMP1IN – 31dB)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
G	Gain			18		dB
IIP3	3rd order intercept point	referred to FMIFAMP1IN		126		dBμV
Rin	input resistance (single-ended)	FMIFAMP1IN w.r.t. gnd		330		W
Rout	output resistance			330		W

Table 8. IF Amplifier 2

(Input at FMIFAMP2IN, fc = 10.7MHz, no mod)
(Output at FMIFAMP2OUT loaded with 330Ω)
(antenna level = FMIFAMP2IN – 45dB)
Gain MUST BE SET to 14dB for ISS operation.

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
G	minimum gain	programmable gain		6		dB
				8		dB
				10		dB
	maximum gain			14		dB
IIP3	Input 3rd order intercept point	referred to FMIFAMP2IN, G = 8dB		134		dBmV
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Rin	input resistance (single-ended)	FMIFAMP2IN to gnd		330		W
Rout	output resistance			330		W

Table 9. Field-strength meter

(Input at FMMIX2IN; fc = 10.7MHz, no mod)
(antenna level = V67 – 49dB)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
FS1	FSmeter1		V(FMMIX2IN+) = 50 dBmV		1.4		dBmV
FS2	FSmeter2		V(FMMIX2IN+) = 70 dBmV		2.7		dBmV
FS3	FSmeter3		V(FMMIX2IN+) = 90 dBmV		4.4		dBmV
FSR	FSmeter filtering resistor		SMETERTC pin		10.7		kW
FFSS	Filtered FSmeter Slider	min			0		V
		max			1.5		V
		step			50		mV

Table 10. MPX output (output at TUNEROUT)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Gc	conversion gain			5.42		mV/kHz
Vaudio	audio level	peak, 40kHz deviation		217		mVp

Table 11. Field strength stop station

(Input at FMMIX2IN – fc = 10.7MHz, no mod) (antenna level = V69 – 49dB)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
FSSSmin	minimum threshold	Vthr = 0.4V		50		dBµV
FSSSmax	maximum threshold	Vthr = 3.4V		78		dBµV
FSSSstep	threshold step	ΔVthr = 200mV		3		dB

Table 12. Soft mute

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
SMD	Soft Mute Depth	min			13.4		dB
					16		dB
					19.5		dB
		max			24		dB
MCVlow	Mute control voltage low		V(FMMUTETC) @ No mute attenuation		0.2		V
MCVhigh	Mute control voltage high		V(FMMUTETC) @ Max mute attenuation		2		V
ACMcl	Adjacent channel mute clamp voltage	min	Max V(FMMUTETC) in Adjacent Channel conditions		500		mV
		max			2000		mV
		step			100		mV

Table 13. ISS filter (FMIF1AMP1 gain must be set to 14dB) **(1)**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
BW1	Wide bandwidth	Full bandwidth @ -3dB		120		kHz
BW2	Narrow bandwidth			80		kHz
BWwb	Weather Band bandwidth			30		kHz

1. *If ISS function is not used, SEEK must be set to "ON" in FM*

2.2 AM

(V_{CC} = 8V; T_{amb} =25°C; Vsg = 74dBµV,emf; fc = 999kHz; 30% modulation; fmod = 400Hz unless otherwise specified).

Table 14. General

(with 20pF/65pF dummy antenna; input levels @ SG,emf; output @ audioprocessor output; audioprocessor all flat; stereo decoder input gain = 5.75dB)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
US	Useable sensitivity		SNR = 20dB		26		dBµV
SNR	Signal to Noise ratio				56	60	dB
MS	Maximum Sensitivity		@ ΔVout = -10dB		20		dBµV
THD	Total Harmonic Distortion		mod =30%, Vsg = 74dBµV		0.59		%
			mod =80%, Vsg = 74dBµV		1.48		%
			mod =30%, Vsg = 120dBµV		1.88		%
			mod =80%, Vsg = 120dBµV		3		%
THDLF	THD @ low frequency		mod =30%, Vsg = 74dBµV, fmod=100Hz		2		%
Vout	Audio output level		rms		266		mV
ISN	Interstation noise level		ΔVout @ RF OFF		-35	-31	dB
IFCS	IF Counter sensitivity			8	10	20	dBµV
Icc	DC current	OSCVcc			5.6		mA
		PLLVcc			1.9		mA
		DIGVcc			12.1		mA
		TUNVcc			68		mA
		IF1Vcc			7.8		mA
		APVcc			27		mA

Table 15. Mixer1 (Input at AMMIX1IN+, no mod)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Gv	conversion gain		from AMMIX1IN+to IFT1 secondary loaded with 330 Ω		13		dB
IIP3	Input 3rd order intercept point		referred to AMMIX1IN+		130		dBµV
Rin	input resistance (differential)		AMMIX1IN+ w.r.t. AMMIX1IN-		1.2		kΩ
CIFT1	IFT1	min	Between MIXOUT+ and MIXOUT-		0		pF
	adjustment	max			8.25		pF
	capacitor	step			0.55		pF

Table 16. AGC1

(Wide AGC input = AM Mixer1 input; Narrow AGC input = AM Mixer2 input; Ultra Narrow AGC input = AM IF2 Amp input; fWAGCin = 999kHz, fNAGCIN = 10.7MHz, fUNAGCin = 450kHz)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
WAGCsp	Wide AGC	min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		85		dBµV
	starting point	max			104		dBµV
NAGCsp	NarrowAGC	min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		79		dBµV
	starting point	max			97		dBµV
UNAGCsp	Ultra Narrow AGC	min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		50		dBµV
	starting point	max			97		dBµV
AGC1R	AGC1 filtering resistor		AMAGC1TC pin		100		KΩ
Iout	min		AGC OFF			1	µA
	max		AGC ON	0.4			mA
Vout	min		AGC ON			0.5	V
	max		AGC OFF		3.38		V
AGC1VRout	AMAGC1VOUT output resistance				23		KΩ

Table 17. Mixer2

(Input at AMMIX2IN, fc = 10.7MHz, no mod)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Gv, max	conversion gain, no AGC		from AMMIX2IN to IFT2 secondary loaded with 2k Ω		15		dB
Gv, min	conversion gain, full AGC		from AMMIX2IN to IFT2 secondary loaded with 2kΩ		-7		dB
IIP3	Input 3rd order intercept point		referred to AMMIX2IN, no AGC		120		dBµV
Rin	input resistance		AMMIX2IN w.r.t. ground		330		W
CIFT2	IFT2	min	Between AMMIX2OUT and gnd		0		pF
	adjustment	max			24		pF
	capacitor	step			1.6		pF

Table 18. IF2 amplifier

(Input at AMIF2AMPIN, fc = 450kHz, no mod)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Gv, max	gain, no AGC	max prog			64.8		dB
					62.8		
					61.7		
					60.2		
					58.3		
					55.8		
		min prog			53.2		
ΔGv	gain decrease in full AGC		w.r.t. Gv, max		-40		dB
Rin	input resistance		AMMIX2IN w.r.t. ground		2		kΩ

Table 19. AGC2

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
AGC2R	AGC2 filtering resistor	reception			150		k Ω
		seek			5		k Ω

Table 20. Audio output

(output at TUNEROUT, 2.7k Ω load)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vaudio	audio level	rms, 30% modulation		305		mV

Table 21. Field strength meter

(Input at AMIF2AMPIN; fc = 450 kHz, no mod)
(SG,emf level = V65 – 29dB)

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
FS1	FSmeter1		V(AMIF2AMPIN) = 50 dBμV		0.7		dBμV
FS2	FSmeter2		V(AMIF2AMPIN) = 70 dBμV		2.1		dBμV
FS3	FSmeter3		V(AMIF2AMPIN) = 90 dBμV		4.2		dBμV
FSR	FSmeter filter resistor	min	SMETERTC pin		16.5		kΩ
		max			75		kΩ
FFSS	Filtered FSmeter Slider	min			0		V
		max			1.5		V
		step			48.4		mV

2.3 Oscillators (V_{CC} = 8V; T_{amb} =25°C)

Table 22. VCO

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Vvco	Oscillation level	Tuning Voltage = 4V	106		108	dBµV
C/N	Carrier to Noise ratio	Δf = 1kHz		85		dBc/Hz

Table 23. XTAL

Symbol	Parameter		Test condition	Min	Typ	Max	Unit
Vxtal	Oscillation level		@ XTAL gate		131		dBµV
FXTAL	Adjustment frequency range	min	referred to 10.25 MHz centered condition		-4		kHz
		max			+4		kHz
		step			238		Hz

Table 24. Audio processor

(VS = 8V; Tamb = 25°C; RL = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input gain						
GIN MIN	Min. Input Gain		-1	0	1	dB
GIN MAX	Max. Input Gain		13	15	17	dB
GSTEP	Step Resolution		0.5	1	1.5	dB
Quasi differential stereo input 1&2						
Rin	Input Resistance	Any input pin to gnd	70	100	130	kΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1V_{RMS} @ 1kHz	45	70		dB
		V_{CM} = 1V_{RMS} @ 10kHz	45	60		dB
Volume control						
GMAX	Max Gain		13	15	17	dB
ASTEP	Step Resolution		0.5	1	1.5	dB
EA	Attenuation Set Error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -60 to 20dB	-4	0	3	dB
ET	Tracking Error				2	dB
VDC	DC Steps	Adjacent Attenuation Steps				mV
		From 0dB to GMIN				mV
SOft mute/AFS						
AMUTE	Mute Attenuation		80	100		dB

Table 24. Audio processor (continued)

(VS = 8V; Tamb = 25°C; RL = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
TD	Delay Time	T1			0.48		ms
		T2			0.96		ms
		T3			20.2		ms
		T4			40.4		ms
VTH low	Low Threshold for SM-/AFS-Pin 1					1	V
VTH high	High Threshold for SM-/AFS-Pin			4			V
Bass control							
CRANGE	Control Range			±13	±15	±17	dB
ASTEP	Step Resolution			0.5	1	1.5	dB
fC	Center Frequency		fC1	54	60	66	Hz
			fC2	63	70	77	Hz
			fC3	72	80	88	Hz
			fC4	90	100 (150) (1)	110	Hz
QBASS	Quality Factor		Q1	0.9	1	1.1	
			Q2	1.1	1.25	1.4	
			Q3	1.3	1.5	1.7	
			Q4	1.8	2	2.2	
DCGAIN	Bass-Dc-Gain		DC = off	-1	0	1	dB
			DC = on	3.5	4.4	5.5	dB
MID control							
CRANGE	Control Range			±13	±15	±17	dB
ASTEP	Step Resolution			0.5	1	1.5	dB
fC	Center Frequency		fC1	450	500	550	Hz
			fC2	0.9	1	1.1	kHz
			fC3	1.35	1.5	1.65	kHz
			fC4	1.8	2	2.2	kHz
QBASS	Quality Factor		Q1	0.9	1	1.1	
			Q2	1.8	2	2.2	
Treble control							
CRANGE	Control Range			±13	±15	±17	dB

Table 24. Audio processor (continued)

(VS = 8V; Tamb = 25°C; RL = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ASTEP	Step Resolution		0.5	1	1.5	dB
fC	Center Frequency	fC1	8	10	12	kHz
		fC2	10	12.5	15	kHz
		fC3	12	15	18	kHz
		fC4	14	17.5	21	kHz
Speaker attenuators						
RIN	Input Impedance		17.5	25	32.5	kΩ
GMAX	Max Gain		13	15	17	dB
AMAX	Max Attenuation		-70	-79		dB
ASTEP	Step Resolution		0.5	1	1.5	dB
AMUTE	Output Mute Attenuation		80	90		dB
EE	Attenuation Set Error				±2	dB
VDC	DC Steps	Adjacent Attenuation Steps				mV
Audio outputs						
VCLIP	Clipping Level	THD = 0.3%	2.2	2.6		VRMS
RL	Output Load Resistance		2			kΩ
CL	Output Load Capacitance				10	nF
ROUT	Output Impedance			30	120	W
VDC	DC Voltage Level			3.9		V
General						
Gqd	Gain (QDin)	Quasi-differential Input		0.5		dB
Gstd	Gain (Tuner)	Tuner Input (STD InGain=4dB)		7.5		dB
eNO	Output Noise (QDin)	BW = 20 Hz to 20 kHz output muted; all flat			15	µV
		BW = 20 Hz to 20 kHz all gain = 0dB		20		µV
S/N	Signal to Noise Ratio (QDin)	all gain = 0dB flat; VO = 2VRMS		100		dB
		bass treble at 12dB; A-weighted; V_O = $2.6V_{RMS}$		96		dB

Table 24. Audio processor (continued)

(VS = 8V; Tamb = 25°C; RL = 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
d	Distortion (QDin)	VIN = 1VRMS; all stages 0dB		0.012	0.1	%
		VIN = 1VRMS; Bass & Treble = 12dB		0.05	0.1	%
SC	Channel separation Left/Right (QDin)		80			dB
ET	Total Tracking Error	AV = 0 to -20dB	-1	0	1	dB
		AV = -20 to -60dB	-2	0	2	dB
Bus inputs						
VIL	Input Low Voltage				0.8	V
VIH	Input High Voltage		2.5			V
IIN	Input Current	VIN = 0.4V	-5		5	µA
VO	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

1. See note in programming part

Note: The SM pin is active low (Mute = 0)

2.4 Stereo decoder

Table 25. Stereo decoder

(Vcc = 8V; deemphasis time constant = 50µs, VMPX = 305mVrms (75kHz deviation), fm= 1kHz, Gv = 4dB, Tamb = 27°C; unless otherwise specified)

Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
Rin	Input Resistance	FM		70	100	130	kΩ
		AM		1.4	2	2.6	kΩ
GV	Stereo decoder input gain	min			0.5		dB
					2.25		dB
					4.0		dB
		max			5.75		dB
SVRR	Supply Voltage Ripple Rejection		Vripple = 100mV; f = 1KHz	35	60		dB
a	Max. channel Separation			30	45		dB
THD	Total Harmonic Distortion				0.02	0.3	%
(S+N)/N	Signal plus Noise to Noise Ratio		A-weighted, S = 2Vrms @ APout	80	91		dB

Table 25. Stereo decoder (continued)

(Vcc = 8V; deemphasis time constant = 50µs, VMPX = 305mVrms (75kHz deviation), fm= 1kHz, Gv = 4dB, Tamb = 27°C; unless otherwise specified)

Symbol	Parameter		Test condition	Min.	Typ.	Max.	Unit
Mono/stereo switch							
VPTHST1	Pilot Threshold Voltage		for Stereo, PTH = 1		15		mV
VPTHST0	Pilot Threshold Voltage		for Stereo, PTH = 0		25		mV
VPTHMO1	Pilot Threshold Voltage		for Mono, PTH = 1		12		mV
VPTHMOO	Pilot Threshold Voltage		for Mono, PTH = 0		19		mV
PLL							
Δf/f	Lock Range			-6		+6	%
f0	Center frequency range	min	VCO Vtuning fixed to reference voltage		328		kHz
		max			619		kHz
		step			9.4		kHz
PILmax	Maximum input pilot voltage		@TUNERIN	276			mV
Deemphasis and highcut							
τHC50	Deemphasis Time Constant		Bit 7, Subadr, 10 = 0, VLEVEL >> VHCH	25	50	75	µs
τHC75	Deemphasis Time Constant		Bit 7, Subadr, 10 = 1, VLEVEL >> VHCH	50	75	100	µs
τHC50	Highcut Time Constant		Bit 7, Subadr, 10 = 0, VLEVEL >> VHCL	100	150	200	µs
τHC75	Highcut Time Constant		Bit 7, Subadr, 10 = 1, VLEVEL >> VHCL	150	225	300	µs
Stereoblend and highcut control							
REF5V	Internal Reference Voltage			4.7	5	5.3	V
LGmin	Min. LEVEL Gain			-1	0	1	dB
LGmax	Max. LEVEL Gain			8	10	12	dB
LGstep	LEVEL Gain Step Resolution			0.3	0.67	1	dB
VSBLmin	Min. Voltage for Mono			25	29	33	%REF5V
VSBLmax	Max. Voltage for Mono			54	58	62	%REF5V
VSBLstep	Step Resolution			2.2	4.2	6.2	%REF5V
VHCHmin	Min. Voltage for NO Highcut			38	42	46	%REF5V
VHCHmax	Max. Voltage for NO Highcut			62	66	70	%REF5V
VHCHstep	Step Resolution			5	8.4	12	%REF5V
Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit

Table 25. Stereo decoder (continued)

(Vcc = 8V; deemphasis time constant = 50µs, VMPX = 305mVrms (75kHz deviation), fm= 1kHz, Gv = 4dB, Tamb = 27°C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VHCLmin	Min. Voltage for FULL Highcut		12	17	22	%VHCH
VHCLmax	Max. Voltage for FULL Highcut		28	33	38	%VHCH
VHCLstep	Step Resolution		2.2	4.2	6.2	%VHCH
Carrier and harmonic suppression at the output						
α19	Pilot Signal f = 19KHz		40	50		dB
α38	Subcarrier f = 38KHz				75	dB
α57	Subcarrier f = 57KHz				62	dB
α76	Subcarrier f = 76KHz				90	dB

2.5 Noise blanker

Table 26. Noise blanker

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
VTR	Trigger Threshold (1) (2)	meas. with V_{PEAK} = 0.9V	NBT = 111	(3)	30	(3)	mV
			NBT = 110	(3)	35	(3)	mV
			NBT = 101	(3)	40	(3)	mV
			NBT = 100	(3)	45	(3)	mV
			NBT = 011	(3)	50	(3)	mV
			NBT = 010	(3)	55	(3)	mV
			NBT = 001	(3)	60	(3)	mV
			NBT = 000	(3)	65	(3)	mV
VTRNOISE	Noise Controlled Trigger threshold (4)	meas. with VPEAK = 1.5V	NCT = 00	(3)	260	(3)	mV
			NCT = 01	(3)	220	(3)	mV
			NCT = 10	(3)	180	(3)	mV
			NCT = 11	(3)	140	(3)	mV
VRECT	Rectifier Voltage	VMPX = 0mV	NRD (8) = 00	0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		VMPX = 200mV; f = 150KHz		2.2	2.5	2.9	V

Table 26. Noise blanker (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
VRECT DEV	Deviation dependent rectifier Voltage (5)	Meas. with VMPX = 800mV (75KHz dev.)	OVD = 11	0.5	0.9	1.3	V
			OVD = 10	0.9	1.2	1.5	V
			OVD = 01	1.7	2	2.3	V
			OVD = 00	2.5	2.8	3.1	V
VRECT FS	Fieldstrength Controlled Rectifier Voltage (6)	Rectifier Voltage 4) V_{MPX} = 0mV V_{LEVEL} << V_{SBL} (fully mono)	FSC = 11	0.5	0.9	1.3	V
			FSC = 10	0.9	1.4	1.5	V
			FSC = 01	1.7	1.9	2.3	V
			FSC = 00	2.1	2.4	3.1	V
TS	Suppression Pulse Duration (7)	Signal HOLDN in Testmode	BLT = 00		38		µs
			BLT = 10		32		µs
			BLT = 01		25.5		µs
			BLT = 00		22		µs
VRECTADJ	Noise Rectifier discharge adjustment (8)	Signal PEAK in Testmode	NRD = 00 (8)	(3)	0.3	(3)	V/ms
			NRD = 01 (8)	(3)	0.8	(3)	V/ms
			NRD = 10 (8)	(3)	1.3	(3)	V/ms
			NRD = 11 (8)	(3)	2	(3)	V/ms
SRPEAK	Noise Rectifier Charge	Signal PEAK in Testmode	PCH = 0 (9)	(3)	10	(3)	mV/µs
			PCH = 1 (9)	(3)	20	(3)	mV/µs
VADJMP	Noise Rectifier adjustment through Multipath (10)	Signal PEAK in Testmode	MPNB = 00 (10)	(3)	0.3	(3)	V/ms
			MPNB = 00 (10)	(3)	0.5	(3)	V/ms
			MPNB = 00 (10)	(3)	0.7	(3)	V/ms
			MPNB = 00 (10)	(3)	0.9	(3)	V/ms

1. All thresholds are measured using a pulse with TR =2ms,THIGH = 2ms and TF = 10ms. The repetition rate must not icrease the PEAK voltage.
2. NBT represents the noiseblanker byte bits D2, D0 for the noise blanker trigger threshold.
3. By design/characterization functionally guaranteed through dedicated test mode structure.
4. NAT represents the noiseblanker byte bit pair D4, D3 for the noise controlled trigger adjustment.
5. OVD represents the noiseblanker byte bit pair D7, D6 for the over deviation detector.
6. FSC represents the fieldstrength byte bit pair D1, D0 for the fieldstrength control.
7. BLT represents the speaker RR byte bit pair D7, D6 for the blanktime adjustment.
8. NRD represents the configuration byte bit pair D1, D0 for the noise rectifier discharge adjustment.
9. PCH represents the stereo decoder byte bit D5 for the noise rectifier charge current adjustment.
10. MPNB represents the highcut byte bit D7 and the field strength byte D7 for the noise rectifier multipath adjustment

2.6 Multipath and quality detectors

Table 27. Multipath and quality detectors

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
fCMP	Center Frequency of Multipath Bandpass	Stereodecoder locked on Pilottone			19		kHz
GBPMP	Bandpass Gain	bits D_2, D_1 configuration byte = 00			6		dB
		bits D_2, D_1 configuration byte = 10			12		dB
		bits D_2, D_1 configuration byte = 01			16		dB
		bits D_2, D_1 configuration byte = 11			18		dB
GRECTMP	Rectifier Gain	bits D_7, D_6 configuration byte = 00			7.6		dB
		bits D_7, D_6 configuration byte = 01			4.6		dB
		bits D_7, D_6 configuration byte = 10			0		dB
		bits D_7, D_6 configuration byte = 11			off		
ICHMP	Rectifier Charge Current	bit D_5 configuration byte = 0			0.5		µA
		bit D_5 configuration byte = 1			1		µA
IDISMP	Rectifier Discharge Current			0.5	1	1.5	mA
A	Multipath Influence Factor	Addr. 12 / Bit 5+6	00		0.7		dB
			01		0.85		dB
			10		1		dB
			11		1.15		dB
B	Noise Influence Factor	Addr. 16 / Bit 1+2	00		15		dB
			01		12		dB
			10		9		dB
			11		6		dB

3 Functional description

3.1 FM section

3.1.1 Mixer1, AGC and 1st IF

Mixer1 is a wide dynamic range stage with low noise and large input signal performance. The mixer1 tank center frequency can be adjusted by software (IF1T). The AGC operates on different sensitivities and bandwidths (FMAGC) in order to improve the input sensitivity and dynamic range (keyed AGC). The output signals of AGC are controlled voltage and current for pre-amplifier and pre-stage PIN diode attenuator. Two 10.7MHz amplifiers (IFG1 - fixed gain - and IFG2 - programmable) correct the IF ceramic insertion loss.

3.1.2 Mixer2, limiter and demodulator

In this 2nd mixer stage the first 10.7MHz IF is converted into the second 450kHz IF. A multi-stage limiter generates signals for the complete integrated demodulator without external tank. MPX output DC offset compensation is possible via software.

3.1.3 Quality detection and ISS field strength

Parallel to the mixer2 input a 10.7MHz limiter generates a signal for the digital IF counter and a fieldstrength output signal. This internal unfiltered fieldstrength is used for adjacent channel and multipath detection. The behaviour of this output signal can be corrected for DC offset (SL). The internally generated unfiltered fieldstrength is filtered at pin #SMETERTC and used for softmute function, FM AGC keying and generation of ISS filter switching signal for weak input level (sm). (See *Figure 1.*)

3.1.4 Adjacent channel detector

The input of the adjacent channel detector is AC coupled to the internal unfiltered fieldstrength. A programmable and configurable highpass or bandpass filter (ACF) and amplifier (ACG) followed by a rectifier measure the adjacent channel content. This voltage is compared with an adjustable threshold (ACWTH, ACNTH) comparator (comparator1). The output signal of this comparator generates a DC level at PIN15 with a programmable time constant. Time constant control (TISS) for the adjacent channel is made by linearly charging and discharging an external capacitor following. The charge current is fixed and the discharge current is controlled by I^2C bus. This level produces digital signals (ac, ac+) after comparing by the following comparator4. The adjacent channel information after filtering and rectification is available as analog output on pin #TUNQUALITY (the gain can be selected via I^2C bus) in combination with multipath content information. It is possible to enable adjacent channel content information output only via I^2C bus control.

3.1.5 Multipath detector

The input of the multipath detector is AC coupled to the internal unfiltered fieldstrength. A programmable band-pass filter (MPF) and amplifier (MPG) followed by a rectifier measures the multipath content. This voltage is compared with an adjustable threshold (MPTH) comparator (comparator2). The output signal of this comparator2 is used to disable the adjacent channel detector control of the ISS filter in case of strong multipath, which would otherwise result in bandwidth reduction because of the multipath-induced high-frequency

content of the fieldstrength signal. The multipath detector influence on the adjacent channel detector is selectable by I^2C bus (MPOFF). The multipath information after filtering and rectification is available as analog output on pin #TUNQUALITY (the gain can be selected via I^2C bus) in combination with the adjacent channel content information. It is possible to enable multipath content information output only via I^2C bus control.

3.1.6 450kHz IF narrow bandpass filter (ISS filter)

The device features an additional automatically selectable IF narrow bandpass filter for suppression noise and adjacent channel signals. This narrow filter has three switchable bandwidth positions: narrow range (80kHz), mid range (120kHz) and weather band (30kHz). WHen the ISS filter is not inserted the IF bandwidth (wide range) is defined only by the ceramic filter chain. The filter is switched in after mixer2 before the 450kHz limiter stage. The centre frequency can be finely adjusted (AISS) by software.

3.1.7 Deviation detector

In order to avoid excessive audio distortion the narrow ISS filter is switched OFF when overdeviation of the incoming signal is detected. The demodulator output signal is low-pass filtered and rectified to generate a DC level in an external capacitor through a software-controlled current (TDEV). This level is compared with a programmable threshold (DWTH, DTH) comparator (comparator3) to generate two digital signals (dev, dev+).

3.1.8 ISS switch logic

All digital signals coming from adjacent channel detector, deviation detector and softmute are combined in a decision matrix to generate the control signals for the ISS filter switch. The IF bandpass switch mode can be also controlled by software (ISSON, ISS30, ISS80, ISSCTL). The switch-on of the IF bandpass can be further controlled from the outside by manipulation of the voltage at pin #ISSTC. Two application modes are available (APPM). The conditions are described in table 1.

3.1.9 Soft mute control

The external fieldstrength signal at pin #SMETERTC is the reference for MPX mute control. The start point and mute depth are programmable over a wide range. The time constant is defined by the external capacitor connected to pin #FMMUTETC.

Additionally adjacent channel mute function is supported. A software-configurable highpass / bandpass filter centered at about 100kHz followed by an amplifier and a peak rectifier generates adjacent noise information starting from the MPX output; the information is acted upon with the same time constant as the softmute by the MPX muting circuit. The adjacent channel mute starting point, slope and depth are I^2C bus programmable.

3.1.10 Station detector and seek stop

A station detection function is provided for easy seek stop operation. The unfiltered fieldstrength signal is compared with a programmable threshold and the result (logic '1' if the current station strength is higher than the threshold) is combined by an AND gate with the IF counter output (logic '1' if the current channel is centered within a programmable window around the desired frequency). The result is available on pin #SD for direct connection to the microprocessor. Channel quality assessment for RDS Alternate Frequency operation makes use of the SD signal in conjunction with analog information on adjacent channel and

multipath content on pin #TUNQUALITY and channel noise (furtherly combined with multipath content information) on pin #QUALITY.

3.2 AM section

The upconversion mixer1 is combined with a gain control circuit 1 sensing three input signals: ultra-narrow band information (from the IF2 amplifier input - pin #AMIF2AMPIN), narrow-band information (from the mixer2 input - pin #AMMIX2IN) and wide band information (from the mixer1 input - pins #AMMIX1IN+ and #AMMIX1IN-). This gain control circuit generates two output signals: a current for P-I-N diode attenuation and a voltage for the external preamplifier cascode upper base. It is possible to put in a separate narrow bandpass filter before mixer2 at PIN 58. The intervention point for first AGC on all three bands is programmable by software.

The oscillator frequency for mixer1 is generated by dividing the FM VCO frequency (AMD) by 6, 8 and 10 (6 for Japan applications, 8 for Eastern European applications, 10 for Western European and North American operation).

In mixer2 the IF1 is downconverted into the 450kHz IF2. The gain of mixer2 is reduced by the 2nd AGC after the gain of the subsequent IF2 amplifier has been reduced by 30dB. The mixer2 tank center frequency is software-adjustable (IF2T).

After channel selection is done by the ceramic filter, a 450kHz amplifier with a gain control is included. The gain is controlled by the AGC2 loop over a 30dB range; the full gain with no AGC applied is programmable.

The AM demodulation is made by multiplication of the IF2 amplifier output by the amplified and limited signal coming from the IF2 amplifier input, thus making the demodulation process inherently linear.

The demodulated audio signal is low-passed by the capacitor at pin #AMAGC2TC to produce the DC AGC2 voltage. The low-pass time constant is switchable by a ratio of 30 in order to reduce the settling time of the AGC2 in 'seek' mode (AMSEEK).

The FM 450kHz limiter is used to generate the square wave needed by the AM demodulator, a fieldstrength indication and to feed the AM IF counter. The fieldstrength information is generated mainly from the narrow-band signal at the input of the IF2 amplifier; since the dynamic range at that input is limited by the AGC2 action, a fieldstrength extension is made adding the contribution of the signal at the input of mixer2. Since the bandwidth there is very large, though, the latter contribution is enabled only if the strength of the narrow-band signal is higher than an internally defined threshold. The fieldstrength signal must be low-passed to remove audio content and this is done by use of the capacitor at pin #SMETERTC with an I^2C bus programmable internal resistor. The value of the capacitor is determined for correct FM operation; the value of the internal resistor for AM is selectable in order to make the AM time constant suitable for AM operation.

A station detection function is provided for easy seek stop operation. The fieldstrength signal is compared with a programmable threshold and the result (logic '1' if the current station strength is higher than the threshold) is combined by an AND gate with the IF counter output (logic '1' if the current channel is centered within a programmable window around the desired frequency). The result is available on pin #SD for direct connection to the microprocessor.

3.3 PLL and IF counter section

The IC contains a frequency synthesizer and a loop filter for the radio tuning system. Only one VCO is required to build a complete PLL system for FM and AM upconversion. For auto search stop operation an IF counter system is available.

3.3.1 PLL frequency synthesizer block

The counter works in a two stages configuration. The first stage is a swallow counter with a two-modulus (32/33) precounter. The second stage is an 11-bit programmable counter. The circuit receives the scaling factors for the programmable counters and the values of the reference frequency via I^2C bus. The reference frequency is generated by an adjustable internal (XTAL) oscillator followed by the reference divider. The reference and step-frequencies are independently selectable (RC, PC). The phase-frequency detector outputs switches the programmable current source. The loop filter integrates the latter to a DC voltage. The current source values is programmable with 6 bits received via I2C bus (A, B, CURRH, LPF). To minimize the noise induced by the digital part of the system, a special guard area is implemented. The loop gain can be adjusted for different conditions by setting the current values of the chargepump generator.

3.3.2 Frequency generation for phase comparison

The VCO signal is fed to a two-modulus counter (32/33) prescaler, which is controlled by a 5-bit divider (A). A 5-bit register (PC0 to PC4) controls this divider. The output of the prescaler is connected to an 11-bit divider (B), controlled by an 11-bit PC register (PC5 to PC15).

The following expressions relate the divider output frequency (f_{SYN}, forced by the loop to equal the reference frequency at the phase comparator input f_{REF}) to the VCO frequency (f_{VCO}) and to the crystal oscillator frequency (f_{XTAL}):

$f_{XTAL} = (R+1) \times f_{REF}$

$f_{VCO} = [33 \times A + (B + 1 - A) \times 32] \times f_{REF}$

$f_{VCO} = (32 \times B + A + 32) \times f_{REF}$

Important: For correct operation: $A \leq 32$; $B \geq A$

3.3.3 Three state phase comparator

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

3.3.4 Charge pump current generator

This system generates correction current pulses with a polarity and a duration dictated by the phase error signal. The current absolute values are programmable through register A for high current and register B for low current.
The charge pump operates in high current mode when the phase difference between between f_{SYN} and f_{REF} is high. The switch back to low current mode can be done either automatically as a function of the inlock detector output (setting bit LDENA to "1") or via software.
After reaching a phase difference equivalent to 10-40 ns (programmable) and a delay multiple of $1/f_{REF}$, the chargepump is forced in low current mode. A new PLL divider programming by I^2C bus will switch the chargepump into high current mode.

A few programmable phase errors (D0, D1) are available for inlock detection. The count of detected inlock informations to release the inlock signal is adjustable (D2, D3), to avoid switching to low current during a frequency jump.

3.3.5 Low noise CMOS op-amp

An internal voltage divider at pin #LFREF is connected to the positive input of the low noise op-amp. The charge pump output is connected to the negative input. This internal amplifier in cooperation with external components provides the active loop filter. Only one loop filter connection is provided because the same reference frequency is used for both AM and FM operation. The pin #LFHC is connected in such a way as to partially shunt the loop filter in order to decrease the time constant of the filter itself during jumps with high current mode activated.

3.3.6 IF counter block

The input signal for FM and AM has the same structure although FM IF is measured at IF1 (10.7MHz) and AM IF is measured at IF2 (450kHz). The degree of integration is adjustable to up to eight different measuring cycle times. The tolerance of the accepted count value is adjustable to reach the optimum compromise between search speed and evaluation precision.

T center frequency of the measured count value is adjustable to fit the IF-filter tolerance.

3.3.7 The IF counter mode

The IF counter works in 2 modes controlled by the IFCM register.

3.3.8 Sampling timer

A 14-bit programmable (IRC) sampling timer generates the gate signal for the main counter. In FM mode a 6.25kHz frequency reference is generated for this purpose, whereas in AM mode this reference becomes 1kHz. These reference frequencies are further divided to generate the measurement time windows (160us - 320µs ... 20.48ms for FM, 1ms - 2ms … 128ms for AM).

3.3.9 Intermediate frequency main counter

This counter is a 11 - 21-bit synchronous autoreload down counter. Five bits (CF) are programmable to allow the adjustment to the peak of the IF-filter response. The counter length is automatically adjusted to the chosen sampling time and counter mode (FM, AM).

The IF counter is also used to automatically perform the stereo decoder 456kHz VCO frequency adjustment.

At the start the counter will be loaded with a value equivalent to the expected number of zero-crossing in the sampling time window (t_{Sample} x f_{IF}). If the correct frequency is applied to the IF counter input, at the end of the sampling time the main counter will have either a 0h state or a 1FFFFFh state stored.

A deviation from the expected IF will result in a difference of the counter final state from either of these values. The counter final state is then compared to either 0h or 1FFFFFh minus a number of LSB's determined by the acceptable frequency window programming (EW).

If the comparison result is good the IF counter output changes from LOW to HIGH and is made available outside at the pin #SD (after a NAND operation with the signal strength evaluation circuit). The following relationships apply:

t_{TIM} = (IRC + 1) / f_{OSC}

t_{CNT} = (CF + 1697) / f_{IF} (FM mode)

t_{CNT} = (CF + 448) / f_{IF} (AM mode)

where

t_{TIM} = IF timer cycle time (sampling time)

t_{CNT} = IF counter cycle time

Counting succesful:

$t_{CNT} - t_{ERR} = t_{TIM} = t_{CNT} + t_{ERR}$

Count failed:

$t_{TIM} > t_{CNT} + t_{ERR}$

$t_{TIM} < t_{CNT} - t_{ERR}$

where

t_{ERR} = discrimination window (controlled by the EW registers)

The IF counter can be started only by inlock information from the PLL, and it is enabled by software (IFENA).

3.3.10 Adjustment of the measurement time and frequency window

The measurement precision is adjustable by controlling the width of the frequency discrimination window through control registers EW0 to EW2. The center frequency of the discrimination window is adjustable by the control register CF0 to CF4. The measurement time per cycle is adjustable by setting the registers IFS0 - IFS2.

3.4 Audio processor

3.4.1 Input multiplexer

CD quasi differential 1

CD quasi differential 2

Stereodecoder input (for both FM and AM signals).

3.4.2 Input stages

The quasi-differential input stages (see *Figure 2.*) have been designed to cope with some CD players in the market having a significant high source impedance which affects strongly the common-mode rejection of "normal" differential input stages. The additional buffer of the CD input avoids this drawback and offers the full common-mode rejection even with those CD players. The quasi-differential input can also be used with normal stereo single-ended output signal sources such as TAPEOUT.

3.4.3 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that in theory any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid this undesired situation a special offset cancellation stage called AutoZero is implemented. This stage is located before the Volume block to eliminate all offsets generated by the Stereodecoder, the Input Stage and the In-Gain stage (please note that externally generated offsets, e.g. those generated because of leakage current into the coupling capacitors, are not cancelled).

The auto-zeroing is started every time the APSD data byte 0 is selected and takes a maximum time of 0.6ms. The rationale behind this choice is that the APSD byte encodes the signal source selection, and auto-zero ought to be performed every time a new source is selected. To avoid audible clicks the audioprocessor is muted before the volume stage during this time.

3.4.4 AutoZero remain

In some cases, for example if the uP is executing a refresh cycle of the I^2C bus programming, it is not necessary to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the device can be switched in the "AutoZero Remain mode" (Bit 6 of the APSD subaddress byte). If this bit is set to high, the APSD data byte 0 can be loaded without invoking the AutoZero and the old adjustment value remains.

3.4.5 Softmute

The digitally controlled softmute stage allows signal muting and unmuting with a I^2C bus programmable slope. The mute process can either be activated by pin #AUDIOMUTE or I^2C bus. The slope is realized in a special S-shaped curve so as to slowly mute in the critical regions (see *Figure 4.*). For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of unmuting.

3.4.6 BASS

There are four parameters programmable in the bass filter stage: (see *Figure 5*, *6*, *7*, and *8*):

3.4.7 Attenuation

Figure 5 shows the attenuation as a function of frequency at a center frequency at a center frequency of 80Hz.

3.4.8 Center frequency

Figure 6 shows the four possible center frequencies: 60,70,80 and 100Hz.

3.4.9 Quality factors

Figure 7 shows the four possible quality factors: 1, 1.25, 1.5 and 2.

3.4.10 DC Mode

In this mode the DC gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25%: this can be used to realize different center frequencies or quality factors with respect to the values listed in the "BASS" section.

3.4.11 MID

There are 3 parameters programmable in the mid filter stage (see *Figure 9*, *10* and *11*):

3.4.12 Attenuation

Figure 9 shows the attenuation as a function of frequency at a center frequency of 1kHz.

3.4.13 Center frequency

Figure 10 shows the four possible center frequencies: 500Hz, 1kHz, 1.5kHz and 2kHz.

3.4.14 Quality factor

Figure 11 shows the two possible quality factors (1 and 2) at a center frequency of 1kHz.

3.4.15 TREBLE

There are two parameters programmable in the treble filter stage (see *Figure 12*, *13*):

3.4.16 Attenuation

Figure 12 shows the attenuation as a function of frequency at a center frequency of 17.5kHz.

3.4.17 Center frequency

Figure 13 shows the four possible Center Fre-quencies: 10, 12.5, 15 and 17.5kHz.

3.4.18 AC coupling

In some applications additional signal manipulations are desired such as surround-sound processing or more extensive band equalizing. For this purpose a AC-Coupling is placed before the Speaker-attenuators, which can be activated or internally shorted by Bit7 in the APSD data byte 0. The input impedance of the AC Inputs is 25kΩ. The external AC coupling is advised for those applications where very low-level "pop" performance is a must.

3.4.19 Speaker attenuator

The speaker attenuators have exactly the same structure and range as the Volume stage.

3.5 Stereo decoder

The stereo decoder part of the present device (see *Figure 14*) contains all functions necessary to demodulate the MPX signal such as pilot tone-dependent MONO/STEREO switch as well as "stereoblend" and "highcut" functions.

3.5.1 Stereo decoder mute

The device has a fast and easy-to-control RDS mute function meant for "freezing" the stereo decoder status during the RDS AF check time period. When this function is invoked three effects take place:

1. The stereo decoder input impedance changes to infinity (condition known as high-ohmic input); this prevents the decoupling capacitor between the pins #TUNER_OUT (tuner output) and #TUNER_IN (stereo decoder input) to be discharged by a channel with a potentially different DC output for the duration of the AF check;
2. The stereo decoder PLL pilot detector is held at the current value;
3. The external capacitor of the multipath detector used inside the stereo decoder for quality control is disconnected from the dection circuit in order to make quality checking the AF faster.

The RDS mute is activated from pin #RDSMUTE in AND with Bit 0 of APSD data byte 9.

3.5.2 Stereo decoder Input stage, Ingain + Infilter

The stereo decoder is crossed by both the FM and the AM signal: the input impedance of the pin #TUNER_IN is different between the two modes in order to allow the same external coupling components between #TUNER_OUT and #TUNER_IN to realize different filtering functions. Whilst the input impedence in FM is 100k , in AM the input impedance is decreased to 2kΩ: this allows the realization of typical high-pass filters with a corner frequency of 70Hz for AM and less than 5Hz for FM. The low-pass section of the typical AM transfer function is realized by use of the internal FM High-Cut filter.

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and nose and acts as an anti aliasing filter for the following switch capacitor filters.

3.5.3 Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage the 19 kHz pilot tone is cancelled.

To reach a good channel separation the device offers an I^2C bus programmable roll-off adjustment which is able to finely compensate for the low-pass behaviour of the tuner section. An adjustment to better than 40dB channel separation is possible. The bits for this adjustment are located ogether with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation in relation to the fieldstrength control are trimmed.

The setup of the Stereoblend characteristics, which is fully programmable, is de-scribed in *Chapter 3.5.8*.

3.5.4 De-emphasis and highcut.

One filter is provided to realize de-emphasis and High-Cut filtering.

The lowpass filter for the de-emphasis allows to choose between a time constant of 50µs and 75µs.
The filter time constant can further be controlled in both cases over the range = 2 DEEMPH.
The control is automatically performed as a function of the filtered field strength level: inside

the highcut control range (between VHCH and VHCL) the level is converted into a 5 bit word which drives the lowpass time constant. The FM highcut function can be switched off by I^2C bus (bit 0,of APSD data byte 11). The setup of the highcut characteristics is described in 2.9.

In AM the high-cut filter can be programmed (bit 3 to 7 of APSD data byte 16) to a fixed value (inside the above-mentioned programmable range) in order to provide the desired lowpass characteristic of the AM signal.

3.5.5 PLL and pilot tone detector

The PLL is tasked with locking on the 19kHz pilot tone during a stereo transmission to allow the correct demodulation. The detector enables the stereo demodulation if the pilot tone reaches the selected pilot tone threshold VPTHST. Two different thresholds are available. The detector output can be checked by reading the status byte of the TDA7407 via I^2C bus.

3.5.6 Fieldstrength control

The filtered field strength signal is fed to the stereo decoder where it can be finely adjusted and normalized so that it can be used to control the highcut and stereoblend functions. Furthermore the adjusted signal can also be used to control the noise-blanker thresholds. The unfiltered field strength meter, on the other hand, is used as input for the stereo decoder multipath detector. These additional functions are described in sections 3.3 and 4.

3.5.7 LEVEL input and gain

To help suppress undesired high frequency modulation of the highcut and stereoblend functions the tuner filtered field strength signal (LEVEL) is lowpassed by a combination of a 1st order RC low-pass at 53kHz (working as anti-aliasing filter) and a 1st-order switched capacitor lowpass at 2.2kHz.
The second stage is a programmable gain stage to finely adapt the LEVEL signal internally against tuner spread (see Testmode section 5 LEVELINTERN). The gain is widely programmable in 16 steps from 0dB to 10dB (step = 0.67dB).

3.5.8 Stereoblend control

The stereoblend control block converts the internal LEVEL voltage (LEVELINTERN) into a demodulator-compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. This control range has a fixed upper limit which is the in-ternal reference voltage REF5V. The lower limit

can be programmed between 29.2% and 58% of REF5V in 4.167% steps (see *Figure 17*).

To adjust the LEVEL voltage to the proper range two values must be defined: the LEVEL gain LG and VSBL (see *Figure 17*). To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain L_G has to be defined. The following equation can be used to estimate the gain:

$$L_G = \frac{REF5V}{Fieldstrengthvoltage[STEREO]}$$

The gain L_G can be programmed with 4 bits. The MONO voltage VMO (0dB channel separation) can be chosen selecting VSBL. All the necessary internal reference voltages

like REF5V are derived from a bandgap circuit, therefore they have a temperature coefficient which is practically zero.

3.5.9 Highcut control

The highcut control setup is similar to the stereoblend control setup, the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17, 22, 28 or 33% of VHCH (see *Figure 18*).

3.5.10 Noise blanker

In the automotive environment the MPX signal is disturbed by spikes produced for example by the ignition and by the wiper motor. The aim of the noiseblanker part is to cancel the audible influence of these spikes. To perform this function the output of the stereo decoder is held at the curent voltage for a time between 22 and 38µs (programmable). The block diagram of the noiseblanker is shown in fig.20. In the first stage the spikes are detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger desensitization control is implemented. Behind the trigger stage a pulse former generates the "blanking" pulse

3.5.11 Trigger path

The incoming MPX signal is highpassed by a filter with a corner frequency of 140kHz, amplified and rectified. The rectified signal (RECT) is lowpassed to generate the signal PEAK. Also noise at a frequency higher than 140kHz increases PEAK. The lowpass output voltage can be adjusted by changing the noise rectifier discharge current. The PEAK voltage is fed to a threshold generator which adds to the PEAK voltage a constant voltage VTH, thus producing the trigger threshold PEAK+VTH. Both RECT and PEAK+VTH are fed to a comparator which trig-gers a re-triggerable monoflop. The monoflop output activates the sample-and-hold circuits in the signalpath for a selectable duration.

3.5.12 Automatic noise controlled threshold adjustment (ATC)

There are mainly two independent possibilities to program the trigger threshold:

a) Programming the so-called "low threshold" in 8 steps;

b) Programming the so-called "noise adjusted threshold" in 4 steps

The "low threshold" is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operating mode is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular mechanism ("noise adjusted threshold") is programmable in 4 steps.

3.6 Automatic threshold control mechanism

3.6.1 Automatic threshold control by the stereoblend voltage

Besides the noise controlled threshold adjustment there is an additional possibility to influence the trigger threshold which depends on the stereoblend control.
The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise controlled trigger adjustment is fixed. In some

cases the behavior of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occures for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold. Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereoblend.
This threshold increase is programmable in 3 steps or switched off.

3.6.2 Over deviation detector

If the system is tuned to stations with a high de-viation the noiseblanker might be erroneously triggered on the higher frequencies of the modulation. To avoid this unnecessary muting of the signal, the noiseblanker offers a deviation-dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. This is used to increase the PEAK voltage. The circuit offset, gain (and enabling) are programmable in 3 steps.

3.7 Multipath detector

Using the stereo decoder multipath detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19kHz spectrum in the fieldstrength signal. An external capacitor is used to define the attack and decay times (see *Figure 20*). The pin #MULTIPATHTC is externally connected to a capacitor of about 47nF and the MPIN signal is internally connected to the unfiltered field strength. To avoid losing the information stored in the external capacitor during AF checks but at the same time to allow some fast multipath detection capability during the same AF check period, the external capacitor is disconnected by the MP-Hold switch. This switch is controlled directly by the pin #RDSMUTE.

Moreover, selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the pin #MULTIPATHTC.

3.7.1 Programming

To obtain a good multipath performance an adaptation is necessary. Therefore tha gain of the 19kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by properly choosing the value of the external capacitor.

3.8 Quality detector

The device offers a quality detector output voltage representing the quality of the FM reception conditions. This voltage is derived from MPX noise information and multipath information according to the following formula:

$$\text{Quality} = 1.6\ (V_{noise} - 0.8V) + a\ (REF5V - V_{MPOUT})$$

The noise signal is the PEAK signal of the noise blanker without additional influences. The multipath information weight "a" can be programmed between 0.7 and 1.15. The circuit output pin #QUALITY is a low impedance output able to drive external circuitry as well as suitable to be simply fed to an A/D converter for RDS applications.

3.8.1 AF search control

The device is supplied with several functionality to support AF checks using the stereo decoder. As already mentioned before the high ohmic mute feature at the stereo decoder input avoids any clicks during the jump condition.

It is possible at the same time to evaluate the noise and multipath content of the alternate frequency by using the Quality detector output. During this time the multipath detector is automatically switched to a small time constant.

One dedicated pin (#RDSMUTE) is provided in order to separate the audioprocessor-mute and stereodecoder AF-functions.

3.9 I^2C bus interface

I^2C bus protocol is supported. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver.

The device that controls the transfer is a master and device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations. The present device always acts as slave, both in transmission and in reception mode.

3.9.1 Data transition

Data transition on the SDA line must only occur when the clock SCL is LOW. SDA transitions while SCL is HIGH will be interpreted as START or STOP condition.

3.9.2 Start condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This "START" condition must precede any command and initiate a data transfer onto the bus. The device continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

3.9.3 Stop Condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus interface of the device into the initial condition.

3.9.4 Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it received the eight bits of data.

3.9.5 Data transfer

During data transfer the device samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

3.9.6 Device addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device.

The device recognizes the following two addresses:

- 1100010d tuner part address
- 1000110d stereo decoder / audio processor address (APSD)

The last bit of the start instruction defines the type of operation to be performed:

- when set to "1", a read operation is selected (data are transferred from the device to the master)
- when set to "0", a write operation is selected (data are transferred from the master to the device)

The device connected to the bus will compare its own hardwired addresses with the slave address being transmitted after detecting a START condition.

After this comparison, the device will generate an "acknowledge" on the SDA line and will perform either a read or a write operation according to the state of the R/W bit.

3.9.7 Write operation

Following a START condition the master sends a slave address word with the R/W bit set to "0". The device will generate an "acknowledge" after this first transmission and will wait for a second word (the subaddress field).

This 8-bit address field provides an access to any of the 64 internal addresses (32 corresponding to the tuner address and 32 corresponding to the stereo decoder / audio processor address). Upon receipt of the subaddress the device will respond with an "acknowledge".

At this time, all the following words transmitted to the device will be considered as Data.

The internal address may be automatically incremented if the auto-increment mode is selected (bit S5 of the subaddress word) .

After each word has been received the device will answer with an "acknowledge".

3.9.8 Read operation

IF the master sends a slave address word with the R/W bit set to "1", the device will transmit one 8-bit data word.

This data word content changes according to the address corresponding to the tuner or to the stereo decoder / audio processor. The information are the following:

Tuner

bit0: ISS filter, 1 = ON, 0 = OFF

bit1: ISS filter bandwidth, 1 = 80kHz, 0 = 120kHz

bit2: MPOUT,1 = multipath present, 0 = no multipath

bit3: 1 = PLL is locked in , 0 = PLL is locked out

bit4: fieldstrength indicator, 1 = lower than softmute; 0 = higher than softmute threshold

bit5: adjacent channel indicator, 1 = adjacent channel present, 0 = no adjacent channel

bit6: deviation indicator, 1 = strong overdeviation present, 0 = no strong overdeviation

bit7: deviation indicator, 1 = overdeviation present, 0 = no overdeviation

Stereo decoder / audio processor

bit2: Soft Mute status, 1 = ON, 0 = OFF

bit3: Stereo mode, 1 = stereo, 0 = mono

Table 28. ISS Modes 1

sm	ac	ac+	dev	dev+	ISSon	80KHz
0	0	0	0	0	0	0
0	1	X	0	0	1	1
0	1	X	1	X	1	0
1	X	X	0	0	1	1
1	0	0	1	X	0	0
1	1	X	1	X	1	0

Table 29. ISS Modes 2

sm	ac	ac+	dev	dev+	ISSon	80KHz
0	0	0	0	0	0	0
0	1	0	0	0	1	0
0	1	1	X	X	1	1
0	1	0	1	X	1	0
1	X	X	0	0	1	1
1	0	0	1	X	0	0
1	1	0	1	X	1	0
1	1	1	1	X	1	1

Figure 4. Softmute timing

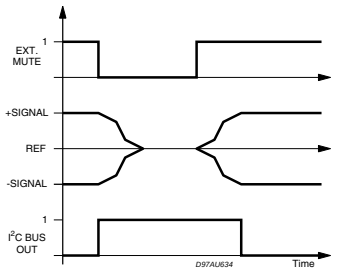


Figure 5. Bass control @ Fc = 80Hz, Q = 1

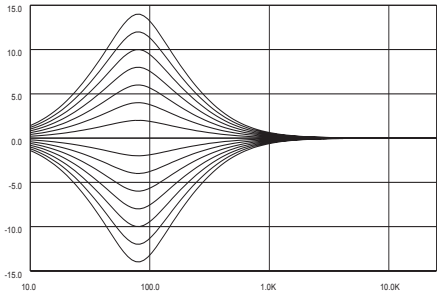


Figure 6. Bass center @ Gain=14dB Q=1

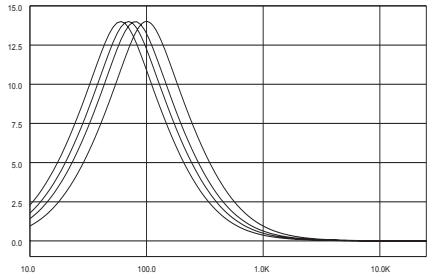


Figure 7. Bass quality factors @ Gain = 14dB, fc = 80Hz

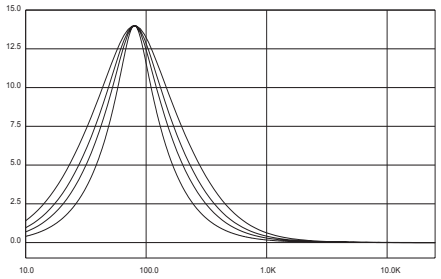


Figure 8. Bass normal and DC mode @ Gain = 14dB, fc = 80Hz

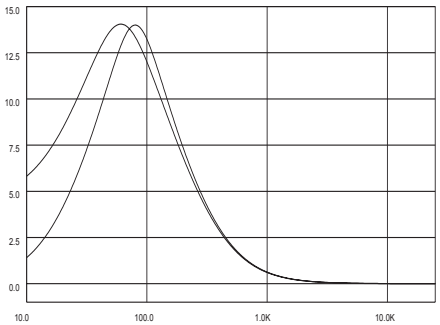


Figure 9. Mid control @ fc = 1KHz, Q = 1

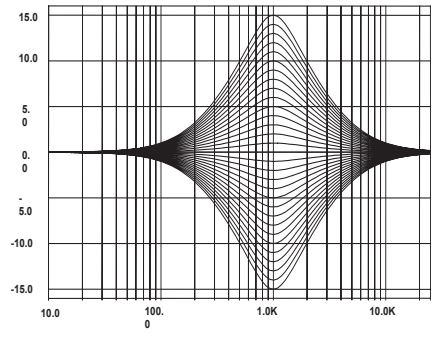


Figure 10. Mid center frequency @ Gain =14dB, Q = 1

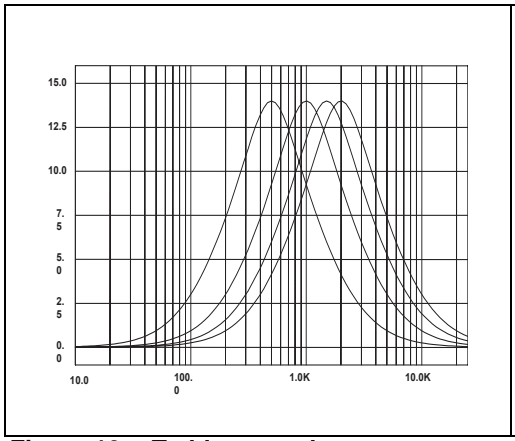


Figure 11. Mid Q factor @ fc=1KHz, Gain =14dB

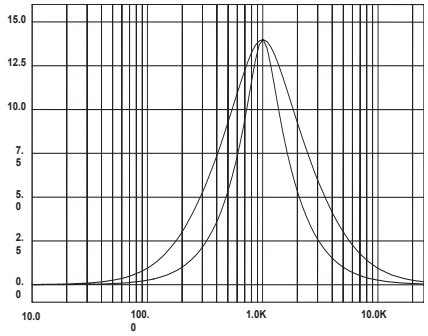


Figure 12. Treble control @ fc = 17.5KHz

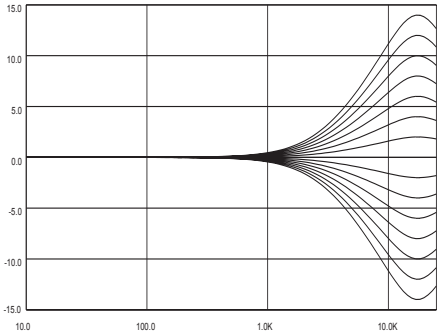


Figure 13. Treble center frequencies @ Gain = 14dB

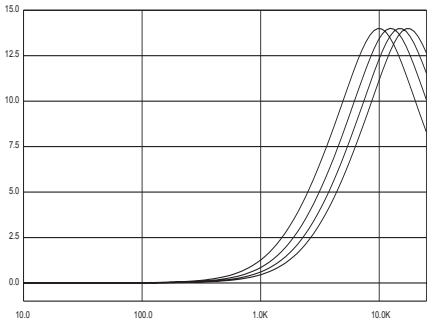


Figure 14. Block diagram of the stereo decoder

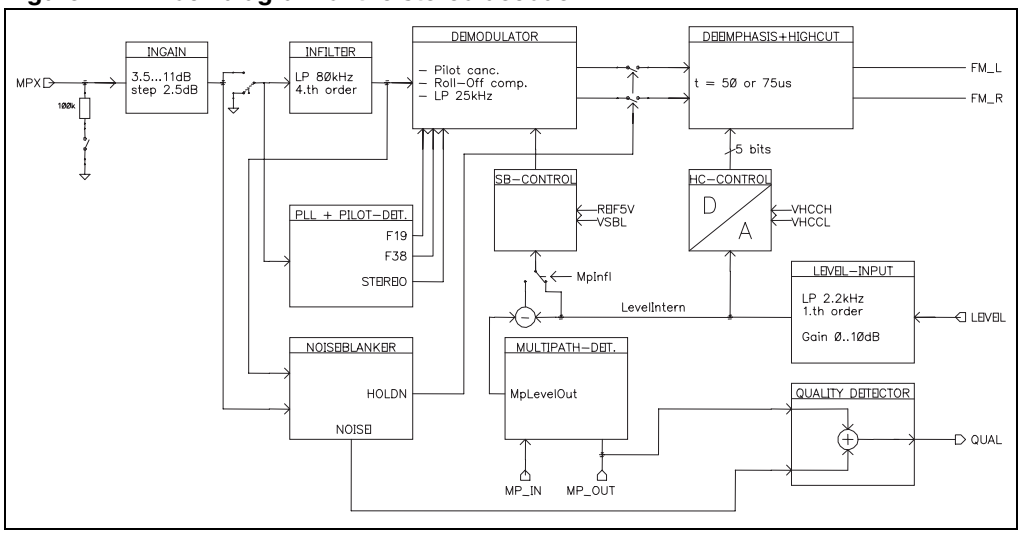


Figure 15. Signal during stereo decoder's softmute

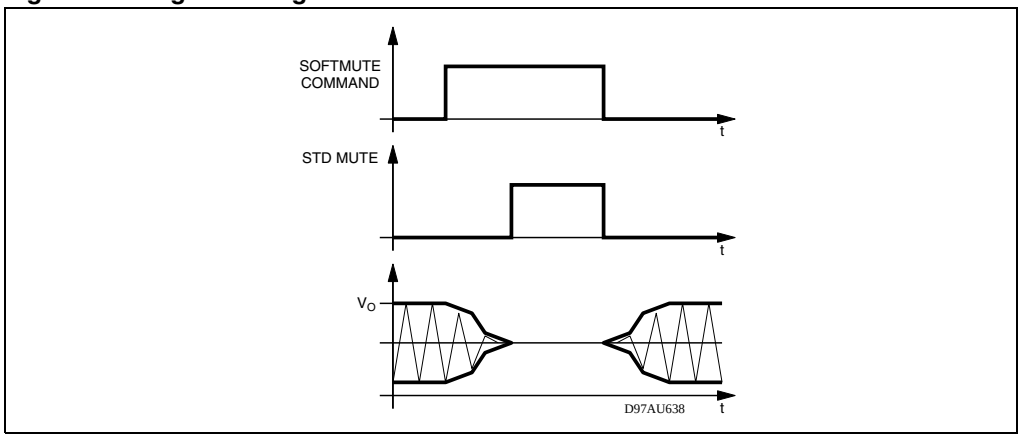


Figure 16. Internal stereo blend characteristics

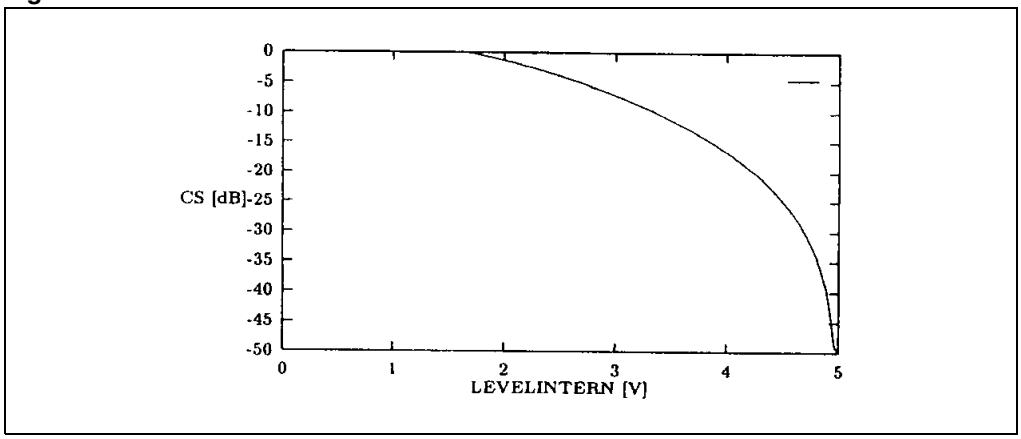


Figure 17. Relationship between unadjusted (LEVEL) and adjusted (LEVELITERN) filtered field strength signals

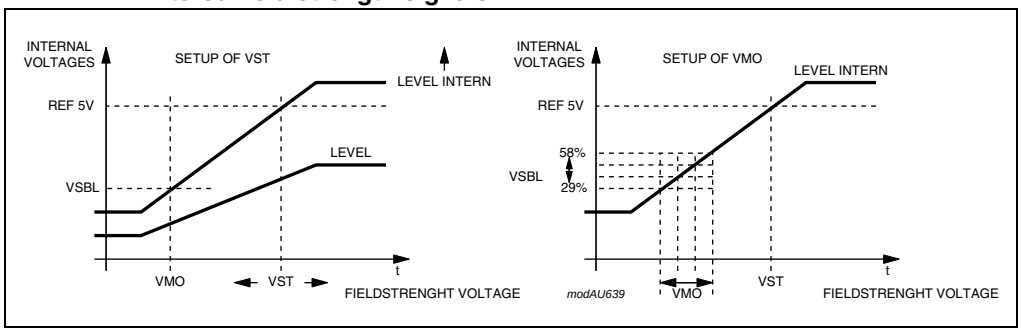


Figure 18. Highcut characteristics

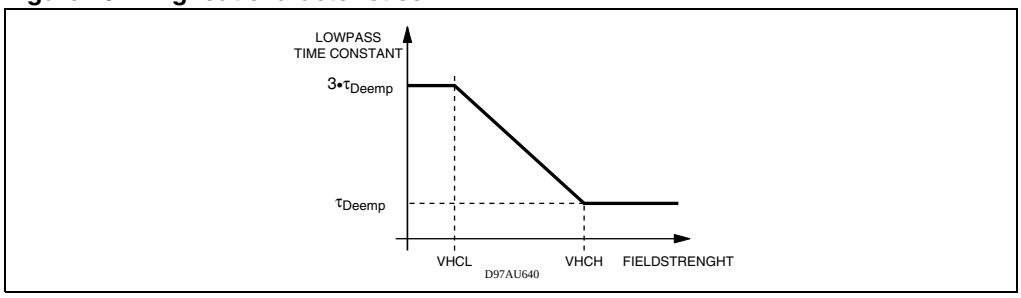


Figure 19. Noise blanker block diagram

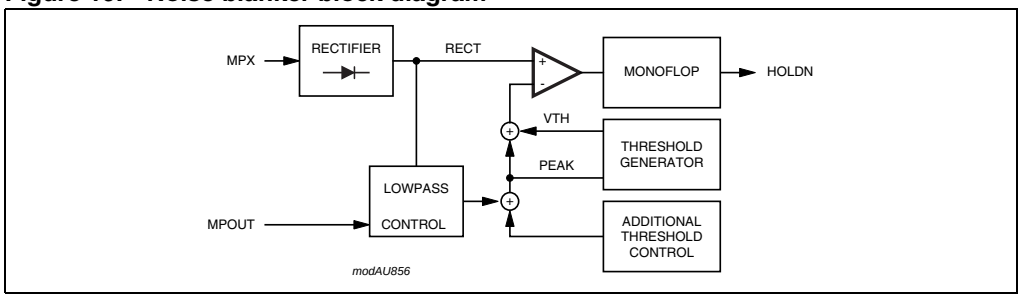
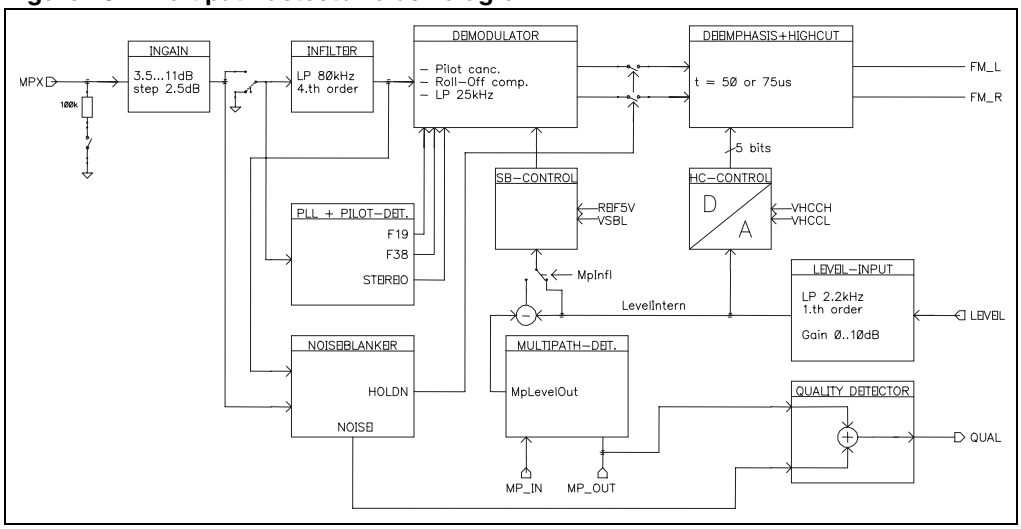


Figure 20. Multipath detector block diagram



4 Software specifications

4.1 Tuner section address organization

Table 30. Address organization (tuner section)

	MSB							LSB	Function
Subaddr.	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
0	STBY	Current select	Low current		High current				Charge Pump Control and STBY
1	Lock detainable	activation delay		Phase difference threshold		AM/FM	fref BYPASS	VCOadj clockenab	PLL Lock Detector, FM mode and tests
2	counter LSB								PLL Counter 1 (LSB)
3	counter MSB								PLL Counter 2 (MSB)
4	counter LSB								PLL Reference Counter 2 (LSB)
5	counter MSB								PLL Reference Counter 2 (MSB)
6	FM ISS DD disable thr @ weak FS	FM audio amp. mute depth		FM antenna adjustment					FM Antenna Adjustment and FM Mute Depth
7	SEEK	AM prescaler		FM RF adjustment					FM RF Adjustment, AM prescaler and Seek
8	AM stop station				IFC enable	Df			IF Counter Control 1 and AM S.S. Threshold
9	t_{SAMPLE}			t_{CENTER}					IF Counter Control 2 (central frequency and sampling time)
10	counter LSB								IF Counter Reference (LSB)
11	IFC AM/FM		counter MSB						IF Counter Reference (MSB) and IF Counter Mode Select
12	AMUNAGC					AMIF2amp			AM Ultra Narrow AGC Thresh., AM IF2 Amplifier Gain, FM Softmute Enable and AC test
							test ACmute	FM SMut enable	
13	MPQUAL test	FM demod noise blanker		FM demodulator fine adjust					FM demodulator Adjust, FM demod noise blanker and MP test
		AM Smeter extens							

Table 30. Address organization (tuner section) (continued)

	MSB							LSB	Function
Subaddr.	D7	D6	D5	D4	D3	D2	D1	D0	
14	ISS AC narrowband threshold		ISS AC wideband threshold			ISS AC gain	ISS AC HP/BP	ISS 30KHz on	Quality Detection Adjacent Channel
15	ISS MP defeat AC	ISS mode		ISS MP threshold		test Smet unfiltered	ISS MP center	ISS MP ctrl on	Quality Detection Multipath
16	0	ISS DD off threshold		ISS DD narrow/wide threshold		ISS DD time constant			Quality Detection Deviation
17	ISS center		ISS time constant			ISS 80/120	ISS on	ISS enable	Quality ISS Filter
18	SO mode		ISS MP gain		VCO adj start	test PLL			PLL test, 456KHz VCO adiustment start (auto mode)
19	Manual / auto	Manual VCO frequency					man SET 456	man ENIFC	456KHz VCO adjustment (manual mode)
20	FM stop station				FM soft mute				FM Stop Station and soft Mute Thresholds
21	AC QUAL test	AdjChan mute clamp				AdjChan mute gain			Adjacent mute gain, clamping threshold and test
22	AM Smeter filter TC			FMSmslider					FM Smeter slider and AM Smeter filter Time Constant
23	IFT2 adjust				IFT1 adjust				IFT1 adjust
24	FMIFamp2		Clkse p	XTAL adjustment					XTAL adjustment and FM IF Amp2
25	AMWAGC					FMNAGCkey			AM WAGC an FM MAGC keying
26	AMNAGC					FM demod ref frequency divider			AM NAGC an FMdemod ref frequency divider
27	test ISS								ISS testing
28	ISS filter test		test ISS MP/AC		Test ISS				ISS testing
29	Smeter pin test		test TURNER						Tuner and Smeter test
30	AdjChan mute disable @ low FS		AdjChan mute BP/HP		AdiChan mute threshold				AdjChan mute disable, filtering and threshold
31	Turner quality AdjChan gain		Turner quality multipath gain		FS ISS activation				Tuner Quality AdjChannel and Multipath gain, FS ISS Activation

Table 31. Address organization addresses

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	1	0	R/W

Table 32. Address organization subaddress

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
X	X	autoincr	subaddress				

Table 33. Address organization read mode: ISS outputs

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
DEV+	DEV	AC	FS	INLOCK	MP	BW	ON

4.2 Tuner section subaddresses

Table 34. Subaddress organisation (tuner section)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Charge pump
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1mA
				0	0	1	1	High current = 1.5mA
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0µA
		0	1					Low current = 50µA
		1	0					Low current = 100µA
		1	1					Low current = 150µA
	0							Select low current
	1							Select high current
								Tuner stand-by
0				0	0	0	0	Tuner StandBy OFF
1				0	0	0	1	Tuner StandBy ON

Table 35. Subaddress 1: PLL lock detector, FM mode and test

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Charge pump
							0	VCO adjust lock Disable
							1	VCO adjust lock Enable
						0		fref BYPASS Disable
						1		fref BYPASS Enable
								Tuner / PLL AM/FM mode
					0			Select AM mode
					1			Select FM mode
								Lock detector control
			0	0				PD phase difference threshold 10ns
			0	1				PD phase difference threshold 20ns
			1	0				PD phase difference threshold 30ns
			1	1				PD phase difference threshold 40ns
	0	0						Not valid
	0	1						Activation delay $4x1/f_{REF}$
	1	0						Activation delay $6x1/f_{REF}$
	1	1						Activation delay $8x1/f_{REF}$
0								Lock detector doesn't control charge pump
1								Lock detector controls charge pump

Table 36. Subaddress 2: PLL counter 1 (LSB)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Table 37. Subaddress 3: PLL counter 2 (MSB)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536

Note: 1 Swallow mode:f_{VCO}/f_{SYN} = LSB + MSB + 32

Table 38. Subaddress 4: reference counter 1 (LSB)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Table 39. Subaddress 5: Reference counter 2 (MSB)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536

Note: 1 f_{VCO}/f_{SYN} = LSB + MSB + 1

Table 40. Subaddress 6: FM antenna adjustment and FM mute depth

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM antenna adj (proportional to Vtuning)
			0	1	1	1	1	-30%
			0	1	1	1	0	-28%
			0	0	0	0	1	-2%
			0	0	0	0	0	-0%
			1	0	0	0	0	+0%
			1	0	0	0	1	+2%
-	-	-	-	-	-	-	-	-
			1	1	1	1	0	+28%
			1	1	1	1	1	+30%
								FM soft mute depth
	0	0						25dB
	1	0						20dB
	0	1						16dB
	1	1						13.5dB
								ISS deviation detector disabling threshold relative to weak fild ISS activation threshold (byte 31 bit 3-00
0								-100mV
1								+100mV

Table 41. Subaddress 7: FM RF adjustment AM prescaler and seek

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM RF adj (proportional to Vtuning)
			0	1	1	1	1	-30%
			0	1	1	1	0	-28%
-	-	-	-	-	-	-	-	-
			0	0	0	0	1	-2%
			0	0	0	0	0	-0%
			1	0	0	0	0	+0%
			1	0	0	0	1	+2%
-	-	-	-	-	-	-	-	-
			1	1	1	1	0	+28%
			1	1	1	1	1	+30%
								AM VCO divider ratio
	0	0						10
	0	1						8
	1	0						6
	1	1						4
								Seek mode
0								Seek OFF
1								Seek ON

Table 42. Subaddress 8: IF counter control 1 and AM S.S. threshold

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								IF counter control
					0	0	0	Not valid
					0	0	1	Not valid
					0	1	0	Not valid
					0	1	1	Δf = 6.25kHz (FM) 1kHz (AM UPC)
					1	0	0	Δf = 12.5kHz (FM) 2kHz (AM UPC)
					1	0	1	Δf = 25kHz (FM) 4kHz (AM UPC)
					1	1	0	Δf = 50kHz (FM) 8kHz (AM UPC)
					1	1	1	Δf = 100kHz (FM) 16kHz (AM UPC)
				0				IF counter disable/stand by

Table 42. Subaddress 8: IF counter control 1 and AM S.S. threshold (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1				IF counter enable
								AM stop station threshold
0	0	0	0					0mV
0	0	0	1					150mV
-	-	-	-	-	-	-	-	-
1	1	1	0					2100mV
1	1	1	1					2250mV

Table 43. Subaddress 9: If counter control 2

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM antenna adj (proportional to Vtuning)
			0	0	0	0	0	f_{center} = 10.60625MHz (FM) 449KHz (AM)
			0	0	0	0	1	f_{center} = 10.61250MHz (FM) 450KHz (AM)
			0	1	0	1	0	f_{center} = 10.66875MHz (FM) 459KHz (AM)
			0	1	0	1	1	f_{center} = 10.67500MHz (FM) 460KHz (AM)
			0	1	1	0	0	f_{center} = 10.68125MHz (FM) 461KHz (AM)
			0	1	1	0	1	f_{center} = 10.68750MHz (FM) 462KHz (AM)
			0	1	1	1	0	f_{center} = 10.69375MHz (FM) 463KHz (AM)
			0	1	1	1	1	f_{center} = 10.70000MHz (FM) 464KHz (AM)
			1	0	0	0	0	f_{center} = 10.70625MHz (FM) 465KHz (AM)
			1	0	0	0	1	f_{center} = 10.71250MHz (FM) 466KHz (AM)
			1	1	1	1	1	f_{center} = 10.80000MHz (FM) 480KHz (AM)
0	0	0						t_{sample} = 20.48ms (FM) 128ms (AM)
0	0	1						t_{sample} = 10.24ms (FM) 64ms (AM)
0	1	0						t_{sample} = 5.12ms (FM) 32ms (AM)
0	1	1						t_{sample} = 2.568ms (FM) 16ms (AM)
1	0	0						t_{sample} = 1.28ms (FM) 8ms (AM)
1	0	1						t_{sample} = 640µs (FM) 4ms (AM)
1	1	0						t_{sample} = 320µs (FM) 2ms (AM)
1	1	1						t_{sample} = 160µs (FM) 1ms (AM)

Table 44. Subaddress 10: IF counter reference (LSB)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Table 45. Subaddress 11: IF counter reference (MSB) and IF counter mode select

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
		0	0	0	0	0	0	MSB = 0
		0	0	0	0	0	1	MSB = 256
		0	0	0	0	1	0	MSB = 512
		1	1	1	1	0	1	MSB = 15616
		1	1	1	1	1	0	MSB = 15872
		1	1	1	1	1	1	MSB = 16128
								IF counter mode
0	0							not valid
0	1							IF counter FM mode (10.7KHz)
1	0							IF counter AM mode (450KHz)
0	0							not valid

Note: 1 f_{OSC}/f_{TIM} = LSB + MSB + 1

Table 46. Subaddress 12: AM IF amplifier gain

Ultra narrow band AGC threshold, FM Smeter and AC test

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								test FM FS soft mute enable (FM mode) [bit shared with AM IF AMP Gain]
							0	FS Soft mute disabled
							1	FS Soft mute enabled
								test AC mute (FM mode) [bit shared with AM IF AMP Gain]
						0		test mode FM demod Vout is disconnected from users
						1		no test (std)
								AM IF AMP Gain (am mode)
					0	0	0	Not used
					0	0	1	53.2dB
					0	1	0	55.8dB
					0	1	1	60.2dB
					1	0	0	58.3dB
					1	0	1	61.7dB
					1	1	0	62.8dB
					1	1	1	64.8dB
								AM UNAGC enable
				1				Enable AM UNAGC
				0				Disable AM UNAGC
								AM Ultra Narrow Band AGC Threshold
0	0	0	0					74.4dBmV @SG
0	0	0	1					78.8dBmV @SG
0	0	1	0					80.0dBmV @SG
0	0	1	1					80.7dBmV @SG 119.5dBmV @ IF2AMPOUT
0	1	0	0					53.2dBmV @SG
0	1	0	1					77.1dBmV @SG
0	1	1	0					78.5dBmV @SG
0	1	1	1					79.4dBmV @SG
1	0	0	0					42.7dBmV @SG
1	0	0	1					65.8dBmV @SG

Table 46. Subaddress 12: AM IF amplifier gain (continued)

Ultra narrow band AGC threshold, FM Smeter and AC test (continued)

MSB							LSB	Function
1	0	1	0					77.6dBmV @SG
1	0	1	1					78.5dBmV @SG
1	1	0	0					32.6dBmV @SG 113.5dBmV @ IF2AMPOUT
1	1	0	1					55.0dBmV @SG
1	1	1	0					73.3dBmV @SG
1	1	1	1					77.6dBmV @SG

Table 47. Subaddress 13: Demodulator fine adjust and noise blanker, MP qual test

MSB							LSB	Function	
D7	D6	D5	D4	D3	D2	D1	D0		
								Fm audio demodulator current adjust	
			0	0	0	0	0	0µA	
			0	0	0	0	1	0.167µA	
			-	-	-	-	-	-	
			0	1	1	1	1	2.51µA	
			1	0	0	0	0	0µA	
			0	0	0	0	1	0.167µA	
			1	-	-	-	-	-	
			1	1	1	1	1	2.51µA	
								Demodulator Noise Blanker	**AM Smeter extension**
	0	0						NB1&2 on (impvic&lontmas)	old (10.7MHz)
	0	1						NB1 on (impvicmas)	old (10.7MHz)
	1	0						NB2 on (implontmas0	new (450kHz)
	1	1						NB1&2 off	new (450kHz)
								Multipath (ISS) test	
								MP test OFF	
								MP test ON (ISS quality detector MP input from #ACinL, ISS MP filter+rect output to Smeter test muxer if input 12 is selected	

Table 48. Subaddress 14: Quality detection adjacent channel

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS Filter for WB
							0	ISS filter 30KHz OFF
							1	ISS filter 30KHz ON
								ISS Adjacent Channel filter configuration
						0		AC highpass frequency 100KHz
						1		AC bandpass frequency 100KHz
								AC gain
					0			32dB
					1			38dB
								ISS Adjacent Channel threshold
		0	0	0				AC wide band threshold 0.25V
		0	0	1				AC wide band threshold 0.35V
		0	1	0				AC wide band threshold 0.45V
		1	1	1				AC wide band threshold 0.95V
0	0							AC narrow band threshold 0V
0	1							AC narrow band threshold 0.1V
1	0							AC narrow band threshold 0.2V
1	1							AC narrow band threshold 0.3V

Table 49. Subaddress 15: Quality detection multipath and Smeter test

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS Multipath control enabling
							0	Multipath control ON
							1	Multipath control OFF
								ISS Multipath filter center frequncy
						0		MP Bandpass frequency 19KHz
						1		MP Bandpass frequency 31KHz
								ISS Multipath filter input selector (test mode)
					0			Smeter unfilt test OFF
					1			Smeter unfilt test ON
								ISS Multipath threshold

Table 49. Subaddress 15: Quality detection multipath and Smeter test (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			0	0				0.5V
			0	1				0.75V
			1	0				1V
			1	1				1.25V
								ISS mode
	0	0						Application mode 1
	0	1						Application mode 2
								ISS Multipath control mode
0								MP control AC+ detection
1								MP control the AC and AC+ detection

Table 50. Subaddress 16: Quality detection deviation

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS deviation detector ime constant
					0	0	0	charge current 34µA; discharge current 6µA
					0	0	1	charge current 32µA; discharge current 8µA
					0	1	0	charge current 30µA; discharge curren10µA
					1	0	0	charge current 26µA; discharge current 14µA
					1	1	1	charge current 20µA; discharge current 20µA
								ISS deviation detector thresholds
			0	0				DEV Threshold for ISS **narrow-wide** 30KHz
			0	1				DEV Threshold for ISS **narrow-wide** 45KHz
			1	0				DEV Threshold for ISS **narrow-wide** 60KHz
			1	1				DEV Threshold for ISS **narrow-wide** 75KHz
	0	0						DEV Threshold for ISS filter **OFF** ratio 1
	0	1						DEV Threshold for ISS filter **OFF** ratio 1.3

Table 50. Subaddress 16: Quality detection deviation (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	1	0						DEV Threshold for ISS filter **OFF** ratio 1.4
	1	1						DEV Threshold for ISS filter **OFF** ratio 1.5
0								not used
1								AUX set int80

Table 51. Subaddress 17: Quality ISS filter

MSB							LSB	Function	Function	Function	Function
D7	D6	D5	D4	D3	D2	D1	D0				
								ISS automatic control fron AC detector			
							0	ON (AC drives ISSTC)			
							1	OFF (AC has no influence on ISSTC)			
								ISS manual control			
						0		automatic control only			
						1		manual force filter ON			
					0			manual force BW 120KHz			
					1			manual force BW 80KHz			
								ISS time constant			
								current:	discharge	chrg mid	chrg narrow
		0	0	0					1µA	74µA	124µA
		0	0	1					3µA	72µA	122µA
		0	1	0					5µA	70µA	120µA
		1	0	0					9µA	66µA	116µA
		1	1	1					15µA	60µA	110µA
								ISS filter center frequency			
0	0							shift from 450kHz		-20KHz	
0	1									-10KHz	
1	0									0KHz	
1	1									10KHz	

Table 52. Subaddress 18: PLL rest, 456KHz VCO adjust start, ISS MP Gain and SD out mode

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								PLL test mode
					0	0	0	
					0	0	1	
					0	1	0	
					0	1	1	
					1	0	0	
					1	0	1	
					1	1	0	
					1	1	1	
								Automatic 456KHz VCO adjustment
				0				Waiting
				1				START
								ISS multipath filter gain
		0	0					ISS MP Gain 2dB
		0	1					ISS MP Gain 13dB
		1	0					ISS MP Gain 16dB
								SD pin configuration
0	0							ISS (IFC and FM SM Stop)
0	1							IF Counter out
1	0							FM Smeter Stop
1	1							Logic 1

Table 53. Subaddress 19: 456KHz VCO adjustment (manual mode)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							0	Enable IFC (I2CBUS) OFF
							1	Enable IFC (I2CBUS) ON
						0		Enable 456KHz VCO adj procedure (I2CBUS) OFF
						1		Enable 456KHz VCO adj procedure (I2CBUS) ON
	0	0	0	0	0			VCO 456KHz frequency adjust (I2CBUS) minfreq

Table 53. Subaddress 19: 456KHz VCO adjustment (manual mode) (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0	0	1			
	-	-	-	-	-			
	0	1	1	1	1			
	1	0	0	0	0			
	-	-	-	-	-			
	1	1	1	1	0			
	1	1	1	1	1			VCO 456KHz frequency adjust (I2CBUS) maxfreq
0								Manual adjustment procedure (I2CBUS)
1								Automatic adjustment procedure (State Machine)

Table 54. Subaddress 20: FM stop station and soft mute threshold

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Soft mute threshold on Smeter
				0	0	0	0	0mV
				0	0	0	1	100mV
				-	-	-	-	-
				1	1	1	0	1.4V
				1	1	1	1	1.5V
								FM stop station threshold on Smeter
0	0	0	0					400mV
0	0	0	1					800mV
-	-	-	-					-
1	1	1	0					3.2V
1	1	1	1					3.6V

Table 55. Subaddress 21: Adjacent channel mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Adj channel mute gain
					0	0	0	10.4dB
					0	0	1	11.4dB

Table 55. Subaddress 21: Adjacent channel mute (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
					0	1	0	12.4dB
					0	1	1	13.4dB
					1	0	0	14.4dB
					1	0	1	15.4dB
					1	1	0	16.4dB
					1	1	1	17.4dB
								Adj channel mute clamp
	0	0	0	0				500mV
	0	0	0	1				600mV
	-	-	-	-				-
	1	0	0	0				1.3V
	-	-	-	-				-
	1	1	1	0				1.9V
	1	1	1	1				2V
								Adjacent Channel (ISS) test
0								AC test OFF
1								AC test ON (ISS qualitydetector AC input from #ACinL, ISS AC filter+rect output to Smeter test muxer if input 12 is selected)

Table 56. Subaddress 22: FM Smeter Sider and AM Smeter time constant

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM Smeter sider
			0	0	0	0	0	0V
			0	0	0	0	1	0.48V
			-	-	-	-	-	-
			1	1	1	1	0	1.45V
			1	1	1	1	1	1.5V
								AM Smeter filter TC (resistor value)
0	0	0						75KΩ
1	0	0						50KΩ
0	1	0						35KΩ

Table 56. Subaddress 22: FM Smeter Sider and AM Smeter time constant

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0						24KΩ
0	0	1						16KΩ

Table 57. Subaddress 23: IFT Adjust

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								IFT1 Adjust
				0	0	0	0	0pF
				0	0	0	1	0.55pF
				-	-	-	-	-
				0	1	1	1	7.7pF
				1	1	1	1	8.25pF
								IFT2 Adjust
0	0	0	0					75pF
1	0	0	0					50pF
-	-	-	-					-
0	1	1	1					22.4pF
1	1	1	1					24pF

Table 58. Subaddress 24: XTAL and FM IF AMP 2 Gain

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								XTAL adjust Cload
			0	0	0	0	0	0pF
			0	0	0	0	1	0.625pF
			0	0	0	1	0	1.25pF
			0	0	1	0	0	2.5pF
			0	1	0	0	0	5pF
			0	0	1	0	0	10pF
			0	1	0	0	0	10.4pF
								XTAL TEST)
		0						xtal clock
		1						clocksep (testing)

Table 58. Subaddress 24: XTAL and FM IF AMP 2 Gain (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM IF Amp2 Gain
0	0							6dB
0	1							8dB
1	0							10dB
1	1							not used

Table 59. Subaddress 25: FM NAGC key and AM WAGC

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								FM Narrow ACGC key IF input
					0	0	0	36dB
					0	0	1	42dB
					0	1	0	48dB
					0	1	1	54dB
					1	0	0	60dB
					1	0	1	66dB
					1	1	0	72dB
					1	1	1	keying OFF
								AM WAGC starting point @ MIX1IN
0	0	0	0	0				88dBµV
-	-	-	-	-				-
1	1	1	1	1				106dBµV

Table 60. Subaddress 26: AM NAGC key and FM demod ref frequency test

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
					1	1	0	test for FM demod ref freq divider (standard configuration)
								AM WAGC starting point @ MIX2IN
0	0	0	0	0				85dBµV
-	-	-	-	-				-
1	1	1	1	1				103dBµV

Table 61. Subaddress 27: ISS tests

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS test multiplexer (1)
0	0	0	0	0	0	0	0	no test
0	0	0	0	0	0	0	1	test MP thresholds
0	0	0	0	0	0	1	0	test ACN thresholds
0	0	0	0	0	1	0	0	test DW thresholds
0	0	0	0	1	0	0	0	test D thresholds
0	0	0	1	0	0	0	0	test ACW thresholds
0	0	1	0	0	0	0	0	test ac
0	1	0	0	0	0	0	0	test MDSCO
1	0	0	0	0	0	0	0	test ISSout

Table 62. Subaddress 28: ISS tests

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS test multiplexer (2)
		0	0	0	0	0	0	no test
		0	0	0	0	0	1	test dev+
		0	0	0	0	1	0	test dev+
		0	0	0	1	0	0	test ref dev
		0	0	1	0	0	0	test dem Vout
		0	1	0	0	0	0	test ISS in
		1	0	0	0	0	0	test ISSC ik Enble
								ISS test in
	0							test in ISS disable
	1							test in ISS enable
								ISS test clock
0								test ISS clock disable
1								test ISS clock enable

Table 63. Subaddress 29: Tuner and Smeter tests

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								SMETER test multiplexer
		0	0	0	0	0	0	test off
		0	0	0	0	0	1	test AMAGC1W
		0	0	0	0	1	0	test AMAGC1N
		0	0	0	0	1	1	test AMAGC1UN
		0	0	0	1	0	0	test FM Smute Threshold
		0	1	0	1	0	1	test FMSMStop
		0	0	0	1	1	0	test AMIF2Amp
		0	0	0	1	1	1	test AMSDDAC
		0	0	1	0	0	0	test FMKAGC
		0	0	1	0	0	1	test FMACMDisable
		0	0	1	0	1	0	test FMDemodAdjON
		0	0	1	0	1	1	test FMDemodAdjONMute
		0	0	1	1	0	0	test FMACMuteRct
		0	0	1	1	0	1	test FSISSONThreshold
		0	0	1	1	1	0	test FSISSON
		0	0	1	1	1	1	test ISSInput
	0							Smeter OUT ACD enable
	1							test Smete IN
0								Smeter filter force enable
1								test TMODE1OUT (byte 27/28)

Table 64. Subaddress 30: Adjacent channel mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Adjacent channel mute threshold
				0	0	0	0	0mV
				0	0	0	1	28.7mV
				-	-	-	-	-
				1	0	0	0	229.3mV
				-	-	-	-	-
				1	1	1	0	401.3mV
				1	1	1	1	430mV
								Adjacent channel mute filter configuration

Table 64. Subaddress 30: Adjacent channel mute (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			0					AdjChannel Mute HighPass filter 1
			1					AdjChannel Mute BandPass filter 1
-	-	0						AdjChannel Mute HighPass filter 2
		1						AdjChannel Mute BandPass filter 2
								Adjacent channel mute disable @ low FS
0	0							threshold 1V
0	1							threshold 1.33V
1	0							threshold 1.66V
1	1							threshold 2V

Table 65. Subaddress 31: Adjacent channel and multipath gain, weak field ISS threshold

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Weak field ISS activation threshold
				0	0	0	0	-450mV
				0	0	0	1	-385.7mV
				-	-	-	-	-
				0	1	1	1	-0mV
				1	0	0	0	+0mV
				1	0	0	1	64.28mV
				-	-	-	-	-
				1	1	1	0	385.7mV
				1	1	1	1	450mV
								Tuner quality multipath gain
		0	0					0 (OFF) dB
		0	1					-4dB
		1	0					0dB
		1	1					4dB
								Tuner quality adjacent channel gain
0	0							(OFF)
0	1							-4dB
1	0							0dB
1	1							4dB

4.3 Stereodecoder and audioprocessor section

Table 66. Address organisation

	MSB							LSB	Function
Subaddr.	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
0	spkr coupl	in gain				source selector			Source selector, in gain, peaker coupling
1	volume steps								Volume
2	not used	treble center freq		treble steps					Treble
3	bass DC mode	bass Q factor		bass steps					Bass
4	volume steps								Speaker attenuator Left Front
5	volume steps								Speaker attenuator Right Front
6	volume steps								Speaker attenuator Left Read
7	volume steps								Speaker attenuator Right Rear
8	NB time		bass center frequency		not used	soft mute time		I^2C soft mute off	Soft mute, soft mute time, Bass, Noise blanker time
9	deemph.	pilot thr.	NB peak dis	force mono	auto zero status	std in gain		std mute disable	Stereo decoder mute, st dec in-gain, mono, NB PEAK disch curr., pilot thresh, deemph.
10	overdev. adj		NB on	noise contr.thresh.		low threshold			Noise Blanker
11	mpath. infl.	VHCL		VHCH		max high out		high cut on	High cut, multipath influence
12	mpath. infl.	Quality del. coeff.		NB field strength gain		NB field strength threshold		not used	Fieldstrength control
13	mpath. det. Reflect. Gain		mpath. charge	mpath.int. infl	mpath.det gain		noise rect.disch, R		Noise rectifier disch. resistor, Multipath del. bandpass gain, multipath internal influence, reflection gain
14	roll-off compens.	level gain				roll-off compensation			Roll-off compensation, level gain
15	AP test ON	400K ON	test signal selection				Itest SC OFF	SID test ON	TEST BYTE

Table 66. Address organisation (continued)

	MSB							LSB	Function
Subaddr.	D7	D6	D5	D4	D3	D2	D1	D0	
16	AM high cut control corner frequency					quality noise gain		mpath test	AMHCC, Quality noise gain, test
17	mid Qfactor	mid center frequency		mid steps					Mid
18	not used					VSBL			Stereo blend

Table 67. Stereodecoder and audioprocessor section SUBADDRESS

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
testcon	azhold	autoincr	subaddress				

Table 68. Stereodecoder and audioprocessor section READ MODE

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
				STEREO	SMON		

Table 69. Stereodecoder and audioprocessor section ADDRESS

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
1	0	0	0	1	1	0	R/W

4.4 Subaddress organization (stereodecoder and audioprocessor section)

Table 70. SUBADDRESS 0: Source selector, in-gain, sSpeaker coupling

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Source selector
					0	0	0	Quasi-differential input 1
					0	0	1	Quasi-differential input 2
					0	1	0	not used (mute)
					0	1	1	Turner input (AM mode)
					1	0	0	Turner input (FM mode)
					1	0	1	not used (mute)

Table 70. SUBADDRESS 0: Source selector, in-gain, sSpeaker coupling

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
					1	1	0	not used (mute)
					1	1	1	not used (mute)
								In-Gain
	0	0	0	0				0dB
	0	0	0	1				1dB
	-	-	-	-				-
	1	1	1	0				14dB
	1	1	1	1				15dB
								Speaker coupling
0								AC (external)
1								DC (internal)

Table 71. Subaddress 1,4,5,6,7: Volume Spkr atten. LF, RF, LR, RR

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Volume steps
1	0	0	0	1	1	1	1	15dB
-	-	-	-	-	-	-	-	-
1	0	0	0	0	0	0	1	1dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	-1dB
-	-	-	-	-	-	-	-	-
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-15dB
-	-	-	-	-	-	-	-	-
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
X	1	1	X	X	X	X	X	mute

Note: No other combinations are allowed

Table 72. Subaddress 2: Treble

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble filter steps
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			-	-	-	-	-	-
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	1dB
			-	-	-	-	-	-
			1	0	0	0	1	-14dB
			1	0	0	0	0	-15dB
								Treble filter center frequency
	0	0						10.0kHz
	0	1						12.5kHz
	1	0						15kHz
	1	1						17.5kHz

Table 73. Subaddress 3: Bass

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Bass filter steps
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			-	-	-	-	-	-
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	1dB
			-	-	-	-	-	-
			1	0	0	0	1	-14dB
			1	0	0	0	0	-15dB
								Bass filter Q-factor
	0	0						1.00

Table 73. Subaddress 3: Bass (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	1						1.25
	1	0						1.50
	1	1						2 (makes cent. freq. = 150Hz when programmed to 100Hz)
								Bass filter DC mode
0								off
1								on

Table 74. Subaddress 4: Speaker attenuator left front

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Volume steps
1	0	0	0	1	1	1	1	15dB
-	-	-	-	-	-	-	-	-
1	0	0	0	0	0	0	1	1dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	-1dB
-	-	-	-	-	-	-	-	-
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-15dB
-	-	-	-	-	-	-	-	-
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
X	1	1	X	X	X	X	X	mute

Note: No other combinations are allowed

Table 75. Subaddress 8: Soft mute, bass, noise blanker time

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Soft mute activation control
							0	I^2C bus Audio Processor mute ON (independently of pin Audio Mute)

Table 75. Subaddress 8: Soft mute, bass, noise blanker time

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
							1	I²C bus Audio Processor mute OFF (pin Audio Mute controls muting: pin=0 □ ≥ mute ON, pin=1 ≥ mute OFF)
					0	0		Soft mute transition time = 0.48ms
					0	1		Soft mute transition time = 0.96ms
					1	0		Soft mute transition time = 20.2ms
					1	1		Soft mute transition time = 40.4ms
								Base filter center frequency
		0	0					60Hz
		0	1					70Hz
		1	0					80Hz
		1	1					100Hz (if bass DC mode OFF)
		1	1					150Hz (if bass DC mode ON)
								Noise Blanker time
0	0							38µs
0	1							25.5µs
1	0							32µs
1	1							22µs

Table 76. Subaddress 9: Stereo decoder mute

Stereo decoder in-gain, mono, NB PEAK disch, Curr., pilot thresh, deemph

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Stereo Decoder Mute
							0	high-ohmic mute, pilot hold, multipath time constant short ENABLED (mute set by pin RDS mute LOW)
							1	high-ohmic mute, pilot hold, multipath time constant short DISABLED (regardless of pin RDS mute)
								Stereo Decoder In-gain
					1	1		0dB
					1	0		2.5dB
					0	1		4dB
					0	0		5.5dB

Table 76. Subaddress 9: Stereo decoder mute

Stereo decoder in-gain, mono, NB PEAK disch, Curr., pilot thresh, deemph

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Auto Zero Status
				0				disabled
				1				enabled; trans. 0 ≥ 1 performs Autozero sequence
								Force MONO
			0					ON
			1					OFF (automatic MONO/STEREO switch)
								Noise PEAK discharge current
		0						low
		1						High
								Pilot Threshold
	0							low
	1							High
								Demphasis
0								50µs
1								75µs

Table 77. Subaddress 10: Noise blanker

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Low threshold
					0	0	0	65mV
					0	0	1	60mV
					-	-	-	-
					1	1	1	30mV
								Noise controlled threshold
			0	0				320mV
			0	1				260mV
			1	0				200mV
			1	1				140mV
								Noise Blanker operation

Table 77. Subaddress 10: Noise blanker (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
		0						OFF
		1						ON
								Overdeviation adjustment
0	0							2.8V
0	1							2.0V
1	0							1.2V
1	1							OFF

Table 78. Subaddress 11: High cut, multipath influence

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								High cut operation
							0	OFF
							1	ON
								Max high cut
					0	0		2dB
					0	1		5db
					1	0		7dB
					1	1		10dB
								VHCH
			0	0				42% REF 5V
			0	1				50% REF 5V
			1	0				58% REF 5V
			1	1				66% REF 5V
								VHCL
	0	0						16.7% VHCH
	0	1						22.2% VHCH
	1	0						27.8% VHCH
	1	1						33.3% VHCH
								Strong Multipath influence on PEAK 18K
0								OFF
1								ON (18K discharge if V_{MPOUT} <2.5V)

Table 79. Subaddress 12: Fieldstrength control

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Noise blanker fieldstrength threshold
						0	0	min
						1	0	
						0	1	
						1	1	max
								Noise blanker fieldstrength gain
				0	0			2.3V
				1	0			1.8V
				0	1			1.3V
				1	1			OFF
								Quality detector coefficient a
0	0							a = 0.7
0	1							a = 0.85
1	0							a = 1.0
1	1							a = 1.15
								Multipath influence on PEAK discharge
0								OFF
1								ON

Table 80. Subaddress 13: Noise rectifier discharge resistor

Bandpass gain, internal influence, change current, reflection gain detectors.

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Noise rectifier discharge resistor
						0	0	R = infinite
						0	1	R = 56K
						1	0	R = 33K
						1	1	R = 18K
								Multipath detector bandpass gain
				0	0			6dB
				0	1			12dB

Table 80. Subaddress 13: Noise rectifier discharge resistor (continued)

Bandpass gain, internal influence, change current, reflection gain detectors. (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1	0			16dB
				1	1			18dB
								Multipath detector internal influence
			0					ON
			1					OFF
								Multipath detector change current
		0						0.5µA
		1						1µA
								Multipath detector reflection gain
0	0							Gain = 7.6dB
0	1							Gain = 4.6dB
1	0							Gain = 0dB
1	1							disabled

Table 81. Subaddress 14: Roll-off compensation, level gain

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Roll-off compensation
0					0	0	0	not allowed
0					0	0	1	7.2%
0					0	1	0	9.4%
-					-	-	-	
0					1	0	0	13.7%
-					-	-	-	
0					1	1	1	20.2%
1					0	0	0	not allowed
1					0	0	1	19.6%
1					0	1	0	21.5%
-					-	-	-	
1					1	0	0	25.3%
-					-	-	-	
1					1	1	1	31.0%

Table 81. Subaddress 14: Roll-off compensation, level gain (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Level gain
	0	0	0	0				0dB
	0	0	0	1				0.66dB
	0	0	1	0				1.33dB
	-	-	-	-				-
	1	1	1	1				10dB

Table 82. Subaddress 15: Test byte

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Stereo decoder test signals enabling
							0	test signal disabled
							1	test signal enabled (if S6=1) on ACinR
								Stereo decoder test signals selection
			0	0	0	0		VHCCH
			0	0	0	1		LEVELINTERN
			0	0	1	0		PILOT
			0	0	1	1		VCOCON (VCO tuning voltage)
			0	1	0	0		PIL_VTH
			0	1	0	1		HOLDN
			0	1	1	0		NB_VTH
			0	1	1	1		F228
			1	0	0	0		VHCCL
			1	0	0	1		VSBL
			1	0	1	0		state machine enable ifc
			1	0	1	1		state machine set456
			1	1	0	0		PEAK
			1	1	0	1		state machine check
			1	1	1	0		REF 5V
			1	1	1	1		SBPWM
								Test SC filter
						0		Fast test enabled (2-phase 200KHz clock)

Table 82. Subaddress 15: Test byte (continued)

MSB							LSB	Function
						1		Test disabled (4-phase 200KHz clock)
								400 KHz VCO OFF
	0							OFF
	1							ON
								Audio processor test enabling
0								Test disabled
1								Test enabled (if S6=1)

Table 83. Subaddress 16: Multipath test, AMHCC

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Multipath test enable
							0	Multipath Detector test input disabled
							1	Multipath Detector test input enabled
								Quality detector noise gain
					0	0		15dB
					0	1		12dB
					1	0		9dB
					1	1		6dB
								AM High-cut control corner frequency
0	0	0	0	0				
0	0	0	0	1				
-	-	-	-	-				
1	1	1	1	0				
1	1	1	1	1				

Table 84. Subaddress 17: Mid

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Mid filter steps
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			-	-	-	-	-	-
			0	1	1	1	0	-1db

Table 84. Subaddress 17: Mid (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	1dB
-			-	-	-	-	-	-
			1	0	0	0	1	14dB
			1	0	0	0	0	15dB
								Mid filter center frequency
	0	0						500Hz
	0	1						1.0KHz
	1	0						1.5KHz
	1	1						2.0KHz
								Mid filter Q factor
0								1.0
1								2.0

Table 85. Subaddress 18: Stereo blend

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								VSBL
					0	0	0	VSBL at 29% REF 5V
					0	0	1	VSBL at 33% REF 5V
					0	1	0	VSBL at 38% REF 5V
					0	1	1	VSBL at 42% REF 5V
					1	0	0	VSBL at 46% REF 5V
					1	0	1	VSBL at 29% REF 5V
					1	1	0	VSBL at 50% REF 5V
-					1	1	0	VSBL at 54% REF 5V
					1	1	1	VSBL at 58% REF 5V

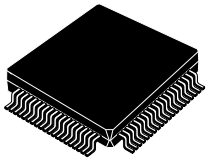
5 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

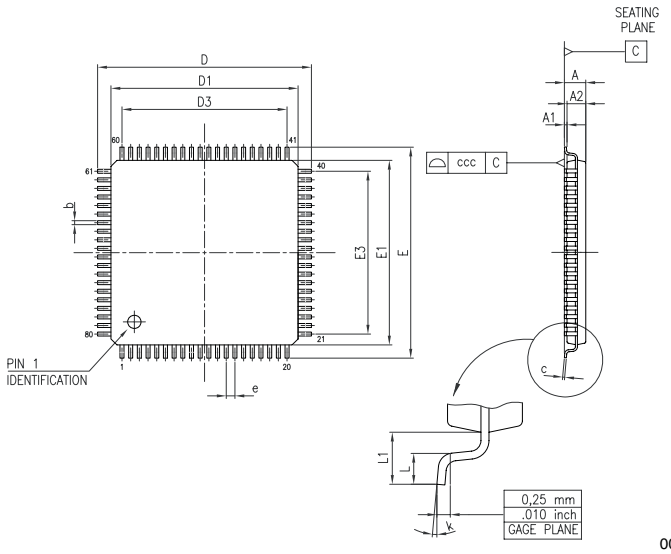
Figure 21. LQFP80 mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.220	0.320	0.380	0.0087	0.0126	0.0150
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3		12.350			0.4862	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3		12.350			0.4862	
e		0.650			0.0256	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0° (min.); 3.5° (typ,); 7° (max.)					
ccc			0.100			0.0039

OUTLINE AND MECHANICAL DATA



LQFP80 (14x14x1.40mm)
Low profile **Q**uad **F**lat **P**ackage



6 Revision history

Table 86. Document revision history

Date	Revision	Changes
01-Jun-2004	1	Initial release.
18-Apr-2007	2	Package changed, text and layour modifications.

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