

**CMOS/MOS
INTEGRATED
CIRCUITS**



41C 08817 D T-51-11

PRELIMINARY DATA

ANALOG MULTIPLEXERS-DEMULPLEXERS:

4051B - SINGLE 8-CHANNEL
4052B - DIFFERENTIAL 4-CHANNEL
4053B - TRIPLE 2-CHANNEL

- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- LOW "ON" RESISTANCE: 125Ω (TYP.) OVER 15V p.p. SIGNAL-INPUT RANGE for $V_{DD}-V_{EE}=15V$
- HIGH "OFF" RESISTANCE: CHANNEL LEAKAGE ± 100 pA (TYP.) $V_{DD}-V_{EE}=18V$
- BINARY ADDRESS DECODING ON CHIP
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT and SUPPLY CONDITIONS: 0.2 μW (TYP.), $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- MATCHED SWITCH CHARACTERISTICS: $R_{ON}=5\Omega$ (TYP.) for $V_{DD}-V_{EE}=15V$
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS: DIGITAL 3 TO 20V, ANALOG TO 20V p.p.
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 mA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The HCC 4051B, 4052B and 4053B (extended temperature range) and HCF 4051B, 4052B and 4053B (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage. HCC/HCF 4051B, HCC/HCF 4052B, and HCC/HCF 4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. These multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channel are off. The HCC/HCF 4051B is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output. The HCC/HCF 4052B is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs. The HCC/HCF 4053B is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20 -0.5 to 18	V V
V_i	Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_i	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor		
	for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

ORDERING NUMBERS:

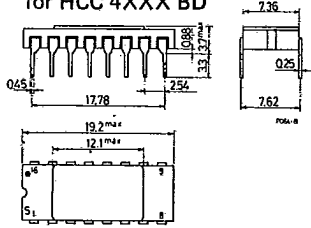
HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BE for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal
HCF 4XXX BM for plastic micropackage



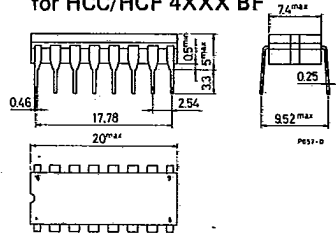
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MECHANICAL DATA (dimensions in mm)

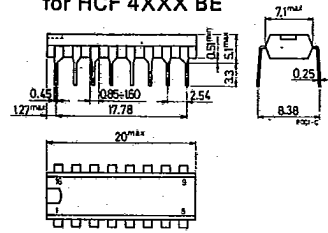
Dual in-line ceramic package for HCC 4XXX BD



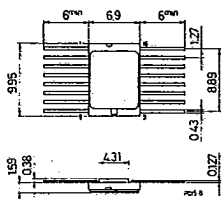
Dual in-line ceramic package for HCC/HCF 4XXX BF



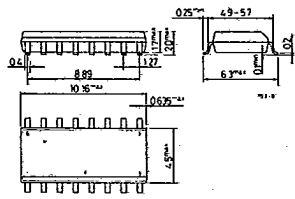
Dual in-line plastic package for HCF 4XXX BE



Ceramic flat package for HCC 4XXX BK

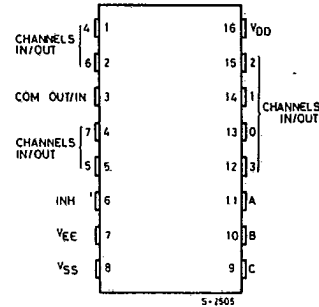


Plastic micropackage for HCF 4XXX BM

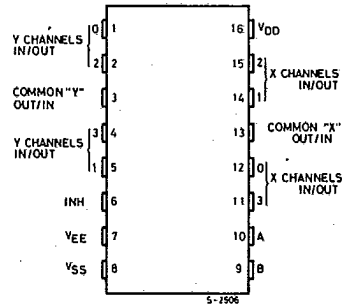


CONNECTION DIAGRAMS

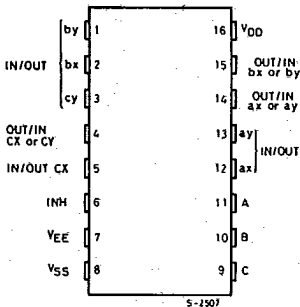
for 4051B



for 4052B



for 4053B



RECOMMENDED OPERATING CONDITIONS

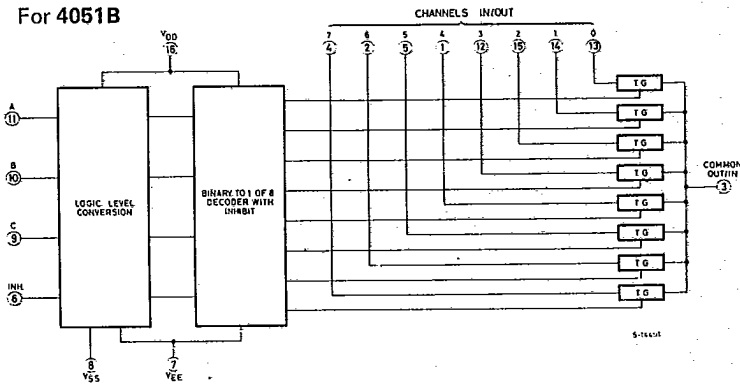
V_{DD}	Supply voltage: HCC types HCF types	3 to 18 V 3 to 15 V
V_I	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 °C -40 to 85 °C



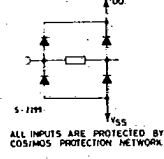
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FUNCTIONAL DIAGRAMS AND TRUTH TABLES

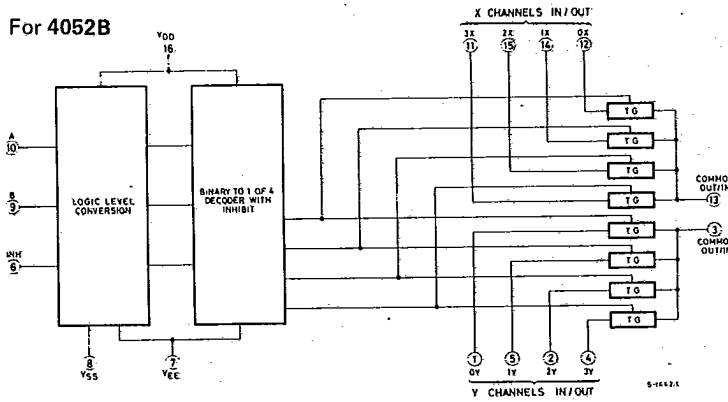
For 4051B



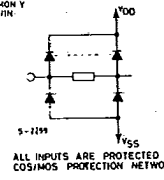
INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	NONE



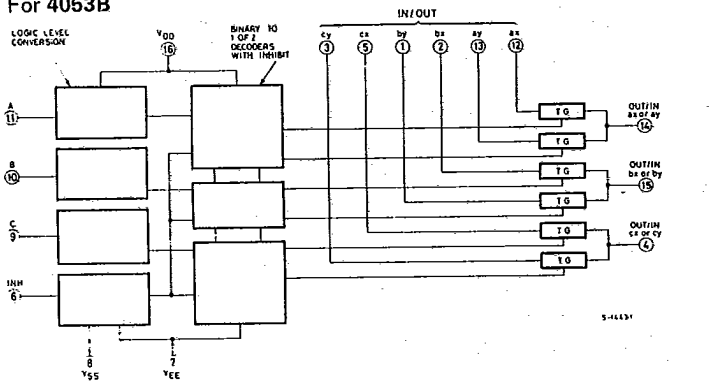
For 4052B



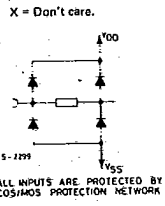
INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE



For 4053B



INHIBIT	A or B or C	
0	0	ax or bx or cx
0	1	ay or by or cy
1	X	NONE





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STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values						Unit		
			V _{IS} (V)	V _{EE} (V)	V _{SS} (V)	V _{DD} (V)	T _{Low} (*)		25°C			T _{High} (*)			
							Min.	Max.	Min.	Typ.	Max.	Min.		Max.	
I _L	Quiescent device current	HCC types				5	5	0.04	5	150	μA				
						10	10	0.04	10	300					
						15	20	0.04	20	600					
						20	100	0.08	100	3000					
		HCF types				5	20	0.04	20	150					
						10	40	0.04	40	300					
SWITCH															
ON	Resistance	HCC types	0 < V _I < V _{DD}	0	0	5	880	470	1050	1200	Ω				
						10	310	180	400	580					
						15	220	125	280	400					
		HCF types				5	880	470	1050	1200					
						10	330	180	400	520					
						15	230	125	280	360					
ΔON	Resistance ΔR _{ON} (Between any 2 channels)			0	0	5		10			Ω				
						10		10							
						15		5							
OFF(*)	Channel Leakage Current	Any channel OFF		0	0	18	100	±0.1	100	1000	nA				
		All channels OFF (common OUT/IN)										HCC types			
		Any channel OFF											HCF types		
		All channels OFF (common OUT/IN)										0		0	15
C	Capacitance	Input									pF				
		Output 4051										-5	-5	5	30
		Output 4052													18
		Output 4053													9
Feedthrough	0.2														
CONTROL (Address or Inhibit)															
V _{IL}	Input low voltage		=V _{DD} thru 1KΩ	V _{EE} =V _{SS} R _I =1KΩ to V _{SS}	I _{IS} < 2 μA (on all OFF channels)	5	1.5		1.5	1.5	V				
						10	3		3	3					
						15	4		4	4					
V _{IH}	Input high voltage					5	3.5	3.5		3.5	V				
						10	7	7		7					
						15	11	11		11					
I _{IH} , I _{IL}	Input leakage current	HCC types	V _I = 0/18V			18	±0.1	±10 ⁻³	±0.1	±1	μA				
		HCF types										V _I = 0/15V	15	±0.3	±10 ⁻³
C _I	Input capacitance		Any address or inhibit input				5	7.5			pF				

(*) Determined by minimum feasible leakage measurement for automatic testing.
 (*) T_{Low} = - 55°C for HCC device; -40°C for HCF device.
 T_{High} = +125°C for HCC device; +85°C for HCF device.



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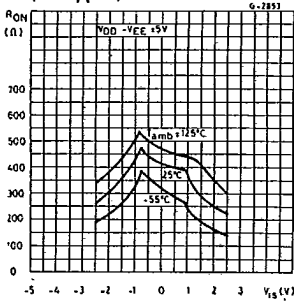
DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}C$, $C_L = 50$ pF all input square wave rise and fall time = 20 ns)

Parameter	Test conditions						Values		Unit				
	V_{EE} (V)	R_L (k Ω)	f_i (KHz)	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)	Typ.	Max.					
SWITCH													
t_{pd} Propagation delay time (Signal Input to output)		200				5	30	30	ns				
						10	15	60					
						15	11	20					
Frequency Response Channel "ON" (Sine Wave Input) at $20 \text{ Log } \frac{V_o}{V_i} = -3\text{dB}$	$=V_{SS}$	1		5(*)		10	V_o at Common OUT/IN	4053B	30	MHz			
								4052B	25				
								4051B	20				
							V_o at Any Channel	60					
Feedthrough (All channels OFF) at $20 \text{ Log } \frac{V_o}{V_i} = -40 \text{ dB}$	$=V_{SS}$	1		5(*)		10	V_o at Common OUT/IN	4053	8	MHz			
								4052	10				
								4051	12				
							V_o at Any channel	8					
Frequency Signal Crosstalk at $20 \text{ Log } \frac{V_o}{V_i} = -40 \text{ dB}$	$=V_{SS}$	1		5(*)		10	Between Any 2 channels		3	MHz			
							Between sections 4052B only	Measured on common	6				
								Measured on Any channel	10				
							Between Any 2 sections 4053B only	In Pin 2 Out Pin 14	2.5				
In Pin 15 Out Pin 14	6												
Sine wave Distortion $f_{IS} = 1$ KHz sine wave	$=V_{SS}$	10	1	2(*)		5			0.3	%			
									0.2				
									0.12				
CONTROL (Address or Inhibit)													
Propagation delay time: Address - to Signal OUT Channels ON or OFF	0								360	720	ns		
	0								0	10		160	320
	0								0	15		120	240
	-5								0	5		225	450
Propagation delay time: Inhibit to signal OUT (channel turning ON)	0	10							360	720	ns		
	0								0	5		160	320
	0								0	15		120	240
	-10								0	5		200	400
Propagation delay time: Inhibit to signal OFF (channel turning OFF)	0	0.3							200	450	ns		
	0									10		90	210
	0									15		70	160
	-10									5		130	300
Address or Inhibit to Signal Crosstalk	0	10*			0	10	$V_C = V_{DD} - V_{SS}$ (Square Wave)	65		mV peak			

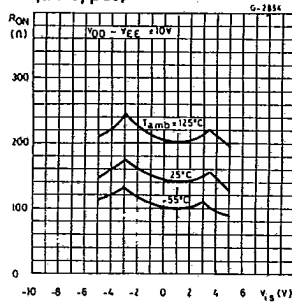
(*) Peak to peak voltage symmetrical about $\frac{V_{DD} - V_{EE}}{2}$
 (*) Both ends of channel.



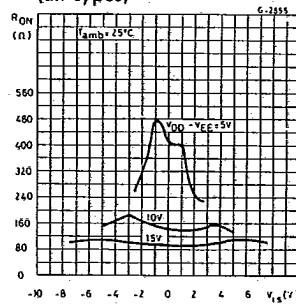
Typical channel ON resistance vs. input signal voltage (all types)



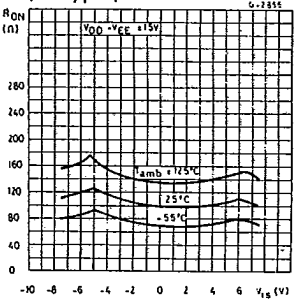
Typical channel ON resistance vs. input signal voltage (all types)



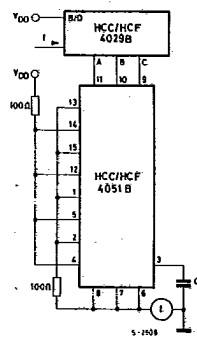
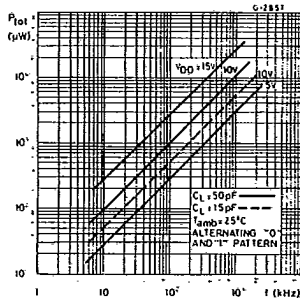
Typical channel ON resistance vs. input signal voltage (all types)



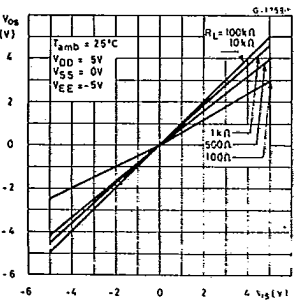
Typical channel ON resistance vs. input signal voltage (all types)



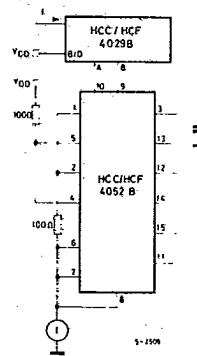
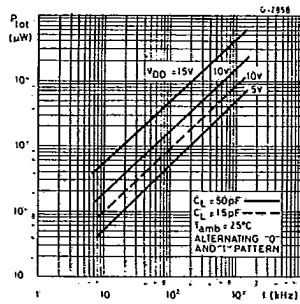
Typical dynamic power dissipation/package vs. switching frequency and test circuit (4051B)



Typical ON characteristics for 1 of 8 channels (4051B)



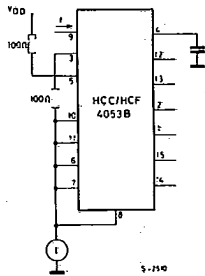
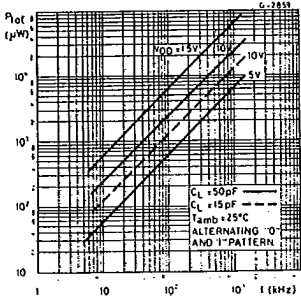
Typical dynamic power dissipation/package vs. switching frequency and test circuit (4052B)





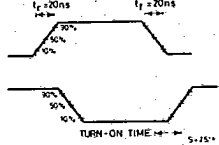
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Typical dynamic power dissipation/package vs. switching frequency and test circuit (4053B)

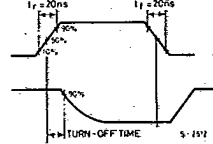


WAVEFORMS

Channel being turned ON ($R_L = 10\text{K}\Omega$)



Channel being turned OFF ($R_L = 300\Omega$)



TYPICAL BIAS VOLTAGES

fig. (a)

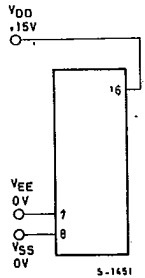


fig. (b)

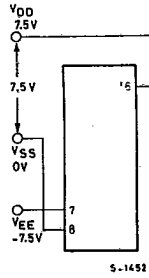


fig. (c)

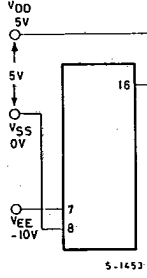
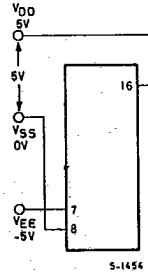


fig. (d)

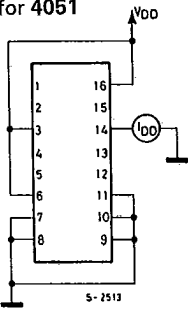


The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD} . The analog signal (through the TG) may swing from V_{EE} to V_{DD} .

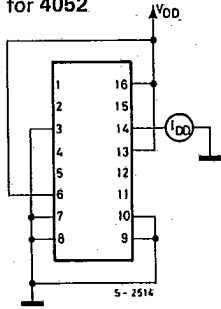
TEST CIRCUITS

OFF channel leakage current-any channel OFF

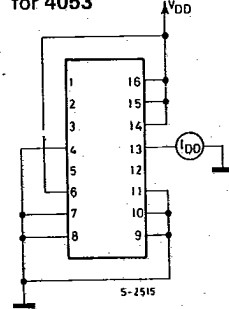
for 4051



for 4052



for 4053



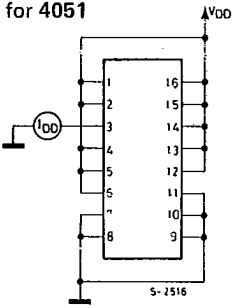
HCC/HCF 4051B
HCC/HCF 4052B
HCC/HCF 4053B

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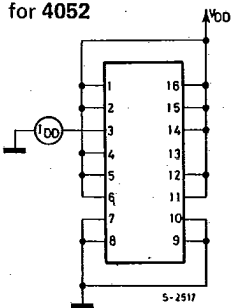
TEST CIRCUITS (continued)

OFF channel leakage current - all channel OFF

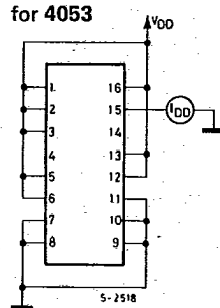
for 4051



for 4052

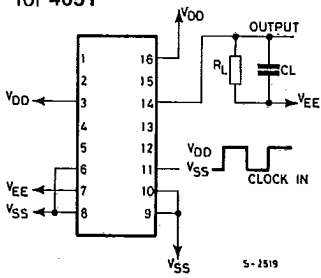


for 4053

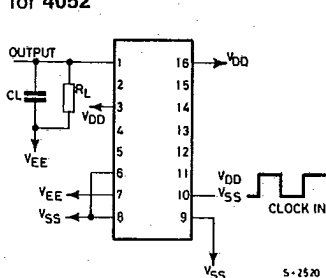


Propagation delay - address input to signal output

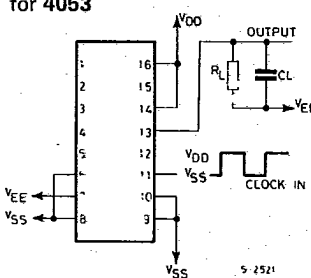
for 4051



for 4052

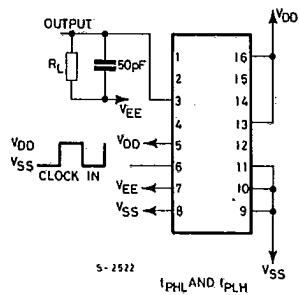


for 4053

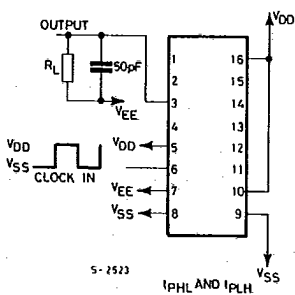


Propagation delay-inhibit input to signal output

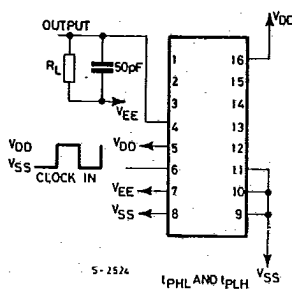
for 4051



for 4052



for 4053



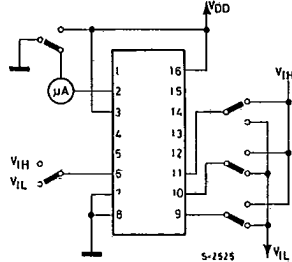


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TEST CIRCUITS (continued)

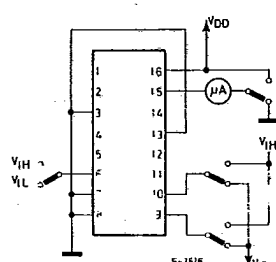
Input voltage

for 4051



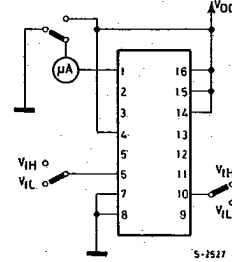
MEASURE $< 2 \mu A$ ON ALL "OFF" CHANNELS (e.g. CHANNEL 6)

for 4052



MEASURE $< 2 \mu A$ ON ALL "OFF" CHANNELS (e.g. CHANNEL 2x)

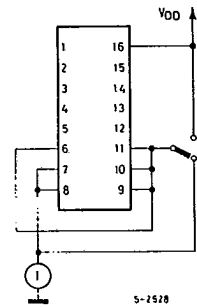
for 4053



MEASURE $2 \mu A$ ON ALL "OFF" CHANNELS (e.g. CHANNEL 6y)

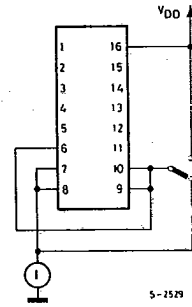
Quiescent device current

for 4051
4053



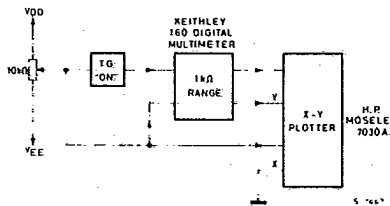
S-2528

for 4052



S-2529

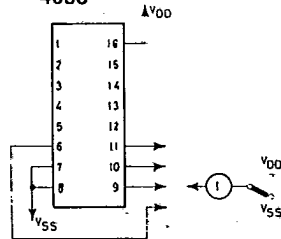
Channel ON resistance measurement circuit



S-2530

Input current

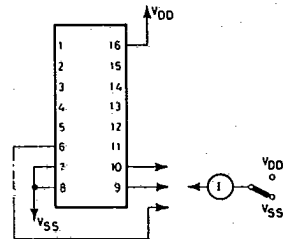
for 4051
4053



S-2532

NOTE: MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

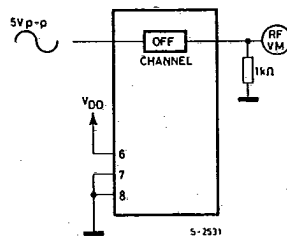
for 4052



S-2534

NOTE: MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

Feedthrough (all types)



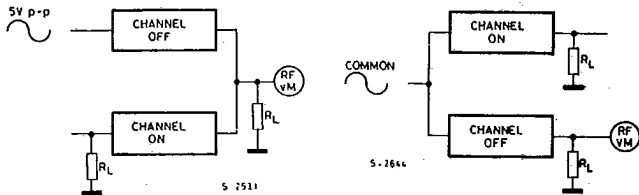
S-2531

HCC/HCF 4051B
 HCC/HCF 4052B
 HCC/HCF 4053B

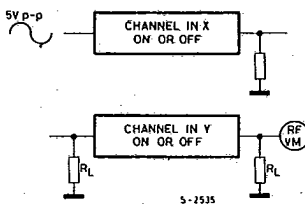
41C 08826 DT-51-11

TEST CIRCUITS (continued)

Crosstalk between any two channels (all types)

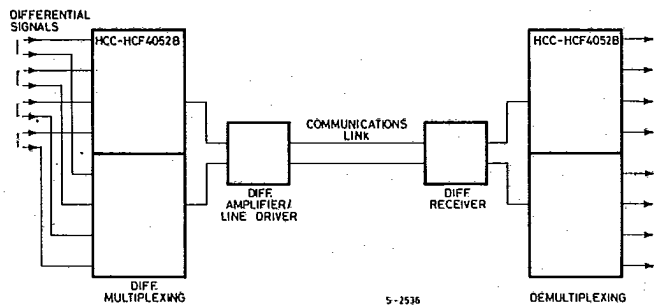


Crosstalk between duals or triplets (4052-4053)



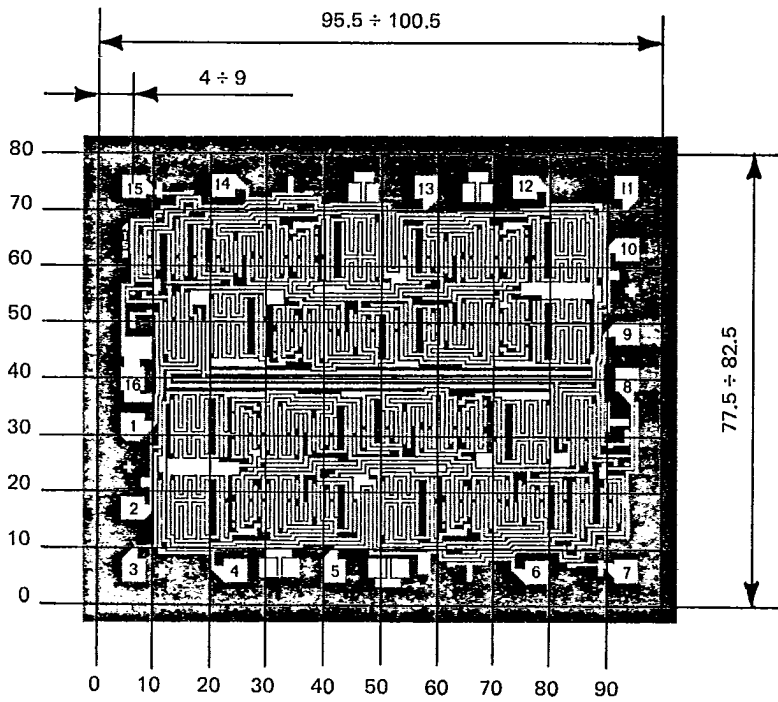
TYPICAL APPLICATIONS

Typical time-division application of the 4052B

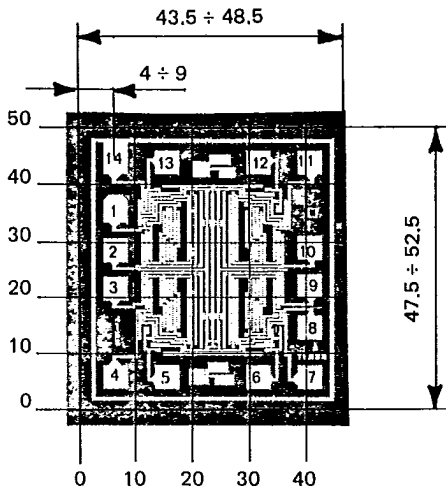


SPECIAL CONSIDERATIONS

Control of analog signals up to 20V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if $V_{DD}-V_{SS}=3V$, a $V_{DD}-V_{EE}$ of up to 13V can be controlled; for $V_{DD}-V_{EE}$ level differences above 13V, a $V_{DD}-V_{SS}$ of at least 4.5V is required). For example, if $V_{DD}=+5V$, $V_{SS}=0$, and $V_{EE}=-13.5V$, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (valuated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into lead 3 on the HCC/HCF 4051; leads 3 and 13 on the HCC/HCF 4052; leads 4, 14, and 15 on the HCC/HCF 4053.



4015B



4016B