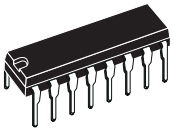
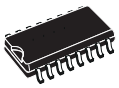
HCF4029B

PRESETTABLE UP/DOWN COUNTER BINARY OR BCD DECADE

- MEDIUM SPEED OPERATION : 8MHz (Typ.) at C_L = 50pF and V_{DD} - V_{SS} = 10V
- MULTI-PACKAGE PARALLEL CLOCKING FOR SYNCHRONOUS HIGH SPEED OUTPUT RESPONSE OR RIPPLE CLOCKING FOR SLOW CLOCK INPUT RISE AND FALL TIMES
- "PRESET ENABLE" AND INDIVIDUAL "JAM" INPUTS PROVIDED
- BINARY OR DECADE UP/DOWN COUNTING
- BCD OUTPUTS IN DECADE MODE
- QUIESCENT CURRENT SPECIF. UP TO 20V
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP



SOP

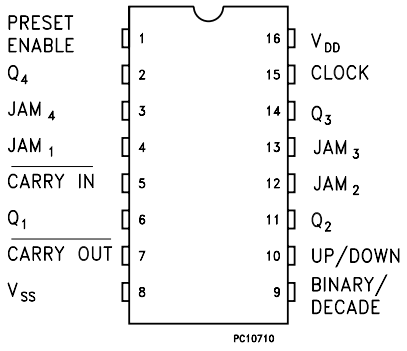
ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4029BEY	
SOP	HCF4029BM1	HCF4029M013TR

DESCRIPTION

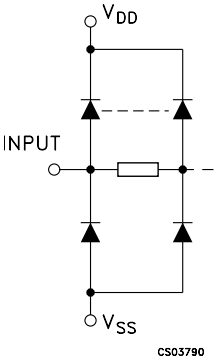
HCF4029B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages.
HCF4029B consists of a four stage binary or BCD-decade up/down counter with provisions for look ahead carry in both counting modes. The inputs consist of a single CLOCK, $\overline{\text{CARRY IN}}$ (CLOCK ENABLE), BINARY/DECADE, UP/DOWN, PRESET ENABLE, and four individual JAM signals. Q1, Q2, Q3, Q4 and a $\overline{\text{CARRY OUT}}$ signal are provided as outputs. A high PRESET ENABLE signal allows information on the JAM INPUTS to preset the counter to any state asynchronously with the clock. A low on each JAM line, when the PRESET-ENABLE signal is high, resets the counter to its zero count. The counter advances one count at the positive transition of the clock when the $\overline{\text{CARRY-IN}}$ and PRESET ENABLE signals are low. Advancement is inhibited when the $\overline{\text{CARRY-IN}}$ or PRESET ENABLE signals are high. The $\overline{\text{CARRY-OUT}}$

PIN CONNECTION



signal is normally high and the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided the CARRY-IN signal is low. The CARRY-IN signal in the low state can thus be considered a CLOCK ENABLE. The CARRY-IN terminal must be connected to V_{SS} when not in use. Binary counting is accomplished when the BINARY/DECODE input is high; the counter counts in the decade mode when the BINARY/DECADE input is low. The counter counts Up when to UP/DOWN INPUT is high, and Down when the UP/DOWN INPUT is low. Multiple packages can be connected in either a parallel clocking or a ripple clocking arrangement. Parallel clocking provides synchronous control and, hence, a faster response from all counting outputs. Ripple clocking allows for longer clock input rise and fall times.

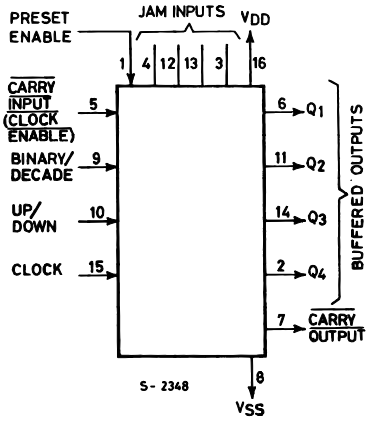
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
15	CLOCK	Clock Input
5	CARRY IN	Carry In Input
9	BINARY/ DECADE	Binary / Decade Select
10	UP/DOWN	Up/Down Select
1	PRESET ENABLE	Preset Enable Input
4, 12, 13, 3	JAM1 to JAM4	Jam Input Signals
6, 11, 14, 2	Q1 to Q4	Q Outputs
7	CARRY OUT	Carry Out Outputs
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM



TRUTH TABLE

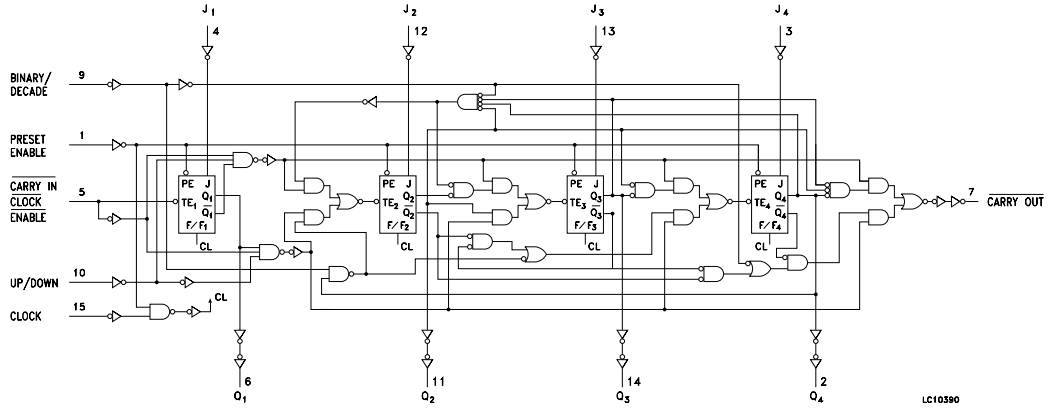
CLOCK	TE	PE	J	Q	$\overline{Q}$
X	X	L	L	L	H
⌐	L	H	X	$\overline{Q}$	Q
X	X	L	H	H	L
⌐	H	H	X	Q	$\overline{Q}$ NC
⌐	X	H	X	Q	$\overline{Q}$ NC

X: Don't Care

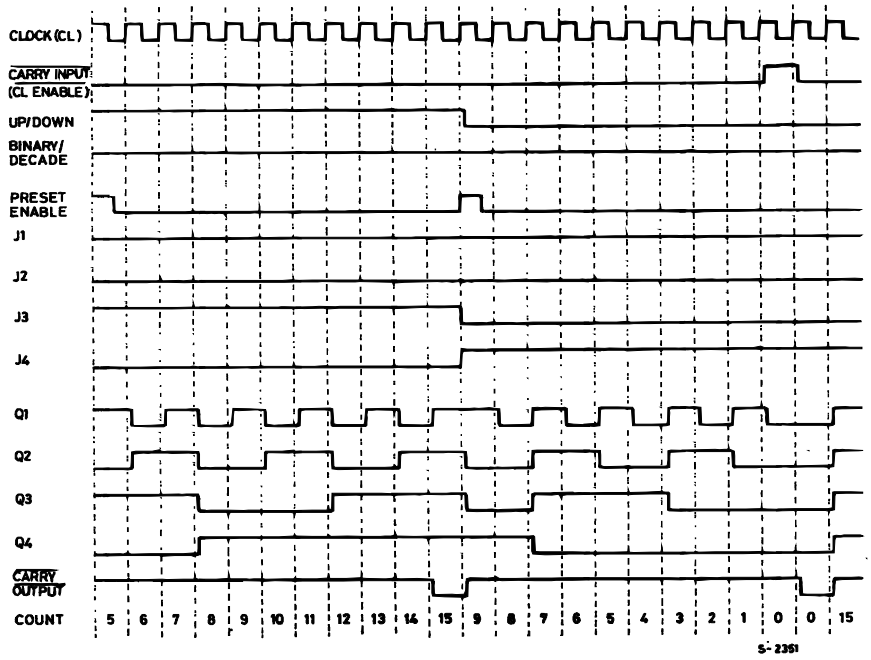
TRUTH TABLE

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/DEC	H	Binary Count
	L	Decade Count
UP/DOWN	H	Up Count
	L	Down Count
PRESET ENABLE	H	Jam In
	L	No Jam
CARRY IN	H	No Counter
	L	Advance counter

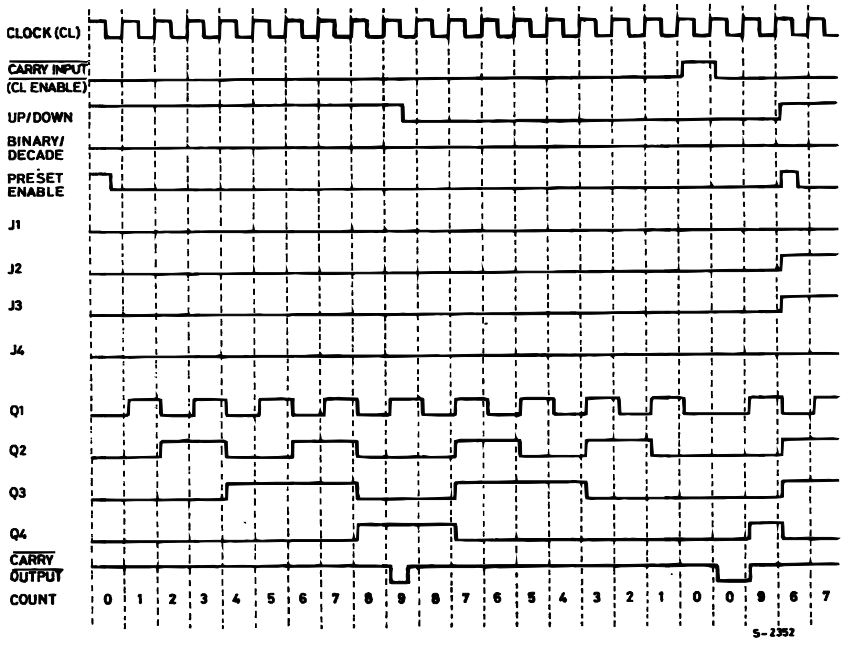
LOGIC DIAGRAM



TIMING CHART - Binary Mode



TIMING CHART - Decade Mode



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/18.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		0.5/4.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			1.5/18.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5		5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6		5	-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4		5	0.44	1		0.36		0.36		mA
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	any input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		any input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

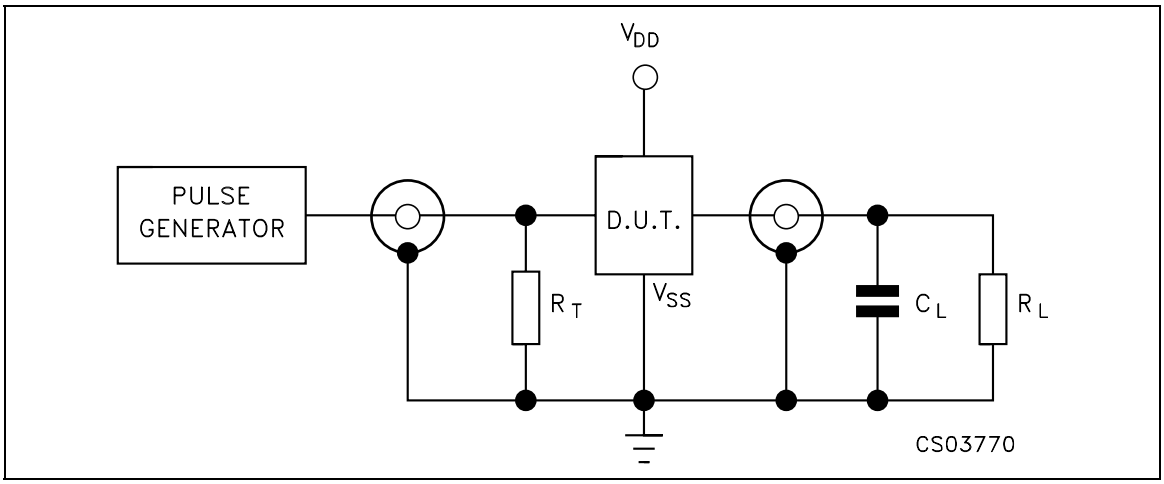
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (Q Outputs)	5			250	500	ns
		10			120	240	
		15			90	180	
t_{PLH} t_{PHL}	Propagation Delay Time (Carry Output)	5			280	560	ns
		10			130	260	
		15			95	190	
t_{THL} t_{TLH}	Transition Time (Q Outputs, Carry Output)	5			100	200	ns
		10			50	100	
		15			40	80	
t_W	Minimum Clock Pulse Width	5			90	180	ns
		10			45	90	
		15			30	60	
$t_{r,}$ t_f (1)	Clock Rise and Fall Time	5				15	ns
		10				15	
		15				15	
t_{setup} (2)	Minimum Setup Time (Carry Input)	5			30	60	ns
		10			10	20	
		15			6	12	
t_{setup}	Minimum Setup Time (B/D or U/D)	5			170	340	ns
		10			70	140	
		15			50	100	
f_{MAX}	Maximum Clock Input Frequency	5		2	4		MHz
		10		4	8		
		15		5.5	11		
PRESET ENABLE							
t_{PLH} t_{PHL}	Propagation Delay Time (Q Outputs)	5			235	470	ns
		10			100	200	
		15			80	160	
t_{PLH} t_{PHL}	Propagation Delay Time (Carry Output)	5			320	640	ns
		10			145	290	
		15			105	210	
t_W	Minimum Preset Enable (Pulse Width)	5			65	130	ns
		10			35	70	
		15			25	50	
t_{rem} (2)	Minimum Preset Enable (Removal Time)	5			100	200	ns
		10			55	110	
		15			40	80	

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
PRESET ENABLE							
t_{PHL} t_{PLH}	Propagation Delay Time (Carry Output)	5			170	340	ns
		10			70	140	
		15			50	100	
t_{setup} (3)	Minimum Setup Time (Carry In)	5			25	50	ns
		10			15	30	
		15			12	25	
t_{hold}	Minimum Hold Time (Carry In)	5			100	200	ns
		10			35	70	
		15			30	60	

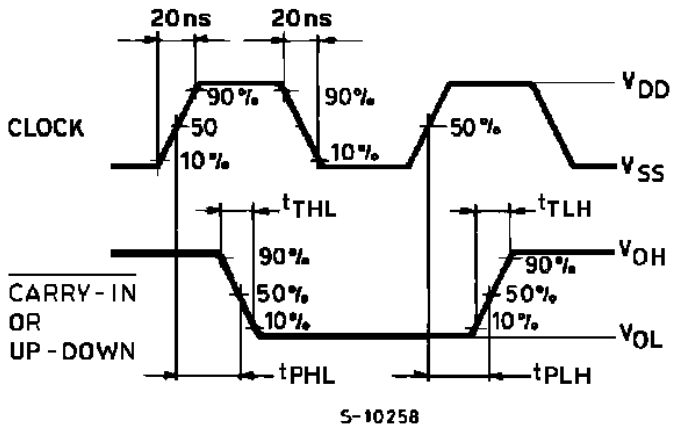
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) If more than one unit is cascated in the parallel clocked application t_r should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitance load.
(2) From Up/Down, Binary/Decade, Carry In or Preset Enable Control Inputs to Clock Edge.
(3) From Carry In to Clock Edge.

TEST CIRCUIT

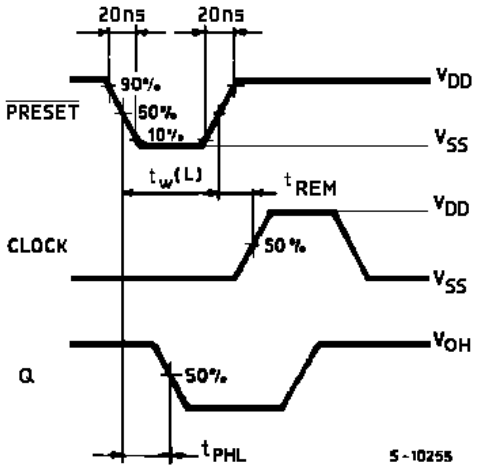


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)

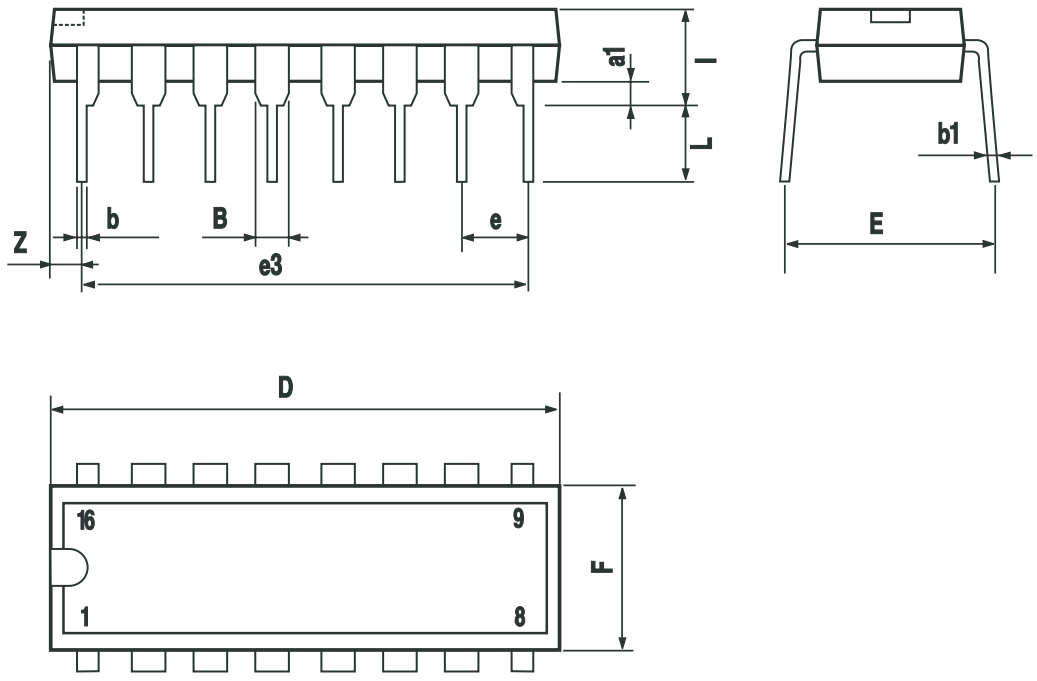


WAVEFORM 2 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-16 (0.25) MECHANICAL DATA

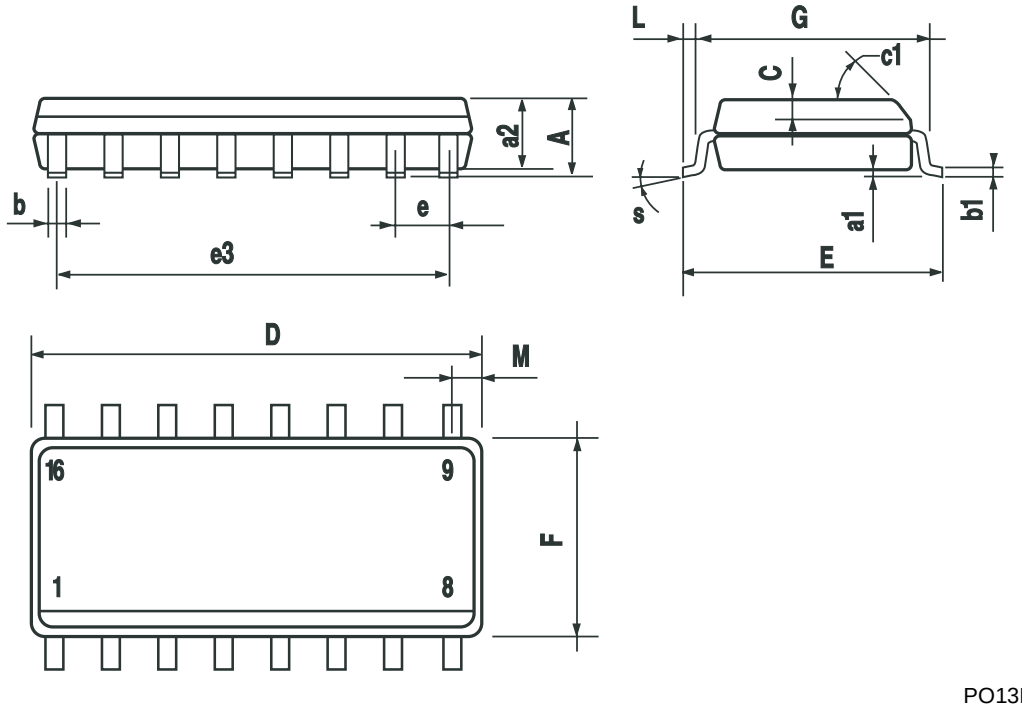
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



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