Notebook LCD Panel EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Provides up to 15dB EMI reduction.
- Generates a low EMI Spread Spectrum clock and a non-spread reference clock of the input frequency.
- Optimized for Frequency range from 20 to 40MHz.
- Internal loop filter minimizes external components and board space.
- Selectable spread options: Down and Center.
- Low Inherent Cycle-to-Cycle jitter.
- Eight spread % selections: ±0.625% to –3.5%.
- ModRate is compliant with ATI M7x VGA spec.
- 3.3V ± 0.3V Operating Voltage range.
- Low power CMOS design.
- Supports notebook VGA and other LCD timing controller applications.
- Power Down function for mobile application.
- Available in Commercial temperature range.
- Available in 8-pin SOIC and TSSOP Packages.

Product Description

The P1819 is a Versatile Spread Spectrum Frequency Modulator designed specifically for input clock frequencies from 20 to 40MHz. (*Refer Input Frequency and Modulation Rate Table).* The P1819 reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The P1819 allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The P1819 modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'Spread Spectrum Clock Generation'.

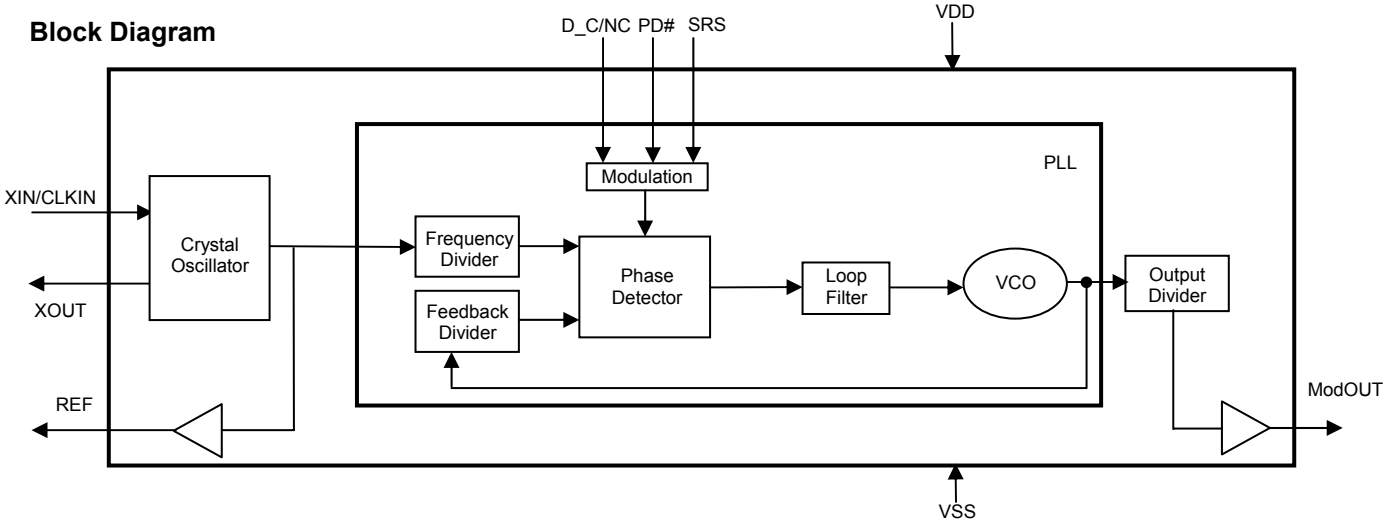
The P1819 is available in different spread deviation, refer to "Spread Deviation Selection" Table.

The P1819 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

Applications

The P1819 is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high-speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.

Block Diagram



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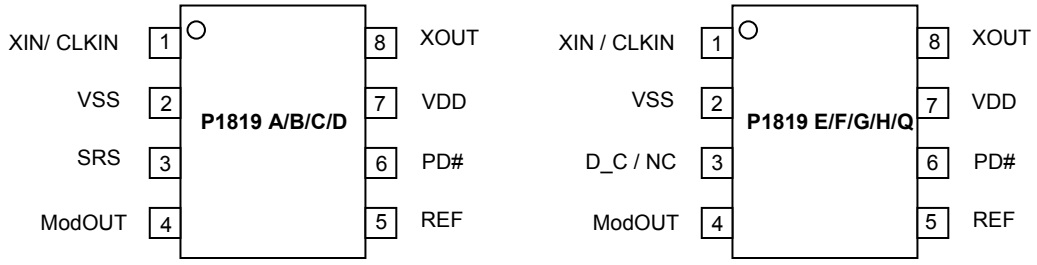
Pin Configuration



Pin Description

Pin#		Pin Name	Type	Description
1819A/B/C/D	1819E/F/G/H/Q			
1	1	XIN / CLKIN	I	Crystal Connection or external frequency input.This pin has dual functions. It can be connected to either an external crystal or an external reference clock
2	2	VSS	P	Ground Connection. Connect to system ground.
3		SRS	I	Spread range select. Digital logic input used to select frequency deviation *(Refer Spread Deviation Selection Table)*. This pin has an internal pull-up resistor.
3	3	D_C / NC	I	Digital logic input used to select Down (LOW) or Center (HIGH) spread options (*Refer Spread Deviation Selection Table)*. This pin has an internal pull-up resistor.
4	4	ModOUT	O	Spread spectrum clock output. *(Refer Input Frequency and Modulation Rate Table and Spread Deviation Selection Table)*
5	5	REF	O	Non-modulated Reference clock output of the input frequency.
6	6	PD#	I	Power down control pin. Pull XIN/CLKIN and PD# LOW to enable Power-Down mode. This pin has an internal pull-up resistor.
7	7	VDD	P	Power Supply for the entire chip.
8	8	XOUT	O	Crystal Connection. Input connection for an external crystal. If using an external reference, this pin must be left unconnected.

Note: Pin 3 is NC in P1819Q

Input Frequency and Modulation Rate

Part Number	Input Frequency Range	Output Frequency range	Modulation rate
P1819	20MHz to 40MHz	20MHz to 40MHz	Input Frequency / 896

Spread Deviation Selection

Part Number	SRS	D_C	Spread Deviation
P1819A	0	NA	-2.50% (DOWN)
	1		-3.50% (DOWN)
P1819B	0	NA	-1.25% (DOWN)
	1		-1.75% (DOWN)
P1819C	0	NA	±1.25% (CENTER)
	1		±1.75% (CENTER)
P1819D	0	NA	±0.625% (CENTER)
	1		±0.875% (CENTER)
P1819E	NA	0	-1.25% (DOWN)
		1	±0.625% (CENTER)
P1819F	NA	0	-2.5% (DOWN)
		1	±1.25% (CENTER)
P1819G	NA	0	-1.75% (DOWN)
		1	±0.875% (CENTER)
P1819H	NA	0	-3.5% (DOWN)
		1	±1.75% (CENTER)
P1819Q	NA	NA	-2.5% (DOWN)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	-0.5 to +7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

DC Electrical Characteristics

(Test condition: All parameters are measured at room temperature (+25°C) unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low voltage	VSS – 0.3		0.8	V
V_{IH}	Input High voltage	2.0		V_{DD} + 0.3	V
I_{IL}	Input Low current (inputs D_C, PD#, SRS)	-60.0		-20.0	µA
I_{IH}	Input High current			1.0	µA
I_{XOL}	X_{OUT} Output low current @ 0.4V, V_{DD} = 3.3V	2.0		12.0	mA
I_{XOH}	X_{OUT} Output high current @ 2.5V, V_{DD} = 3.3V			12.0	mA
V_{OL}	Output Low voltage V_{DD} = 3.3V, I_{OL} = 20mA			0.4	V
V_{OH}	Output High voltage V_{DD} = 3.3V, I_{OH} = 20mA	2.5		-	V
I_{CC}	Dynamic supply current normal mode 3.3V and 25pF probe loading	7.1 $f_{IN - min}$		26.9 $f_{IN - max}$	mA
I_{DD}	Static supply current standby mode		4.5		mA
V_{DD}	Operating Voltage	3.0	3.3	3.6	V
t_{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock Output impedance		50		Ω

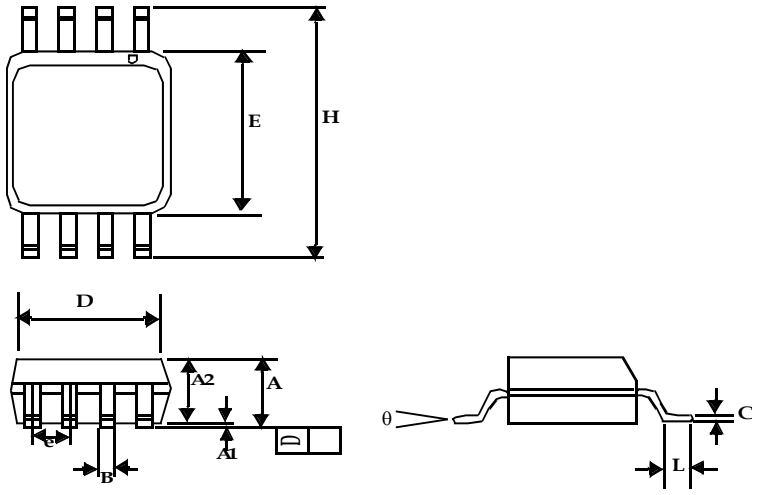
AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency	20		40	MHz
f_{OUT}	Output Frequency	20		40	MHz
t_{LH}*	Output Rise time Measured from 0.8V to 2.0V		0.66		nS
t_{HL}*	Output Fall time Measured from 2.0V to 0.8V		0.65		nS
t_{JC}	Jitter (cycle to cycle)	-200		200	pS
t_{LTJ}	Long Term Jitter,(1000 cycle) on Refout @ 27MHz		475		pS
t_D	Output Duty cycle	45	50	55	%

*t_{LH} and t_{HL} are measured into a capacitive load of 15pF

Package Information

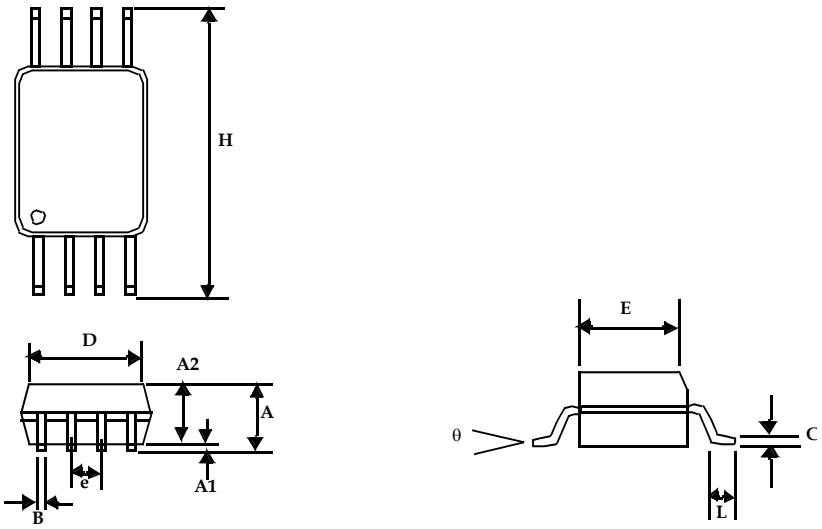
8-Pin SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Note: Controlling dimensions are millimeters
SOIC – 0.074 grams unit weight

8-Pin TSSOP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.10
A1	0.002	0.006	0.05	0.15
A2	0.033	0.037	0.85	0.95
B	0.008	0.012	0.19	0.30
c	0.004	0.008	0.09	0.20
D	0.114	0.122	2.90	3.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.028	0.50	0.70
θ	0°	8°	0°	8°

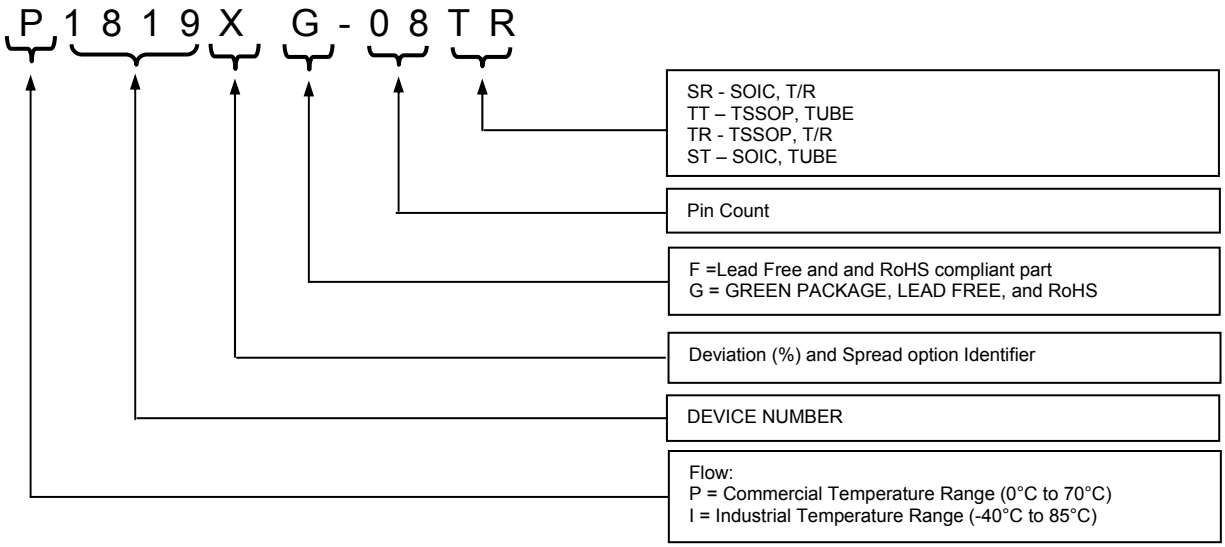
Note: Controlling dimensions are millimeters
TSSOP – 0.0325 grams unit weight

Ordering Codes

Part Number	Marking	Package Type	Temperature
P1819XF-08ST	P1819XF	8-pin SOIC, tube	Commercial
P1819XF-08SR	P1819XF	8-pin SOIC, tape & reel	Commercial
P1819XF-08TT	P1819XF	8-pin TSSOP, tube	Commercial
P1819XF-08TR	P1819XF	8-pin TSSOP, tape & reel	Commercial
P1819XG-08ST	P1819XG	8-pin SOIC, tube	Commercial
P1819XG-08SR	P1819XG	8-pin SOIC, tape & reel	Commercial
P1819XG-08TT	P1819XG	8-pin TSSOP, tube	Commercial
P1819XG-08TR	P1819XG	8-pin TSSOP, tape & reel	Commercial

Products are available for industrial temperature range operation. Please contact factory for more information.
Note: X=A/B/C/D/E/F/G/H/Q

Device Ordering Information



Note: X=A/B/C/D/E/F/G/H/Q

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to PulseCore Semiconductor, dated 11-11-2003