RENESAS

HD74LS192 Synchronous Up / Down Decade Counter (dual clock lines)

REJ03D0454-0200 Rev.2.00 Feb.18.2005

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the output change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high. This counter is fully programmable; that is, each output may be preset to either level by desired data at the data inputs while the load inputs is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs. A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words. This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up-and down-counting functions.

The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count up input when an overflow condition exists.

The counters can be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of .the succeeding counter.

Features

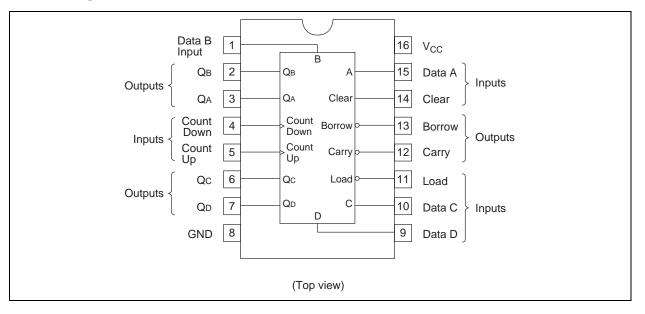
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS192P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	—
HD74LS192FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

• Ordering Information

Note: Please consult the sales office for the above package availability.

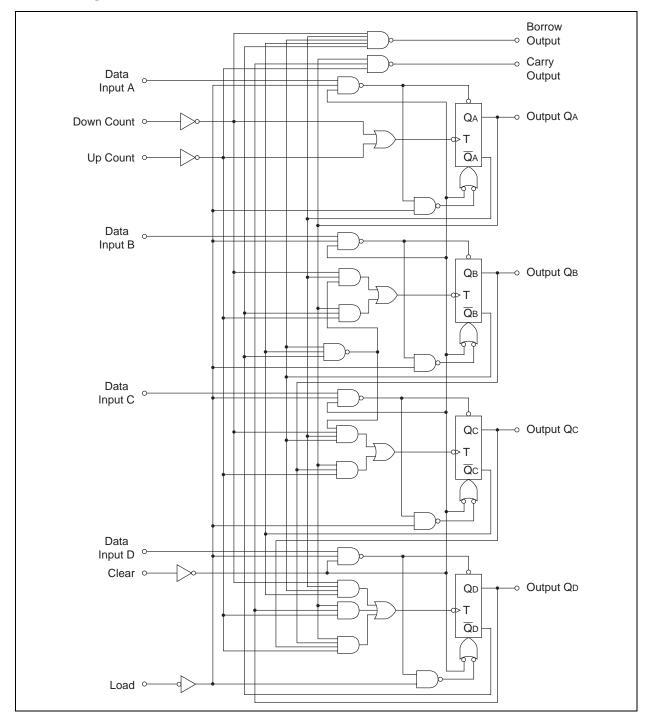


Pin Arrangement





Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	PT	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Rev.2.00, Feb.18.2005, page 3 of 10



Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	V
	I _{ОН}	—	—	-400	μA
Output current	l _{oL}	—	—	8	mA
Operating temperature	T _{opr}	-20	25	75	°C
Clock frequency	fclock	0	—	25	MHz
Pulse width	t _w	20	—	—	ns
Setup time (Clear)	t _{su (CLR)}	40	—	—	ns
Setup time	t _{su}	20	—	—	ns
Hold time	t _h	3	—	—	ns

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

ltem	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0			V	
Input voltage	VIL			0.8	V	
	V _{он}	2.7			V	$V_{CC} = 4.75 \text{ V}, \text{ V}_{IH} = 2 \text{ V}, \text{ V}_{IL} = 0.8 \text{ V},$
	VOH	2.1	_	_	v	I _{OH} = -400 μA
Output voltage	V _{OL}			0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, \text{ V}_{IH} = 2 \text{ V},$
		_	_	0.5	v	I _{OL} = 8 mA V _{IL} = 0.8 V
	I _{IH}	_	_	20	μΑ	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 2.7 \text{ V}$
Input current	IIL	_	_	-0.4	mA	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 0.4 \text{ V}$
	l _l	_	_	0.1	mA	$V_{CC} = 5.25 \text{ V}, \text{ V}_{I} = 7 \text{ V}$
Short-circuit output	l	-20		-100	mA	V _{CC} = 5.25 V
current	I _{OS}	-20	_	-100	ШA	V _{CC} – 5.25 V
Supply current**	Icc	_	19	34	mA	V _{CC} = 5.25 V
Input clamp voltage	Vık			-1.5	V	$V_{CC} = 4.75 \text{ V}, \text{ I}_{IN} = -18 \text{ mA}$

Notes: * $V_{CC} = 5 V$, Ta = 25°C

 ** I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

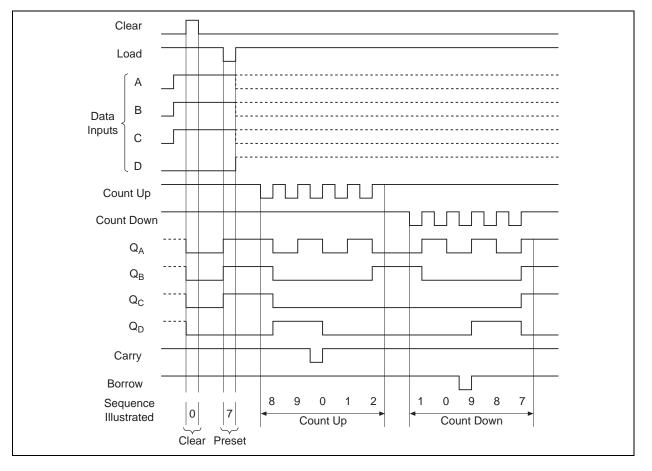
Switching Characteristics

 $(V_{CC} = 5 V, Ta = 25^{\circ}C)$

							(,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	v, 1a = 25 C)
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{\sf max}$			25	32	—	MHz	
	t _{PLH}	Countin	Carry	_	17	26	ns	C _L = 15 pF, R _L = 2 kΩ
	t _{PHL}	Count-up		_	18	24		
	t _{PLH}	Count-down	Borrow	—	16	24	ns	
	t _{PHL}			—	15	24		
Propagation delay time	t _{PLH}	Either Count	Q	—	27	38	ns	
	t _{PHL}			_	30	47		
	t _{PLH}	Lood	Q	_	24	40	ns	
	t _{PHL}	Load		—	25	40		
	t _{PHL}	Clear	Q	_	23	35	ns	



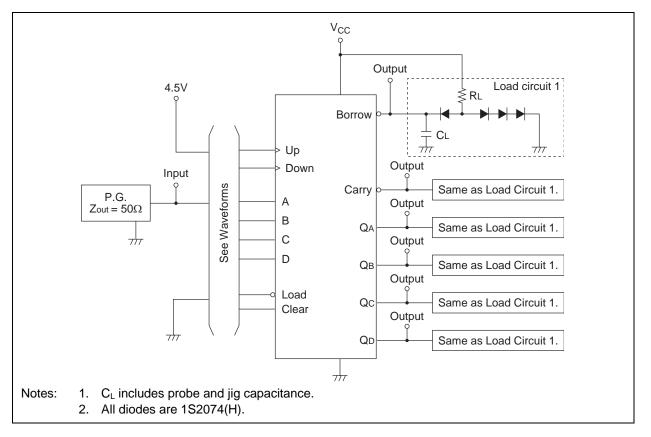
Count Sequence





Testing Method

Test Circuit



Testing Table

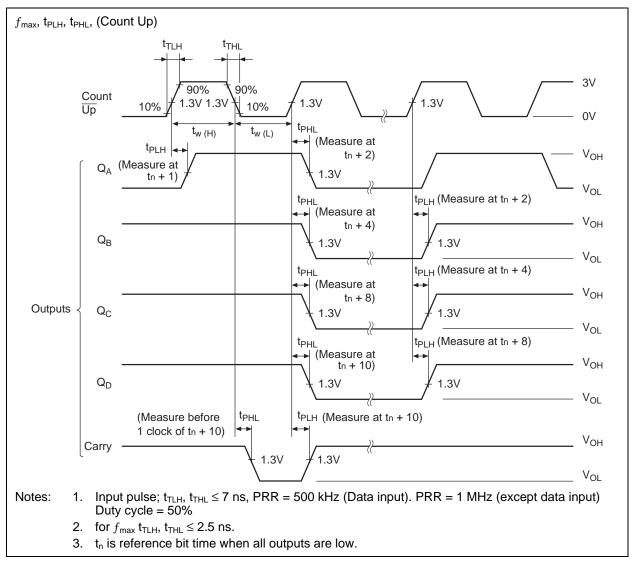
Item	From input to output	Inputs									
item		CLR	Load	Up	Down	Α	В	С	D		
£		GND	4.5V	IN	4.5V	GND	GND	GND	GND		
∫ max		GND	4.5V	4.5V	IN	GND	GND	GND	GND		
	Up Count	GND	4.5V	IN	4.5V	GND	GND	GND	GND		
t _{PLH}	Down Count	GND	4.5V	4.5V	IN	GND	GND	GND	GND		
t _{PHL}	Load→Q	GND	IN	GND	GND	IN	IN	IN	IN		
	Clear→Q	IN	IN*	GND	GND	4.5V	4.5V	4.5V	4.5V		

Note: *. For initialized

Item	From input to output	Outputs									
Item		Q _A	Q _B	Q _c	QD	Carry	Borrow				
£		OUT	OUT	OUT	OUT	OUT	—				
Jmax		OUT	OUT	OUT	OUT	_	OUT				
	Up Count	OUT	OUT	OUT	OUT	OUT	—				
t _{PLH}	Down Count	OUT	OUT	OUT	OUT		OUT				
t _{PHL}	Load→Q	OUT	OUT	OUT	OUT		—				
	Clear→Q	OUT	OUT	OUT	OUT		—				

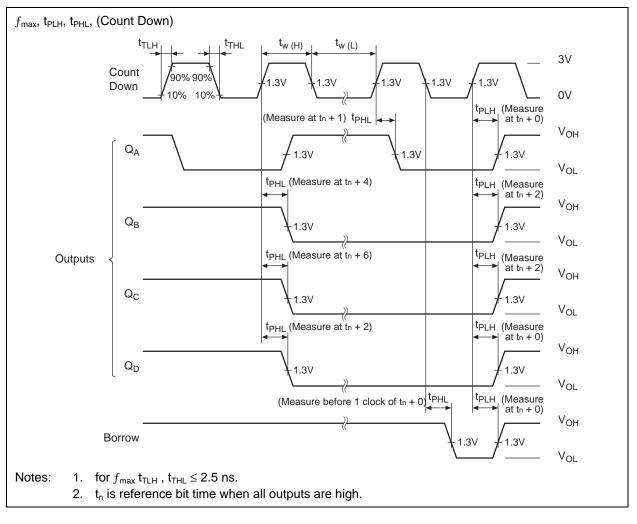


Waveforms 1



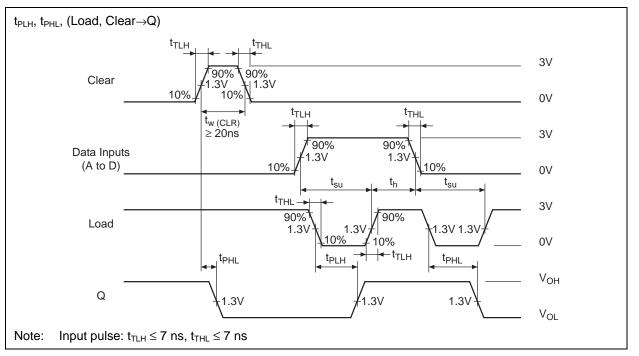


Waveforms 2



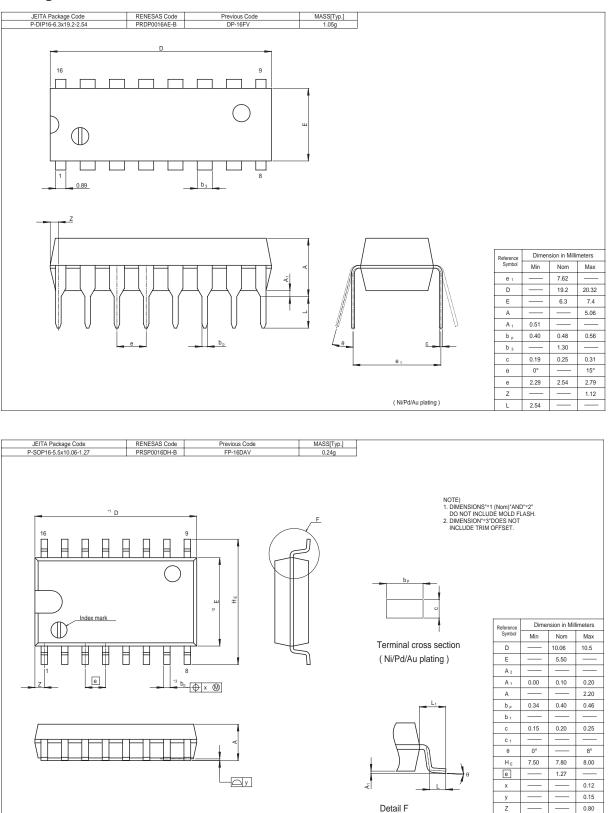


Waveforms 3





Package Dimensions





L

L 1

0.50

0.70

1.15 -----

0.90

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