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# HD74LVC540A

Octal Buffers / Line Drivers with 3-state Outputs

## HITACHI

ADE-205-114B(Z)

3rd Edition

December 1996

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### Description

The HD74LVC540A has eight inverter drivers with three state outputs in a 20 pin package. When  $\overline{G1}$  and  $\overline{G2}$  is low level, this drivers set up output is enable. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH} (\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- All outputs  $V_{OUT} (\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V or output off state})$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V, }T_a = 25^\circ\text{C})$
- High output current  $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$

### Function Table

Inputs			Output $\overline{Y}$
$\overline{G1}$	$\overline{G2}$	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H: High level

L: Low level

X: Immaterial

Z: High impedance

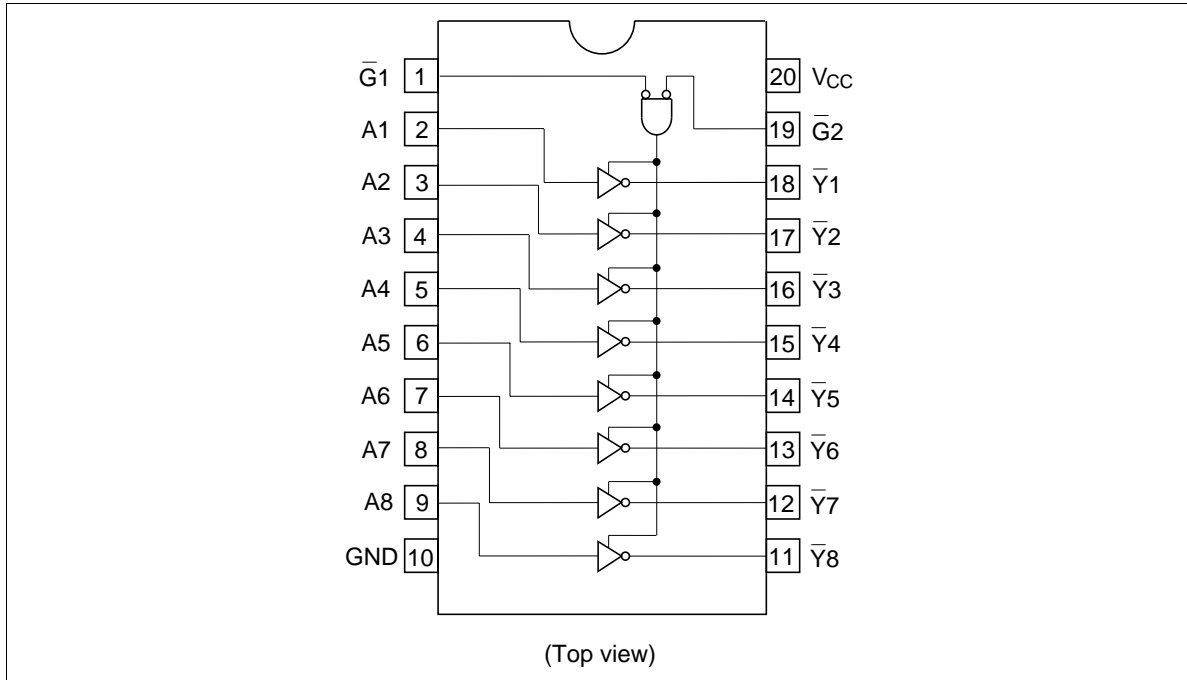


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## Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 6.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5$ V
Input voltage	$V_I$	-0.5 to 6.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5$ V
		50	mA	$V_O = V_{CC} + 0.5$ V
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$	V	Output "H" or "L"
		-0.5 to 6.0	V	Output "Z" or $V_{CC}:OFF$
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	100	mA	
Storage temperature	Tstg	-65 to +150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

**Recommended Operating Conditions**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.5 to 5.5	V	Data hold
		2.0 to 5.5	V	At operation
Input / output voltage	$V_I$	0 to 5.5	V	$\overline{G1}$ , $\overline{G2}$ , A
		0 to $V_{CC}$	V	Output "H" or "L"
		0 to 5.5	V	Output "Z" or $V_{CC}:OFF$
Operating temperature	Ta	-40 to 85	°C	
Output current	$I_{OH}$	-12	mA	$V_{CC} = 2.7$ V
		$-24^{*2}$	mA	$V_{CC} = 3.0$ V to 5.5 V
	$I_{OL}$	12	mA	$V_{CC} = 2.7$ V
		$24^{*2}$	mA	$V_{CC} = 3.0$ V to 5.5 V
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle  $\leq 50\%$

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## Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C		Unit	Test Conditions
			Min	Max		
Input voltage	V <sub>IH</sub>	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	V <sub>CC</sub> ×0.7	—	V	
	V <sub>IL</sub>	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	V <sub>CC</sub> ×0.3	V	
Output voltage	V <sub>OH</sub>	2.7 to 5.5	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA
		2.7	2.2	—	V	I <sub>OH</sub> = -12 mA
		3.0	2.4	—	V	
		3.0	2.2	—	V	I <sub>OH</sub> = -24 mA
		4.5	3.8	—	V	
	V <sub>OL</sub>	2.7 to 5.5	—	0.2	V	I <sub>OL</sub> = 100 μA
		2.7	—	0.4	V	I <sub>OL</sub> = 12 mA
		3.0	—	0.55	V	I <sub>OL</sub> = 24 mA
		4.5	—	0.55	V	
Input current	I <sub>IN</sub>	0 to 5.5	—	±5.0	μA	V <sub>IN</sub> = 5.5 V or GND
Off state output current	I <sub>OZ</sub>	2.7 to 5.5	—	±5.0	μA	V <sub>IN</sub> = V <sub>CC</sub> , GND V <sub>OUT</sub> = 5.5 V or GND
Output leak current	I <sub>OFF</sub>	0	—	20	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 5.5 V
Quiescent supply current	I <sub>CC</sub>	2.7 to 3.6	—	±10	μA	V <sub>IN</sub> / V <sub>OUT</sub> = 3.6 to 5.5 V
		2.7 to 5.5	—	10	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
	ΔI <sub>CC</sub>	3.0 to 3.6	—	500	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6)V, other inputs at V <sub>CC</sub> or GND

**Switching Characteristics**

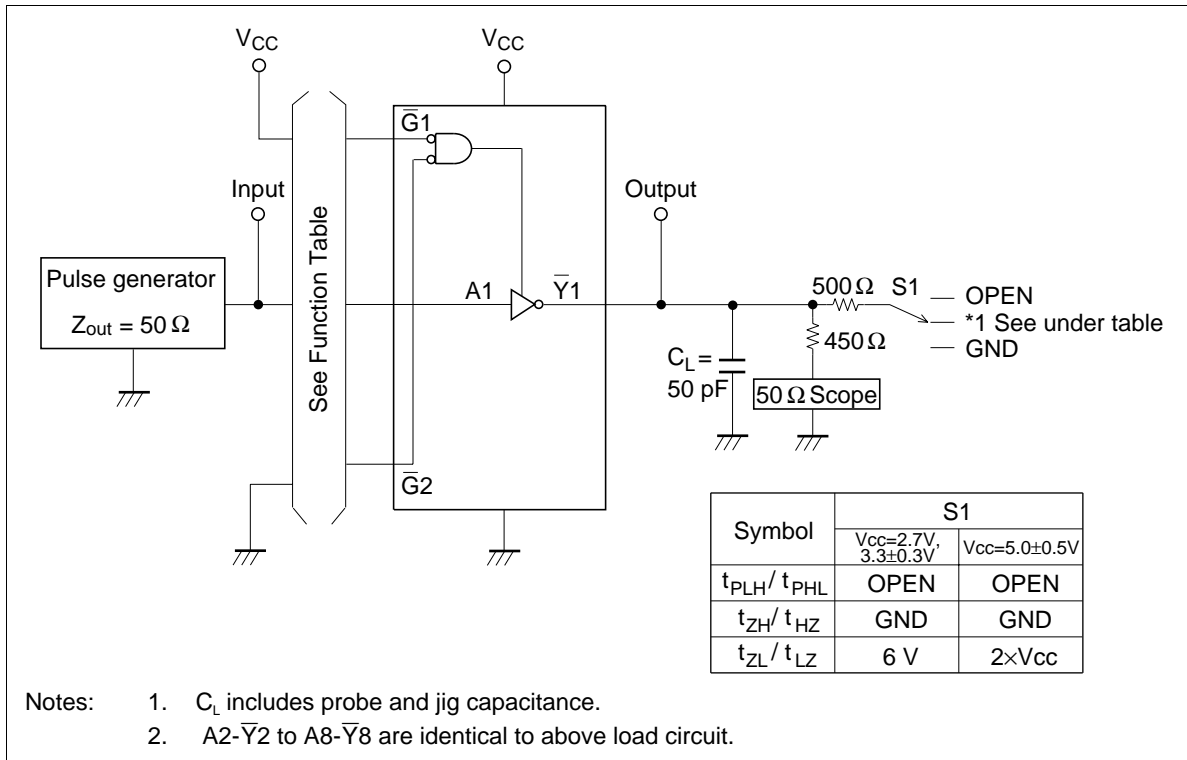
Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Propagation delay time	t <sub>PLH</sub>	2.7	—	—	7.5	ns	A	Y
	t <sub>PHL</sub>	3.3±0.3	1.5	—	6.5	ns		
		5.0±0.5	—	—	5.0	ns		
Output enable time	t <sub>ZH</sub>	2.7	—	—	9.5	ns	G1 or G2	Y
	t <sub>ZL</sub>	3.3±0.3	1.5	—	8.5	ns		
		5.0±0.5	—	—	7.0	ns		
Output disable time	t <sub>HZ</sub>	2.7	—	—	8.5	ns	G1 or G2	Y
	t <sub>LZ</sub>	3.3±0.3	1.5	—	7.5	ns		
		5.0±0.5	—	—	6.5	ns		
Between output pins skew <sup>*1</sup>	t <sub>OSLH</sub>	2.7	—	—	—	ns		
	t <sub>OSHL</sub>	3.3±0.3	—	—	1.0	ns		
		5.0±0.5	—	—	1.0	ns		
Input capacitance	C <sub>IN</sub>	2.7	—	3.0	—	pF		
Output capacitance	C <sub>O</sub>	2.7	—	15.0	—	pF		

Note: 1. This parameter is characterized but not tested.

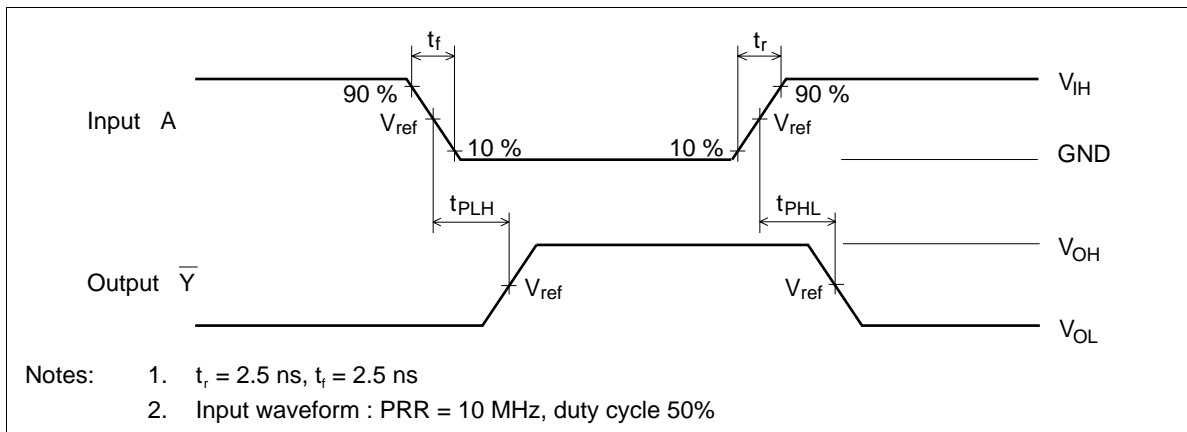
$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

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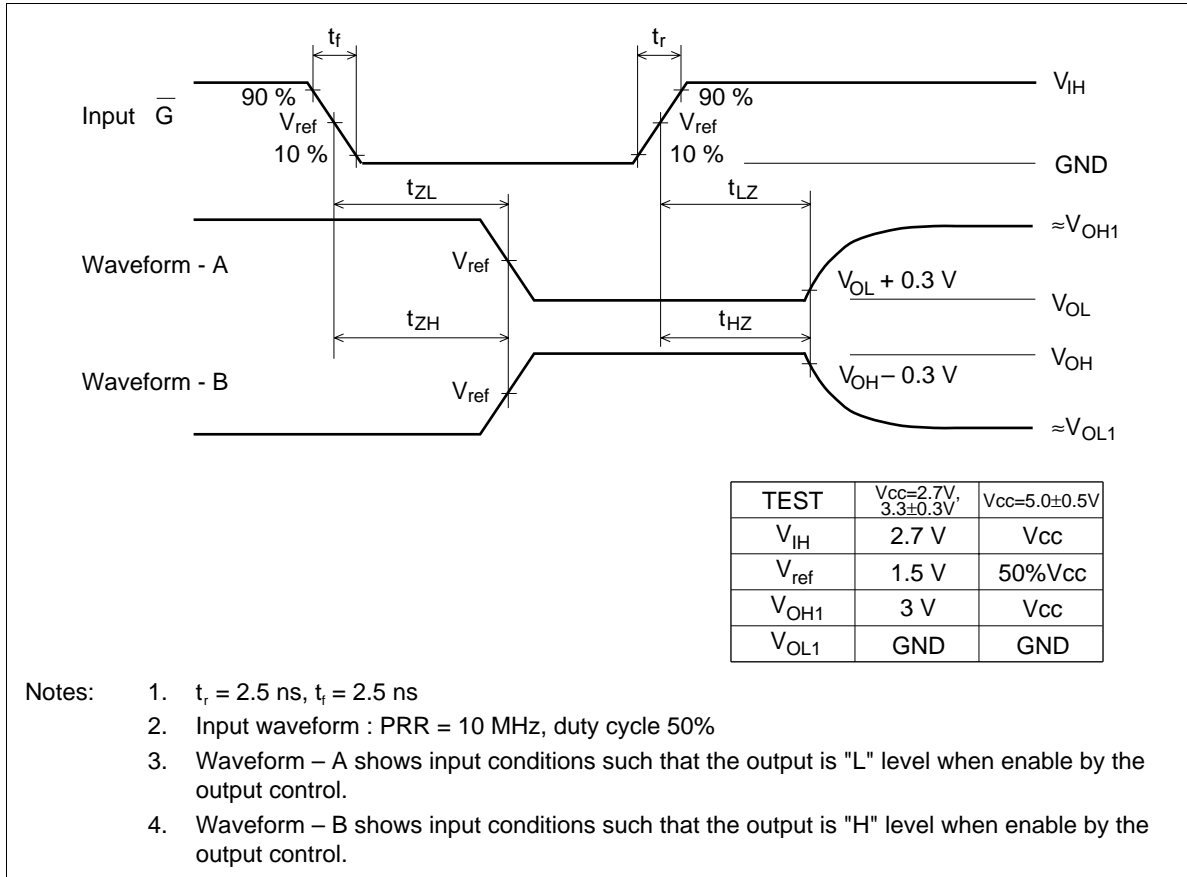
## Test Circuit



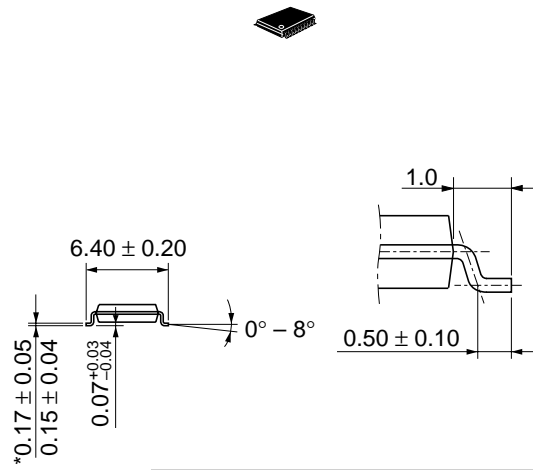
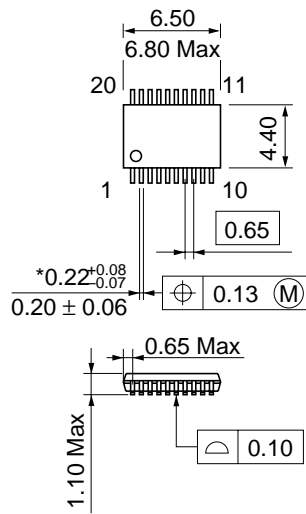
## Waveforms - 1



## Waveforms – 2



Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g



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# HITACHI

## Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan  
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL      NorthAmerica      : <http://semiconductor.hitachi.com/>  
             Europe                : <http://www.hitachi-eu.com/hel/ecg>  
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## For further information write to:

Hitachi Semiconductor  
(America) Inc.  
179 East Tasman Drive,  
San Jose, CA 95134  
Tel: <1> (408) 433-1990  
Fax: <1> (408) 433-0223

Hitachi Europe GmbH  
Electronic components Group  
Dornacher StraÙe 3  
D-85622 Feldkirchen, Munich  
Germany  
Tel: <49> (89) 9 9180-0  
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Group.  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA, United Kingdom  
Tel: <44> (1628) 585000  
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 049318  
Tel: 535-2100  
Fax: 535-1533

Hitachi Asia Ltd.  
Taipei Branch Office  
3F, Hung Kuo Building, No.167,  
Tun-Hwa North Road, Taipei (105)  
Tel: <886> (2) 2718-3666  
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.  
Group III (Electronic Components)  
7/F., North Tower, World Finance Centre,  
Harbour City, Canton Road, Tsim Sha Tsui,  
Kowloon, Hong Kong  
Tel: <852> (2) 735 9218  
Fax: <852> (2) 730 0281  
Telex: 40815 HITEC HX

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