FAIRCHILD SEMICONDUCTOR®

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74VHC4066
Quad Analog Switch

Features

- Typical switch enable time: 15ns
- Wide analog input voltage range: 0–12V
- Low "ON" resistance: 30 Typ. ('4066)
- Low quiescent current: 80µA maximum (74VHC)
- Matched switch characteristics
- Individual switch controls
- Pin and function compatible with the 74HC4066

General Description

These devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the 4066 switches contain linearization circuitry which lowers the "ON" resistance and increases switch linearity. The 4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

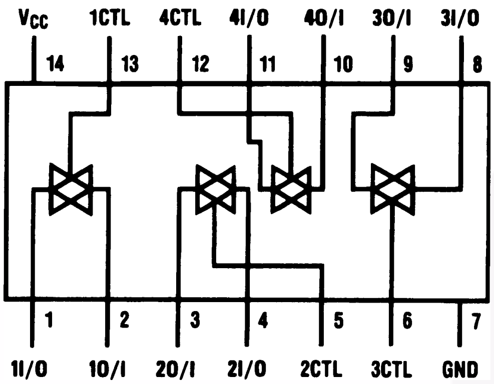
Ordering Information

Order Number	Package Number	Package Description
74VHC4066M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC4066MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

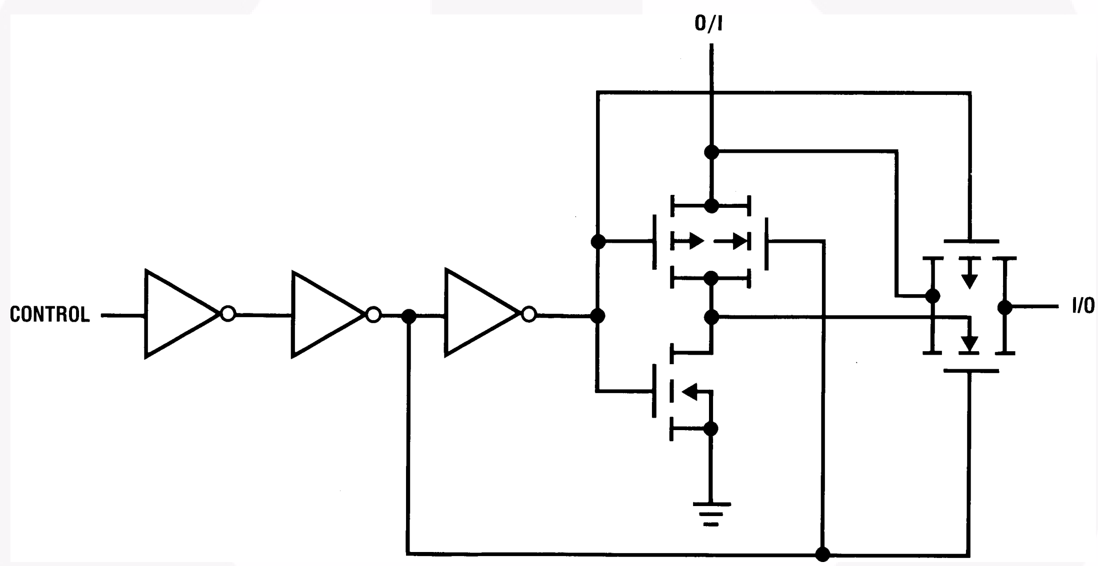


Top View

Truth Table

Input	Switch
CTL	**I/O–O/I**
L	"OFF"
H	"ON"

Schematic Diagram



Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +15V
V_{IN}	DC Control Input Voltage	–1.5 to V_{CC}+1.5V
V_{IO}	DC Switch I/O Voltage	V_{EE}–0.5 to V_{CC}+0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Note:
1. Unless otherwise specified all voltages are referenced to ground.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	12	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise or Fall Times			
	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	
	V_{CC} = 9.0V		400	

DC Electrical Characteristics(2)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C Typ	T_A=25°C Guaranteed Limits	T_A= –40°C to 85°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	
			9.0V		6.3	5.3	
			12.0V		8.4	8.4	
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	
			9.0V		2.7	2.7	
			12.0V		3.6	3.6	
R_{ON}	Maximum "ON" Resistance(3)	$V_{CTL} = V_{IH}$, $I_S = 2.0mA$, $V_{IS} = V_{CC}$ to GND (Fig. 1)	4.5V	100	170	200	Ω
			9.0V	50	85	105	
			12.0V	30	70	85	
		$V_{CTL} = V_{IH}$, $I_S = 2.0mA$, $V_{IS} = V_{CC}$ or GND (Fig. 1)	2.0V	120	180	215	
			4.5V	50	80	100	
			9.0V	35	60	75	
			12.0V	20	40	60	
R_{ON}	Maximum "ON" Resistance Matching	$V_{CTL} = V_{IH}$, $V_{IS} = V_{CC}$ to GND	4.5V	10	15	20	Ω
			9.0V	5	10	15	
			12.0V	5	10	15	
I_{IN}	Maximum Control Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 2 – 6V$			±0.05	±0.5	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	$V_{OS} = V_{CC}$ or GND, V_{IS} = GND or V_{CC}, $V_{CTL} = V_{IL}$ (Fig. 2)	6.0V	10	±60	±600	nA
			9.0V	15	±80	±800	
			12.0V	20	±100	±1000	
I_{IZ}	Maximum Switch "ON" Leakage Current	$V_{IS} = V_{CC}$ to GND, $V_{CTL} = V_{IH}$, V_{OS} = OPEN (Fig. 3)	6.0V	10	±40	±150	nA
			9.0V	15	±50	±200	
			12.0V	20	±60	±300	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0μA$	6.0V		1.0	10	μA
			9.0V		2.0	20	
			12.0V		4.0	40	

Notes:

2. For a power supply of 5V ± 10% the worst case on resistance (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.
3. At supply voltages (V_{CC} – GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–12V, C_L = 50pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A= 25°C		T_A= –40°C to 85°C	Units
				Typ.	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		3.3V	25	30	20	ns
			4.5V	5	10	13	
			9.0V	4	8	10	
			12.0V	3	7	11	
t_{PZL}, t_{PZH}	Maximum Switch Turn “ON” Delay	R_L = 1kΩ	3.3V	30	58	73	ns
			4.5V	12	20	25	
			9.0V	6	12	15	
			12.0V	5	10	13	
t_{PHZ}, t_{PLZ}	Maximum Switch Turn “OFF” Delay	R_L = 1kΩ	3.3V	60	100	125	ns
			4.5V	25	36	45	
			9.0V	20	32	40	
			12.0V	15	30	38	
	Minimum Frequency Response (Fig. 7) 20 log (V_O/V_I) = –3dB	R_L = 600Ω, V_{IS} = 2 V_{PP} at (V_{CC} / 2)(4)(5)	4.5V	40			MHz
			9.0V	100			
	Crosstalk Between any Two Switches (Fig. 8)	R_L = 600Ω, F = 1MHz(5)(6)	4.5V	–52			dB
			9.0V	–50			
	Peak Control to Switch Feedthrough Noise (Fig. 9)	R_L = 600Ω, F = 1 MHz, C_L = 50 pF	4.5V	100			mV
			9.0V	250			
	Switch OFF Signal Feedthrough Isolation (Fig. 10)	R_L = 600Ω, F = 1 MHz, $V_{(CT)}$ V_{IL} (5)(6)	4.5V	–42			dB
			9.0V	–44			
THD	Total Harmonic Distortion (Fig. 11)	R_L = 10 kΩ, C_L = 50pF, F = 1kHz					%
		V_{IS} = 4 V_{PP}	4.5V	.013			
		V_{IS} = 8 V_{PP}	9.0V	.008			
C_{IN}	Maximum Control Input Capacitance			5	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20			pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		0.5			pF
C_{PD}	Power Dissipation Capacitance			15			pF

Notes:

4. Adjust 0dBm for F = 1kHz (Null R_L / R_{ON} Attenuation).
5. V_{IS} is centered at V_{CC} / 2.
6. Adjust input for 0dBm.

AC Test Circuits and Switching Time Waveforms

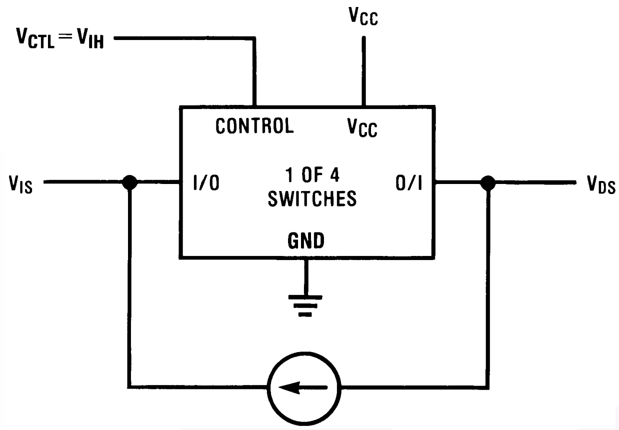


Figure 1. "ON" Resistance

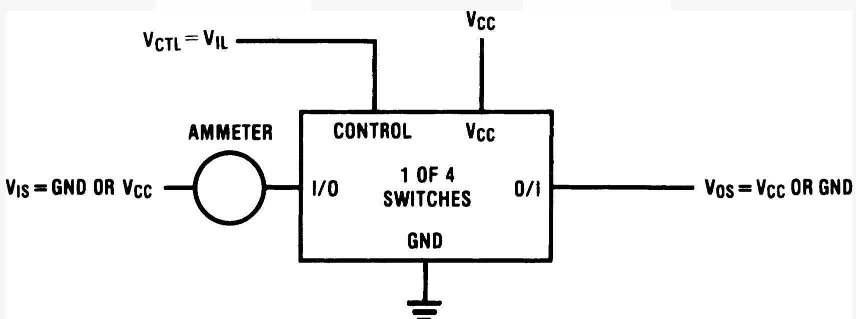


Figure 2. "OFF" Channel Leakage Current

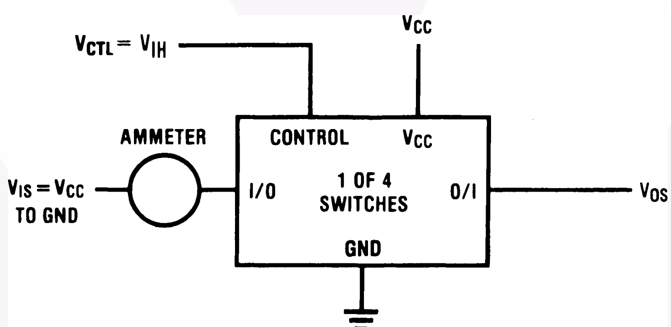


Figure 3. "ON" Channel Leakage Current

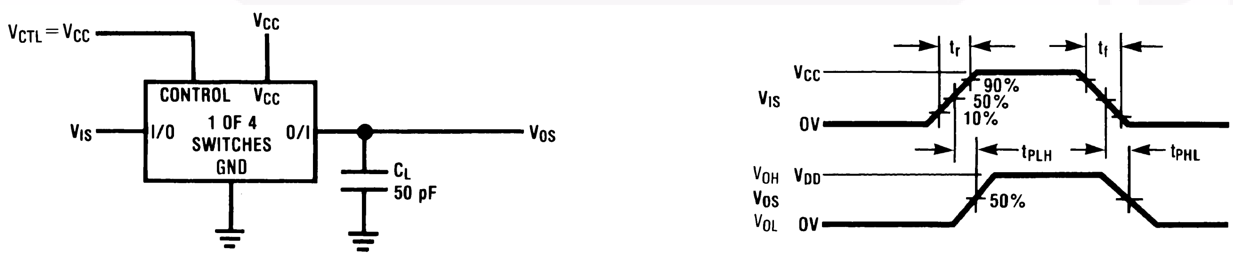


Figure 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

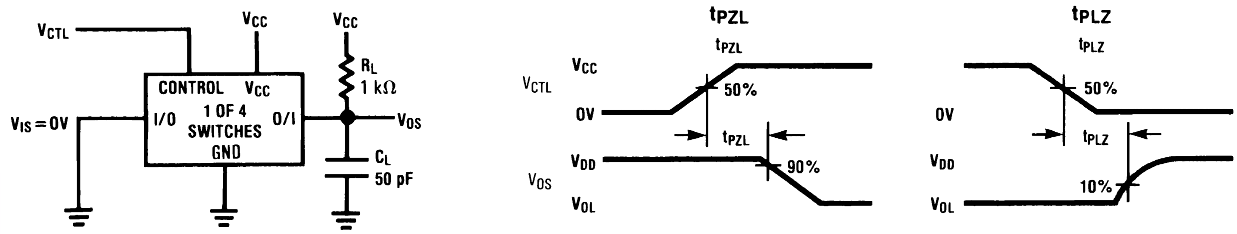


Figure 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

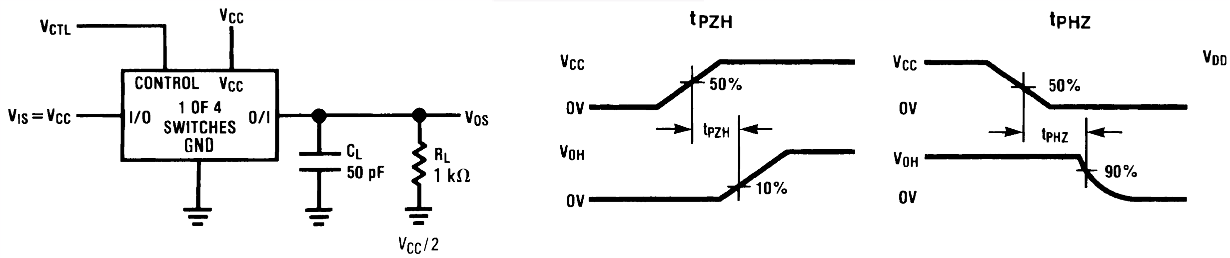


Figure 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

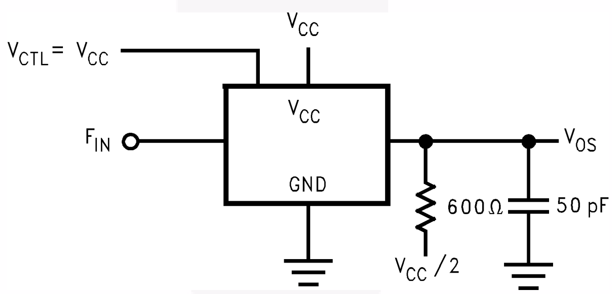


Figure 7. Frequency Response

Crosstalk and Distortion Test Circuits

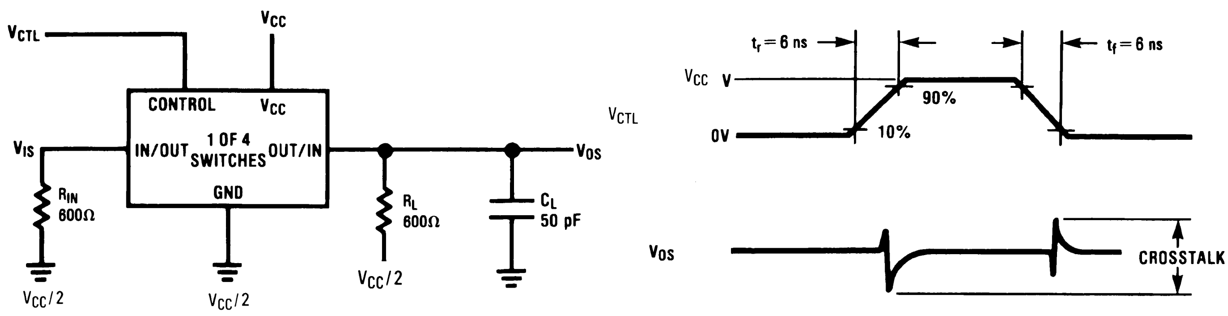


Figure 8. Crosstalk: Control Input to Signal Output

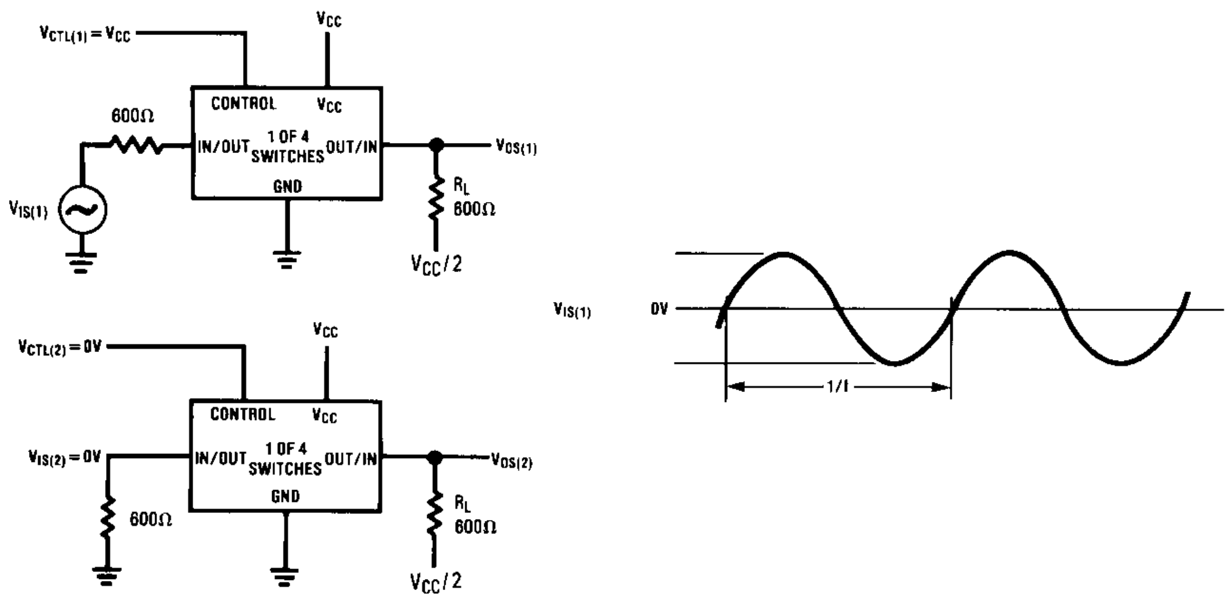


Figure 9. Crosstalk Between Any Two Switches

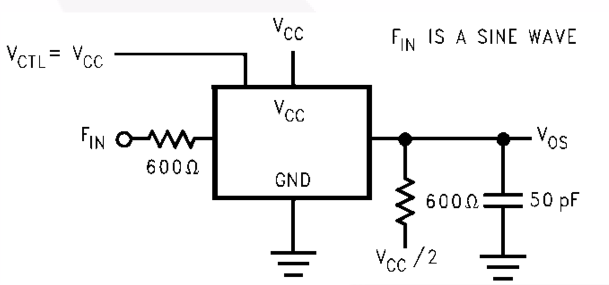


Figure 10. Switch OFF Signal Feedthrough Isolation

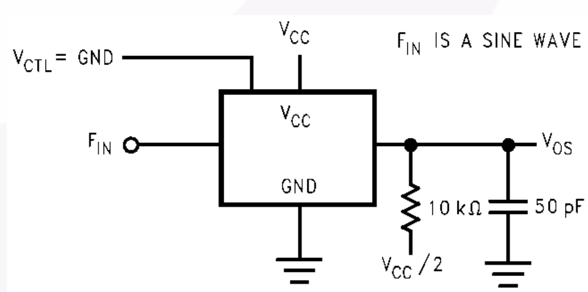
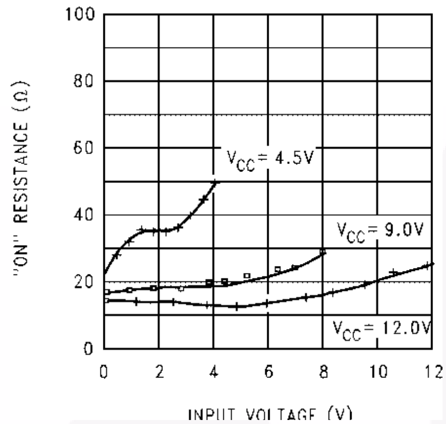


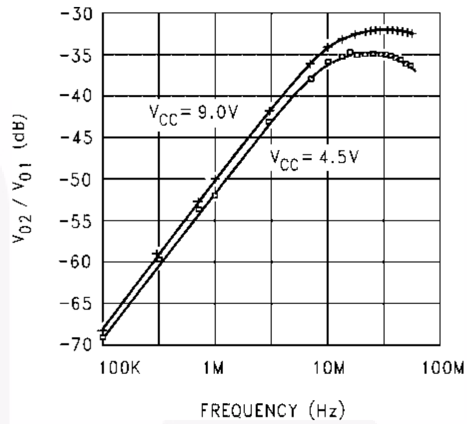
Figure 11. Sinewave Distortion

Typical Performance Characteristics

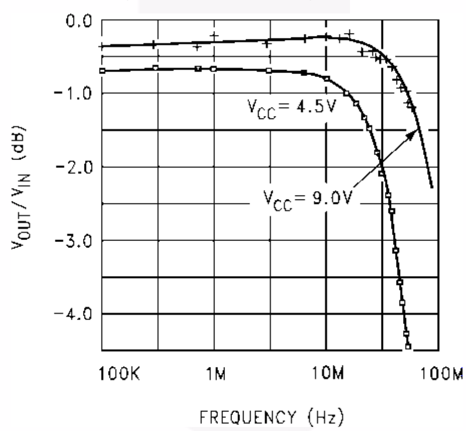
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



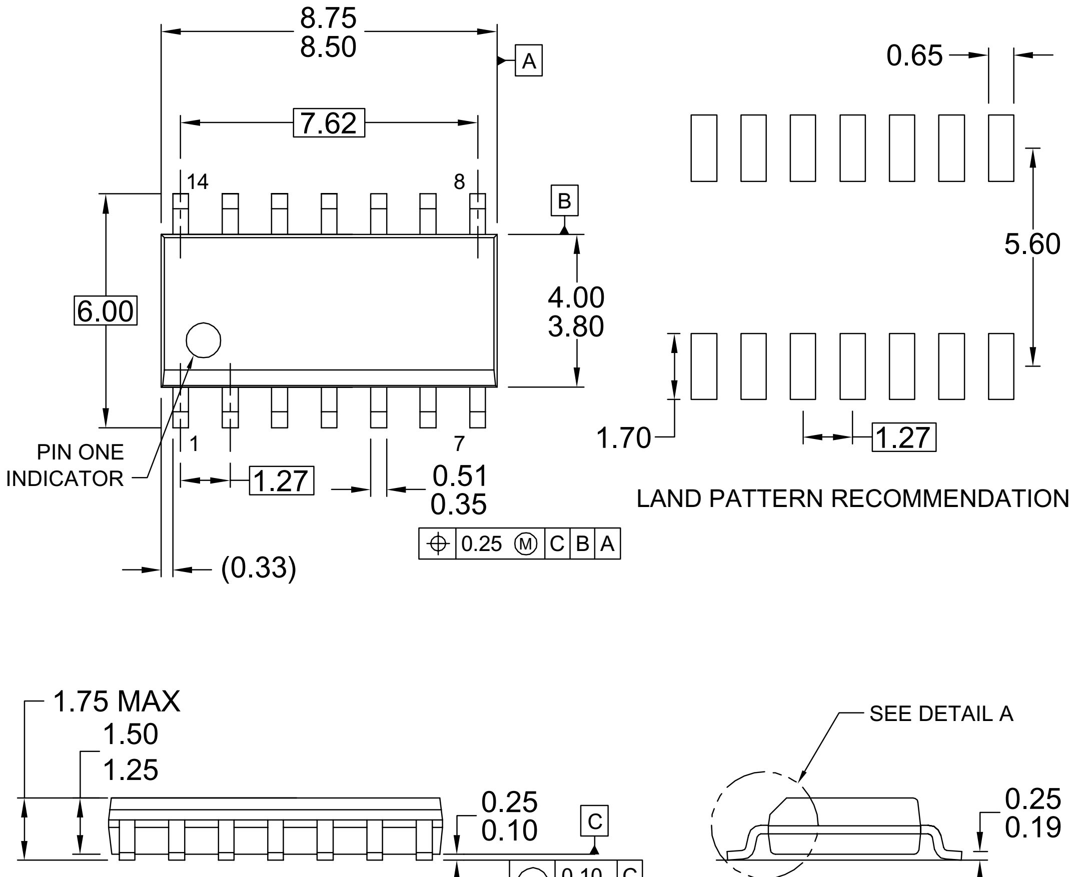
Typical Frequency Response



Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON Resistance).

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

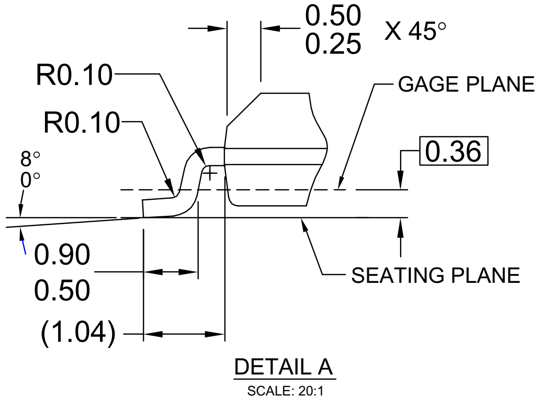


Figure 12. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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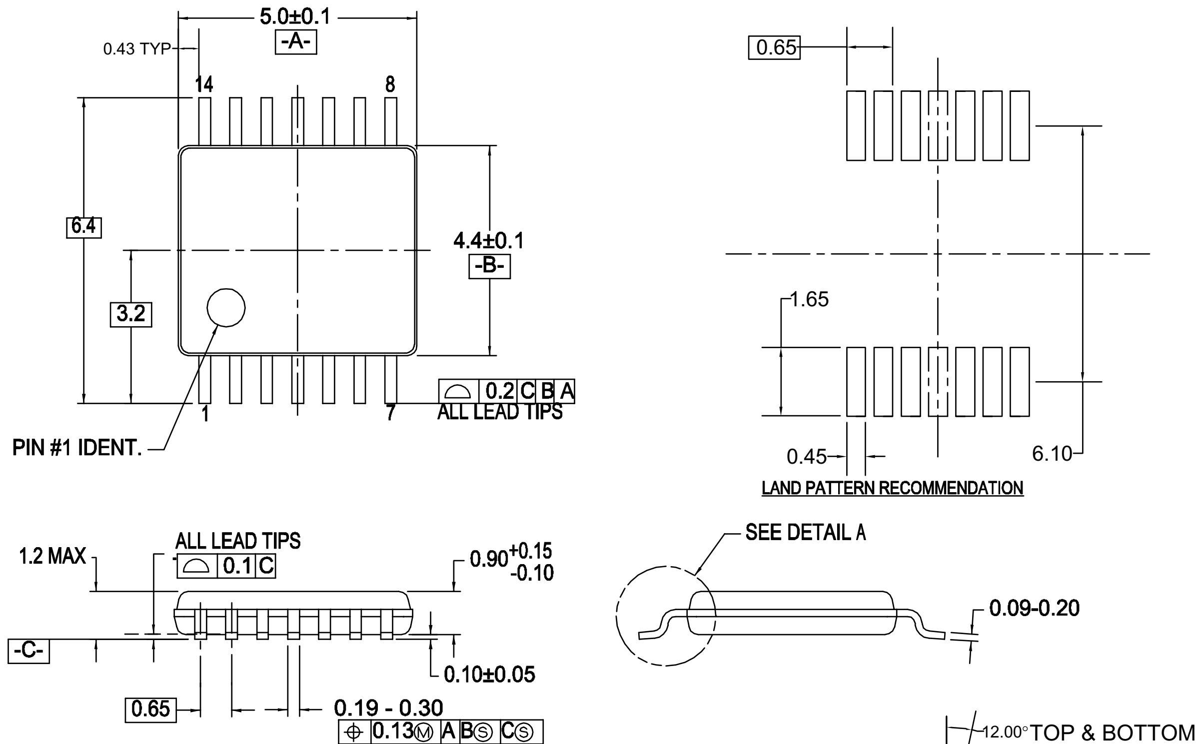

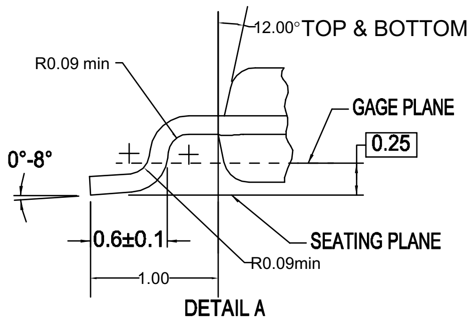

NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

Figure 13. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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