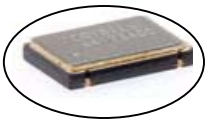
Clock Oscillator

CPLL-018 Model
5x7 mm SMD, **3.3V, CMOS**

RoHS Compliant

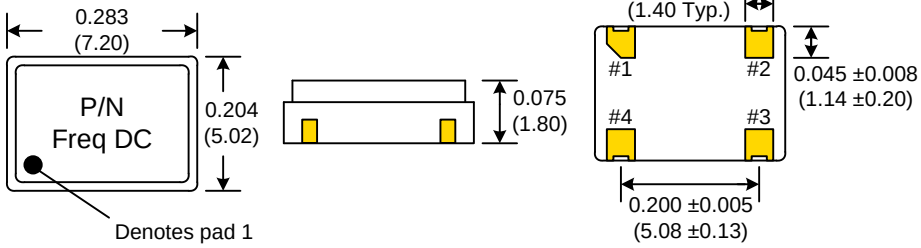


Frequency Range:	1.544MHz to 200MHz
Frequency Stability:	±25ppm, ±50ppm, ±100ppm
Temperature Range:	
Operating:	0°C to 70°C
(Option M)	-20°C to 70°C
(Option X)	-40°C to 85°C
Storage:	-55°C to 120°C
Input Voltage:	3.3V ± 0.3V
Input Current:	45mA Max
Output:	CMOS
Symmetry:	40/60% Max @ 50% Vdd
Rise/Fall Time:	10ns Max @ 20/% to 80% Vdd
Logic:	"0" = 80% Vdd Max
	"1" = 90% Vdd Min
Load:	15pF
Jitter:	150pS pk-pk Max
Aging:	<3ppm 1st/yr, <1ppm every year thereafter

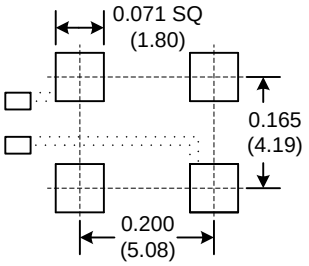
Designed to meet today's requirements for economical 3.3V applications. Available on 16mm tape and reel in quantities of 1K.

Dimensions inches (mm)

All dimensions are Max unless otherwise specified.

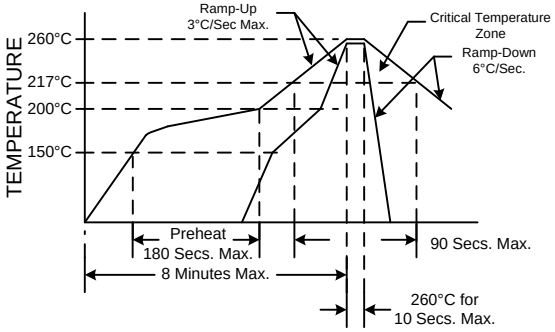


SUGGESTED PAD LAYOUT



0.01uF Bypass Capacitor Recommended

RECOMMENDED REFLOW SOLDERING PROFILE



NOTE: Reflow Profile with 240°C peak also acceptable.

Crystek Part Number Guide

CPLL-018 X - 25 - 200.000
#1 #2 #3 #4 #5

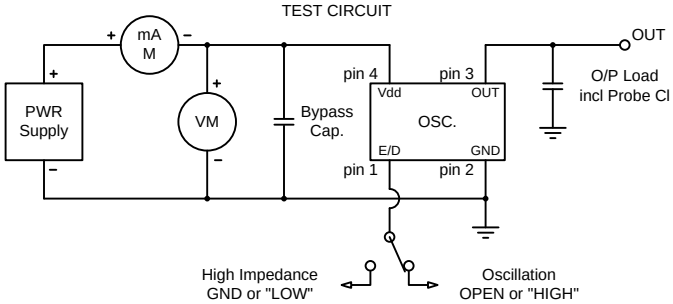
#1 Crystek Clock PLL Osc.
#2 Model
#3 Temp. Range: Blank= 0/70°C, M= -20/70°C, X= -40/85°C
#4 Stability: (see Table 1)
#5 Frequency in MHz: 3 or 6 decimal places

Stability Indicator	
Blank (std)	± 100ppm
50	± 50ppm
25	± 25ppm

Table 1

Example:
CPLL-018X-25-200.000 = 3.3V Tristate, -40/85°C, 25ppm, 200.000 MHz
CPLL-018-50-19.660800 = 3.3V Tristate, 0/70, 50ppm, 19.660800 MHz

TEST CIRCUIT



Tri-State Function	
Function pin 1	Output pin
Open "1" level 2.4V Min "0" level 0.4V Max	Active Active High Z

Specifications subject to change without notice.

TD-040405 Rev.D

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