SM840051

10 Gigabit Ethernet Ultra-Low Jitter Clock Synthesizer

General Description

The SM840051 clock synthesizer was designed for Ethernet standards. The SM840051 is optimized for 77.76, 78.125, 80.56, 155.52, 156.25, and 161.13MHz, using a crystal at 1/8th the output frequency. The SM840051 includes a unique power reduction methodology, along with a patented RotaryWave™ architecture, that provides a stable clock with very low noise for optimized performance. This yields an overall improved Bit Error Rate (BER) and improved waveform integrity.

Power supplies of either 3.3V or 2.5V are supported, with superior jitter and phase noise performance. An FSEL pin supports 4x or 8x multiplication of the crystal frequency.

The SM840051 provides ultra-low jitter, and consumes low power.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

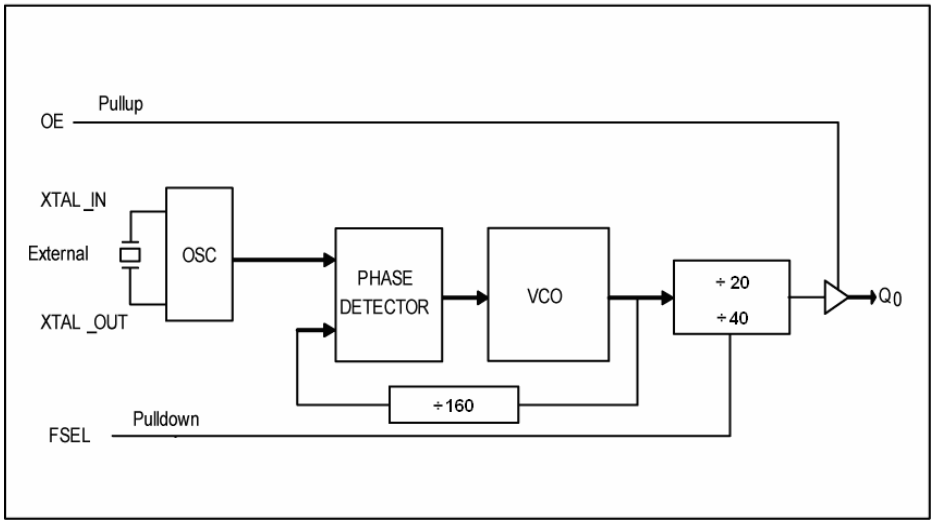
Features

- Generates a single LVCMOS/LVTTL output
- Output Frequencies: 77.76, 78.125, 80.56, 155.52, 156.25, and 161.13MHz
- RMS Phase Jitter at 156.25MHz(1.875MHz-20MHz): 58fs (typical)
- Integrated loop filter components
- Operates with either a 3.3V or 2.5V supply
- Power consumption is <77mA @ 3.3 V
- Fundamental parallel resonant crystal
- Crystal Frequencies: 20.141601MHz,19.53125MHz, and 19.44MHz
- Industrial temperature range: –40°C to +75°C
- Available in 8-pin TSSOP package

Applications

- 10 Gigabit Ethernet
- SONET/SDH

Block Diagram



RotaryWave is a trademark of Multigig, Inc.

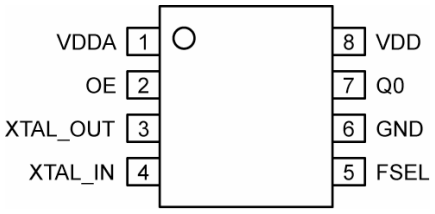
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SM840051KA	K-8	-40°C to +75°C	840051	NiPdAu
SM840051KA TR[2]	K-8	-40°C to +75°C	840051	NiPdAu

Note:

1. Devices are Green, RoHS-compliant and PFOS-compliant.
2. Tape and Reel.

Pin Configuration



8-Pin TSSOP (K-8)

Pin Description

Pin Number	Pin Name	Type	Level	Pin Function
1	VDDA	P		Analog power.
2	OE	I	Pull-up	Output Enable: 1 = Enable, 0 = Disable.
3	XTAL OUT	O		Crystal Output.
4	XTAL IN	I		Crystal Input.
5	FSEL	I	Pull down	Frequency Select Pin.
6	GND	P		Ground.
7	Q0	O		Single Ended LVCMOS Clock Out.
8	VDD	P		Core Power.

Configuring the SM840051 (Frequency Table)

Xtal Frequency (MHz)	FSEL	Output Frequency (MHz)
20.141601	0	161.132812
20.141601	1	80.566406
19.53125	0	156.25
19.53125	1	78.125
19.44	0	155.52
19.44	1	77.76

Output Enable

OE	Output
0	Disable
1	Enable

Absolute Maximum Ratings[1]

Supply Voltage (V_{DD}) ..... +4.6V
Input Voltage (V_{IN}) ..... –0.50V to V_{DD}+0.5V
Output Voltage (V_{OUT}) ..... –0.50V to V_{DD}+0.5V
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +2.375V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +75°C
Junction Thermal Resistance
TSSOP (θ_{JA}) ..... 150°C/W

DC Electrical Characteristics

V_{DD} = 2.5V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		2.375	2.50	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.50	2.625	V
I_{DD}	Core Supply Current	No load		12	20	mA
I_{DDA}	Analog Supply Current			48	55	mA

DC Electrical Characteristics

V_{DD} = 3.3V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DD}	Core Supply Voltage		3.135	3.30	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.30	3.465	V
I_{DD}	Core Supply Current	No load		15	25	mA
I_{DDA}	Analog Supply Current			49	60	mA

LVCMOS Electrical Characteristics

V_{DD} = 2.5V and 3.3V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	V_{DD} = 3.3V ±5%	2		V_{DD} +0.3	V
		V_{DD} = 2.5V ±5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DD} = 3.3V ±5%	-0.30		0.80	V
		V_{DD} = 2.5V ±5%	-0.30		0.70	V
V_{OH}	Output HIGH Voltage	V_{DD} = 3.3V ±5%	2.6			V
		V_{DD} = 2.5V ±5%	1.8			V
V_{OL}	Output LOW Voltage				0.5	V
I_{IH}	Input HIGH Current	Output Enable input			5	µA
I_{IL}	Input LOW Current	Output Enable input	-150			µA
I_{IH}	Input HIGH Current	FSEL input			150	µA
I_{IL}	Input LOW Current	FSEL input	-5			µA

Notes:

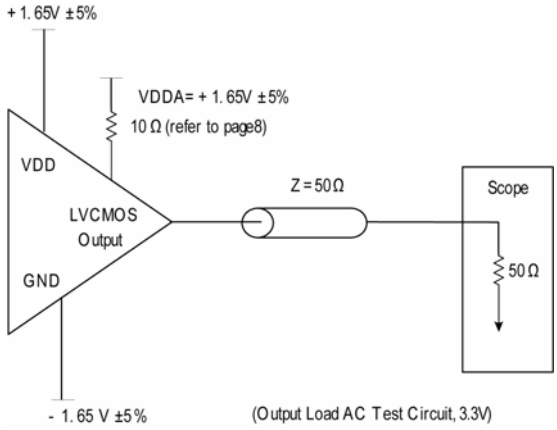
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.

AC Electrical Characteristics

V_{DD} = 2.5V and 3.3V ±5%; T_A = –40°C to +75°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
F_{OUT}	Output frequency		77.76		162.4	MHz
t_{JITTER}	RMS phase jitter @ 156.25MHz	Integration Range: 1.875M to 20MHz		58		fs
t_R / t_F	Output rise/fall time	20% to 80%	100		350	ps
ODC	Output Duty Cycle		48	50	52	%

Test Circuit



(Output Load AC Test Circuit, 3.3V)

3.3V Carrier Frequency, 156.25MHz

Offset from Carrier	Measured Phase Noise	Unit
100Hz	-85	dBc/Hz
1kHz	-122	dBc/Hz
10kHz	-130	dBc/Hz
100kHz	-127	dBc/Hz
1MHz	-140	dBc/Hz
10MHz	-165	dBc/Hz
40MHz	-166	dBc/Hz

Crystal Characteristics[1]

Parameter	Min	Typ	Max	Units
Mode of Oscillation	Fundamental Parallel Resonant			
Frequency	19.44		20.3	MHz
Equivalent Series Resistance (ESR)			50	Ω
Shunt Capacitor			7	pF
Drive Level			1	mW

Note:

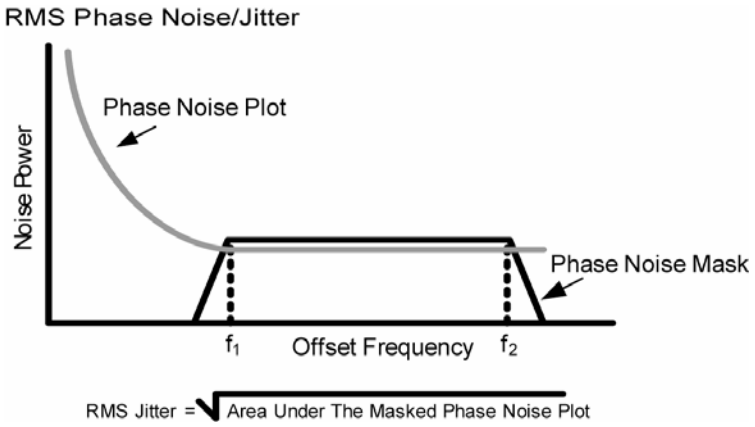
1. Devices are Green, RoHS-compliant and PFOS-compliant

Functional Description

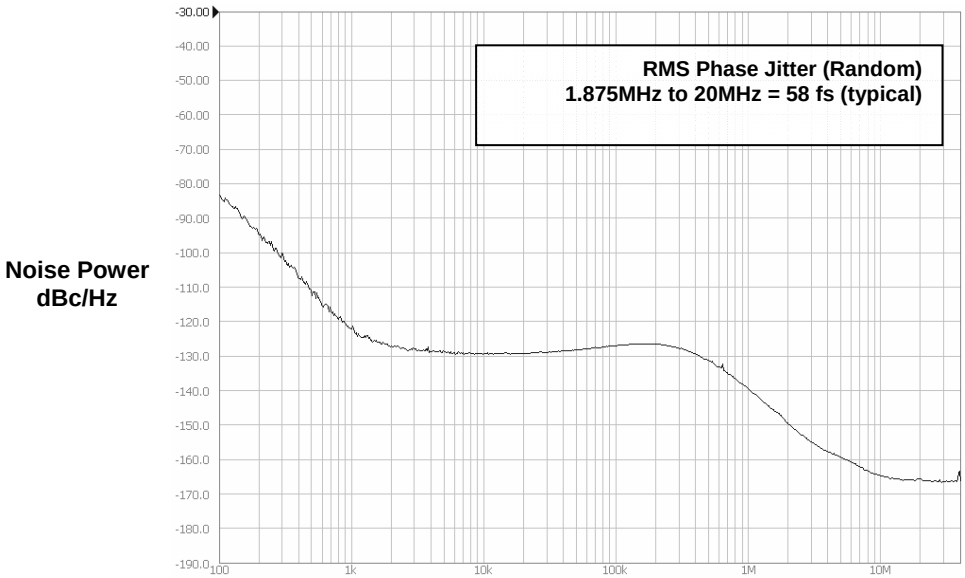
The SM840051 synthesizer provides a high performance solution to frequency generation. Low cost crystals of 20.141601MHz, 19.53125MHz, and 19.44MHz are used to provide low jitter output clocks of 161.132MHz, 156.25MHz , and 155.52MHz, respectively. A single LVCMOS output, capable of driving a 50 ohm load, is provided, which may be tri-stated by the OE input.

The design of the SM840051 consumes very low power in the PLL due to a patented technology in the VCO and the associated dividers. The VCO range is ~3.2GHz to 3.5GHz providing high resolution and easy integer divide ratios. Output Divider ratios are fixed at either ÷20 or ÷40 controlled via the FSEL pin, and the feedback divider also fixed at ÷160. Duty Cycle is inherently improved and guarantees tight control and stability on this critical specification. This provides improved specifications for Duty Cycle, Jitter, Phase Noise, Power Consumption, and noise sensitivity. Additionally, the SM840051 will operate at either 3.3V or 2.5V supplies.

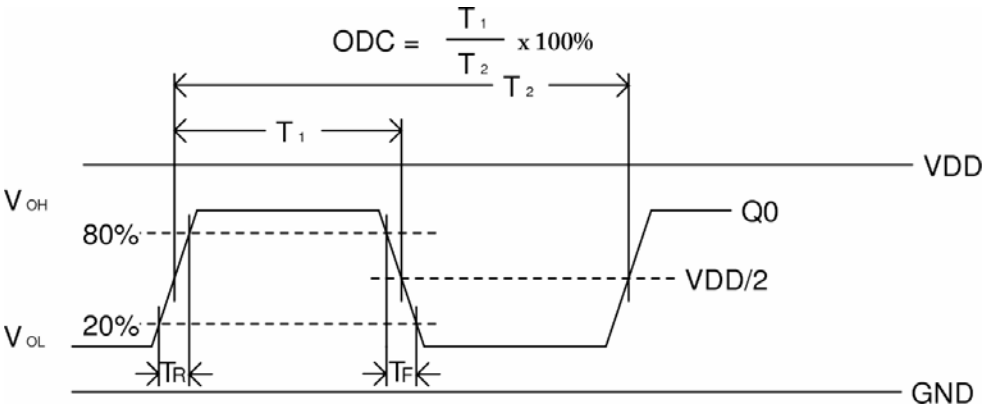
RMS Phase Noise/Jitter



Phase Noise Plot: 156.25MHz @ 3.3V



Switching Waveforms



Power Supply Filtering

The SM840051 provides separate power supply pins to isolate any high switching noise from outputs to internal core blocks. VDD and VDDA should be individually connected to the power plane through vias. Bypass capacitors should be used for each pin. Figure 2, illustrates how the power supply filter for 3.3V and 2.5V is configured.

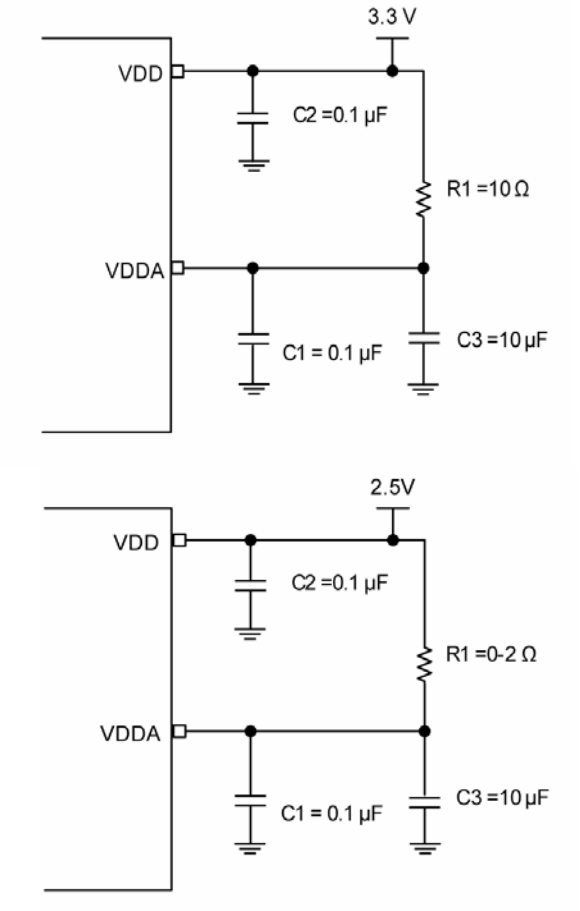
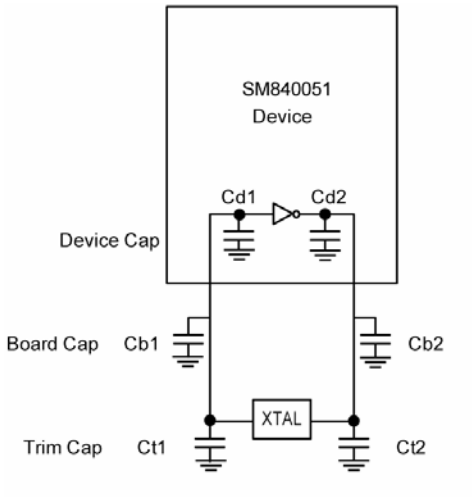


Figure 2. Power Supply Filter

Crystal Loading



Crystal Recommendations

This device requires a parallel resonance crystal. Substituting a series resonance crystal will cause this device to operate at the wrong frequency and violate the ppm specifications.

To achieve low ppm error, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Load Capacitance at each side: Trim Capacitance = Ct = (2*CL-(Cb + Cd))

CL: Crystal load capacitance. Defined by manufacturer

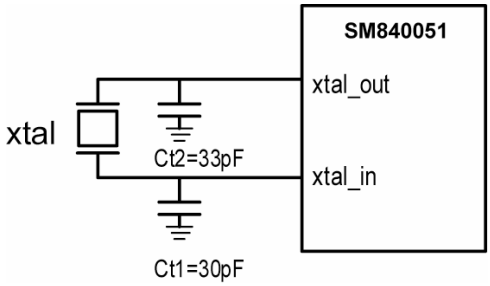
Ct: External trim capacitors. (Trimmed CL Load capacitance to get the right ppm)

Cb: Board capacitance (vias, traces, etc.)

Cd: Internal capacitance of the device (lead frame, bond wires, pin, etc.)

Equivalent Series Resistance (ESR) Max.	Cut	Load Cap.	Shunt Cap. Max.	Drive Max.
50Ω	AT	18pF	7pF	0.1mW

Crystal Input Interface



Total capacitance seen by crystal = CL =

$$\frac{1}{\frac{1}{(Ct1 + Cb1 + Cd1)} + \frac{1}{(Ct2 + Cb2 + Cd2)}}$$

Example:

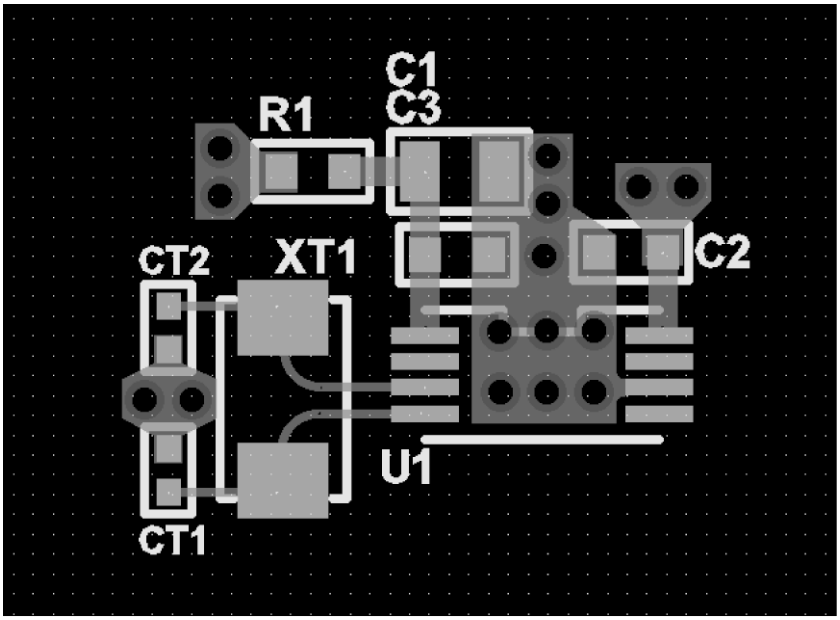
CL = 18pF, Cb = 2pF, Cd = 4pF

Trim Cap = Ct = 2 (18pF) - (2pF +4pF) = 30pF

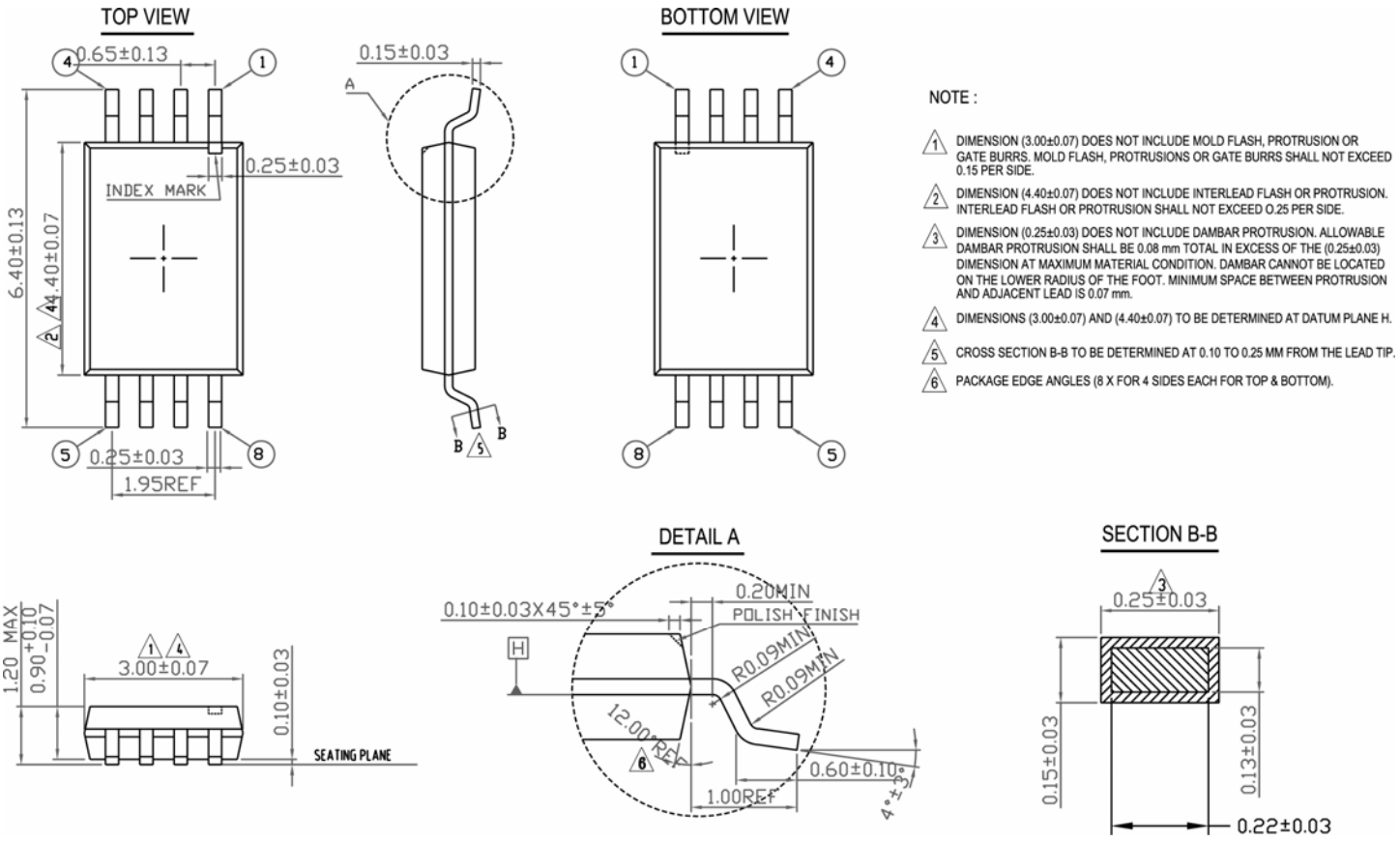
The SM840051 has been characterized with 19.44MHz, 18pF parallel resonant crystal. The trim capacitors Ct1 and Ct2 were optimized to minimize the ppm error.

To minimize the board capacitance, a short trace from pin to crystal footprint without vias is desirable. It is preferable to have ground shielding or distance between the crystal traces and noisy signals on the board.

Board Layout



Package Information



8-Pin TSSOP (K-8)

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