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MOTOROLA

# 2.0GHz Dual Modulus Prescaler

The MC12034A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0 GHz in programmable frequency steps.

The MC12034B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5 V
- MC12034A for Positive Edge Triggered Synthesizers
- 12mA Maximum, –40 to 85°C, $V_{CC}$ = 5.5 Vdc
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low–Power 8.5 mA Typical

## FUNCTIONAL TABLE

| SW | MC | Divide Ratio |
|---|---|---|
| H | H | 32 |
| H | L | 33 |
| L | H | 64 |
| L | L | 65 |

**NOTES:** 1. SW: H = $V_{CC}$, L = Open. A logic L can also be applied by grounding this pin, but this is not recommended due to increased power consumption.
2. MC: H = 2.0 V to $V_{CC}$, L = GND to 0.8 V.

| Design Criteria | Value | Unit |
|---|---|---|
| Internal Gate Count * | 67 | ea |
| Internal Gate Propagation Delay | 200 | ps |
| Internal Gate Power Dissipation | 0.75 | mW |
| Speed Power Product | 0.15 | pJ |

**NOTE:** *Equivalent to a two–input NAND gate.

## MAXIMUM RATINGS

| Characteristic | Symbol | Range | Unit |
|---|---|---|---|
| Power Supply Voltage, Pin 2 | $V_{CC}$ | –0.5 to +7.0 | Vdc |
| Operating Temperature Range | $T_A$ | –40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Modulus Control Input, Pin 6 | MC | –0.5 to +6.5 | Vdc |

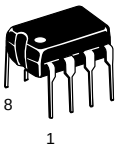
**NOTES:** 1. ESD data available upon request.
2. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

# MC12034A
# MC12034B

## MECL PLL COMPONENTS
## ÷32/33, ÷64/65
## DUAL MODULUS PRESCALER

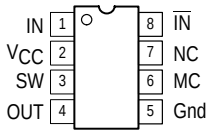
**SEMICONDUCTOR TECHNICAL DATA**

**D SUFFIX**
PLASTIC PACKAGE
CASE 751
(SO–8)




**P SUFFIX**
PLASTIC PACKAGE
CASE 626

## PIN CONNECTIONS




(Top View)

## ORDERING INFORMATION

| Device | Operating Temp Range | Package |
|---|---|---|
| MC12034AD | $T_A$ = –40° to +85°C | SO–8 |
| MC12034AP | | Plastic |
| MC12034BD | | SO–8 |
| MC120348BP | | Plastic |

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Rev 3

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**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 4.5 to 5.5 Vdc, $T_A$ = –40 to 85°C, unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Toggle Frequency (Sine Wave) | $f_t$ | 0.5 | 2.4 | 2.0 | GHz |
| Supply Current Output Unloaded (Pin 2) | $I_{CC}$ | – | 8.5 | 12 | mA |
| Modulus Control Input High (MC) | $V_{IH1}$ | 2.0 | – | $V_{CC}$ | V |
| Modulus Control Input Low (MC) | $V_{IL1}$ | – | – | 0.8 | V |
| Divide Ratio Control Input High (SW) | $V_{IH2}$ | $V_{CC}$ | $V_{CC}$ | $V_{CC}$ | Vdc |
| Divide Ratio Control Input Low (SW) | $V_{IL2}$ | OPEN | OPEN | OPEN | – |
| Output Voltage Swing ($C_L$ = 12 pF, $R_L$ = 1.1 kΩ) | $V_{out}$ | 1.0 | 1.6 | – | $V_{pp}$ |
| Modulus Setup Time MC to Out | $t_{SET}$ | – | 8.0 | 10.0 | ns |
| Input Voltage Sensitivity 500–2000 MHz | $V_{in}$ | 100 | – | 1500 | mVpp |
| Output Current ($C_L$ = 12 pF, $R_L$ = 1.1 kΩ) | $I_O$ | – | – | 3.5 | mA |

**Figure 1. Logic Diagram (MC12034A)**

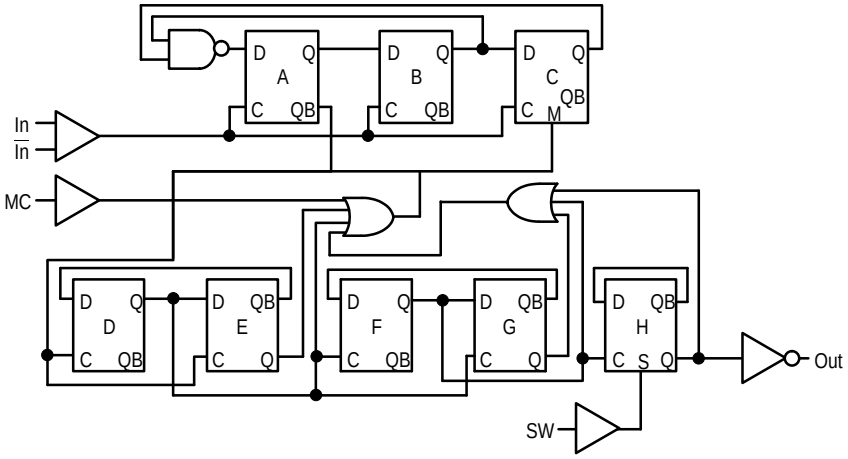
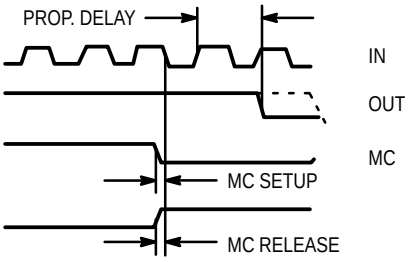



**Figure 2. Modulus Setup Time**




Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

**Figure 3. Typical Output Waveform**

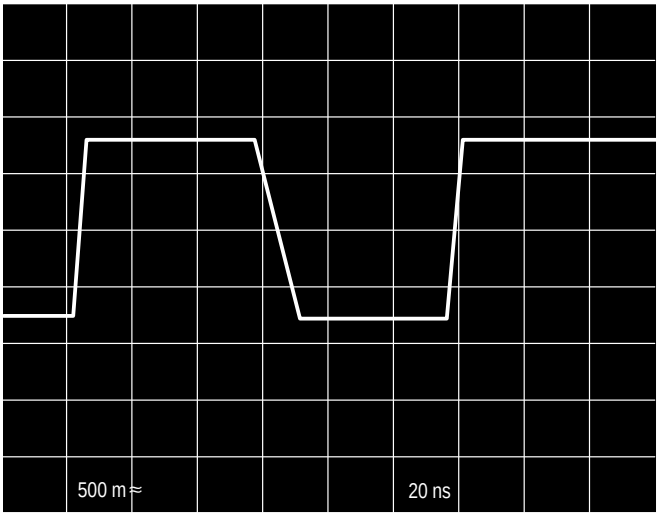





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**Figure 4. AC Test Circuit**

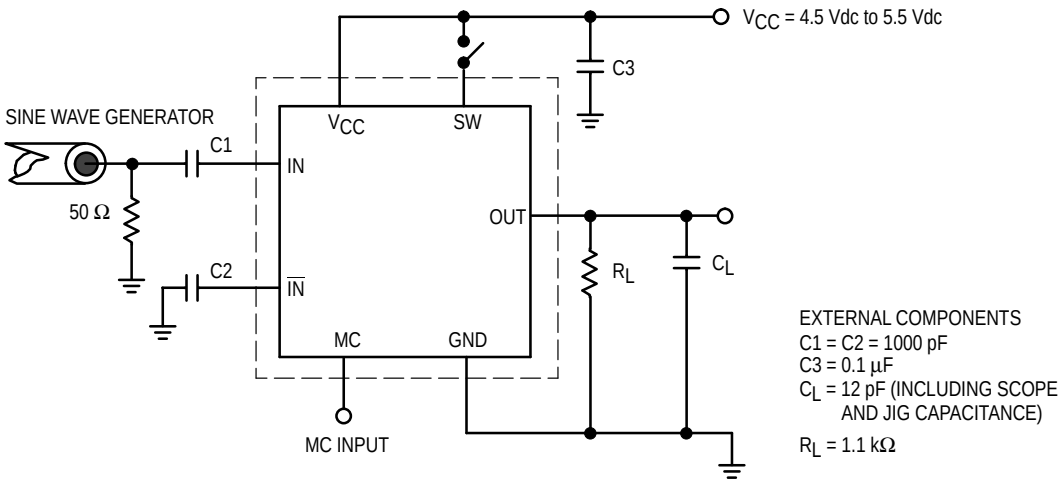



**Figure 5. Input Signal Amplitude versus Input Frequency**

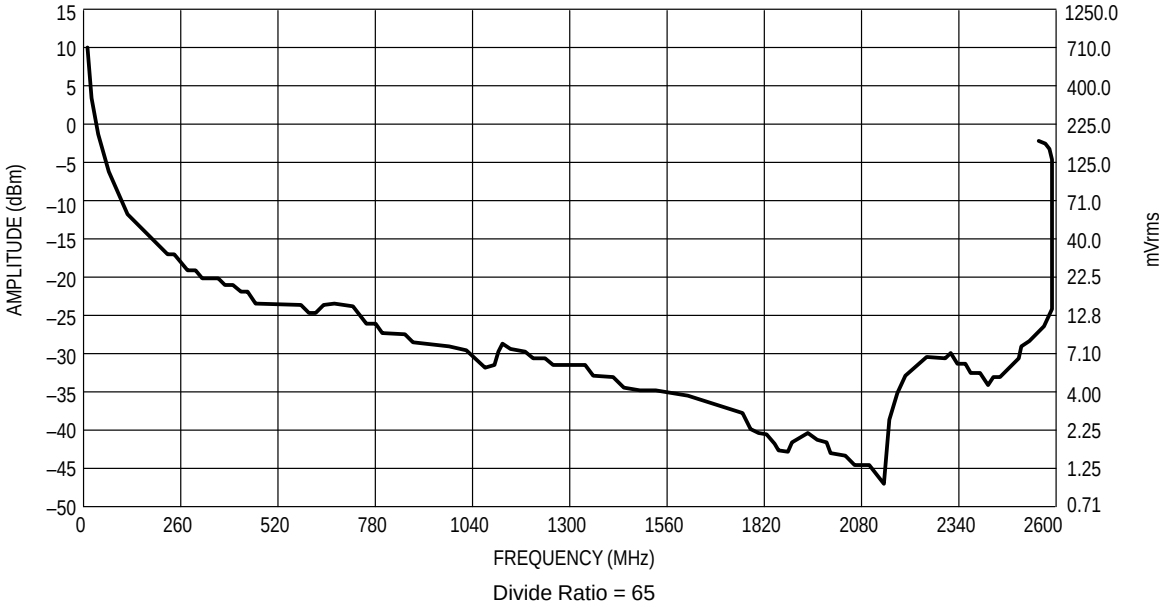
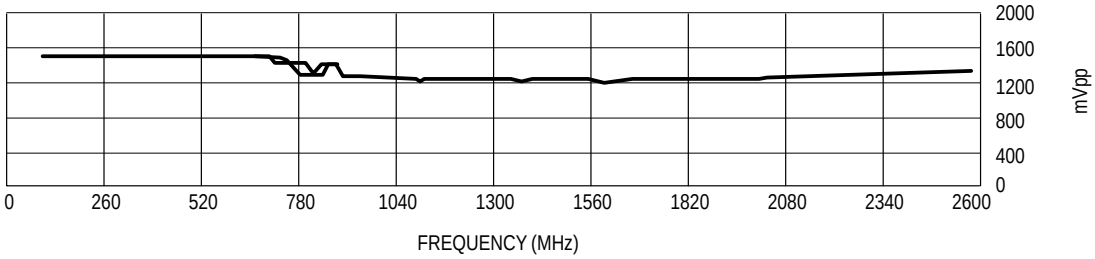



**Figure 6. Output Amplitude versus Input Frequency**



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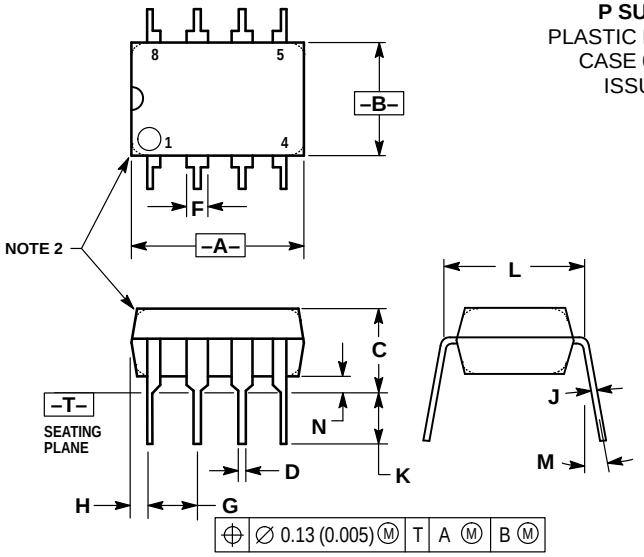
## OUTLINE DIMENSIONS

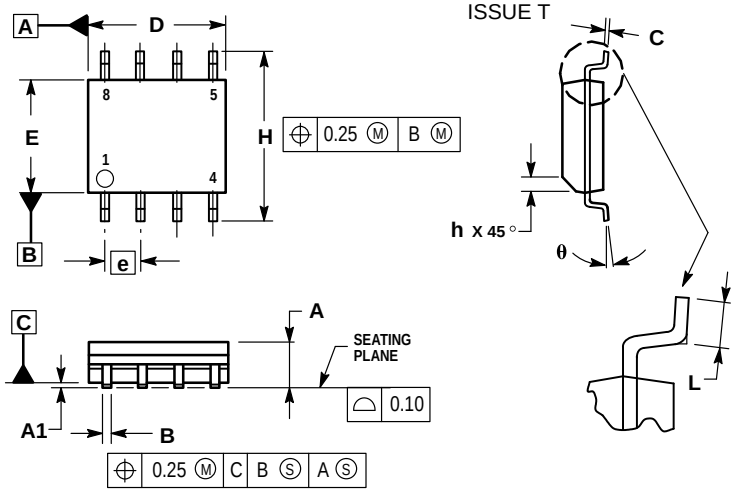
**P SUFFIX**
PLASTIC PACKAGE
CASE 626–05
ISSUE K




NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | — | 10° | — | 10° |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

**D SUFFIX**
PLASTIC PACKAGE
CASE 751–06
(SO–8)
ISSUE T




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

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