

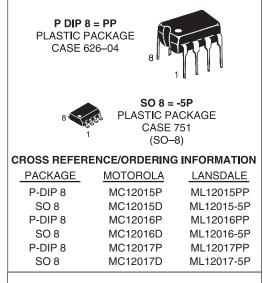
# ML12015 ML12016 ML12017 Dual Modulus Prescaler

## MECL PLL COMPONENTS SEMICONDUCTOR TECHNICAL DATA

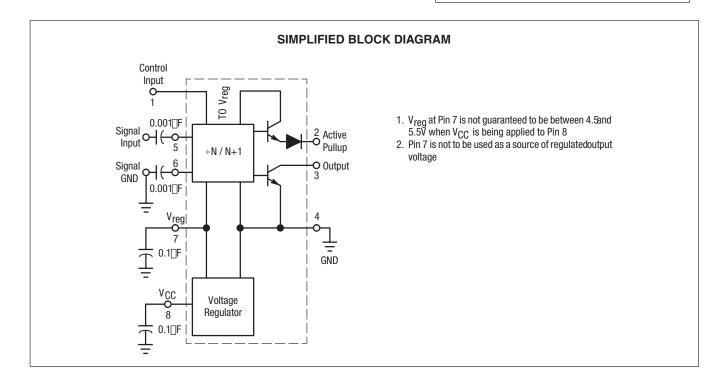
Legacy Device: Motorola MC12015, MC12016, MC12017

The ML12015, ML12016 and ML12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power–supply voltages. The devices may be operated by applying a supply voltage of 5.0 Vdc  $\pm 10\%$  at Pin 7, or by applying an unregulated voltage source from 5.5 Vdc to 9.5 Vdc to Pin 8.

- 225 MHz Toggle Frequency
- Low–Power 7.5 mA Maximum at 6.8 V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V
- Operating Temperature Range  $T_A = -40$  to  $85^{\circ}C$



**Note:** Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.



#### MAXIMUM RATINGS

Rating	Symbol Value		Unit
Regulated Voltage, Pin 7	V <sub>reg</sub>	8.0	Vdc
Power Supply Voltage, Pin 8	V <sub>CC</sub>	10	Vdc
Operating Temperature Range	TA	-40 to +85	]C
Storage Temperature Range	T <sub>stg</sub>	-65 to +175	_C

### **ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5.5 to 9.5 V; V<sub>reg</sub> = 4.5 to 5.5 V; T<sub>A</sub> = -40 to 85[C, unless otherwise noted.)

Characteristic	Symbol	Min	Тур	Мах	Unit
Toggle Frequency (Sine Wave Input)					MHz
	fmax	225	-	-	
	fmin	-	-	35	
Supply Current	ICC	-	6.0	7.8	mA
Control Input HIGH (∐32, 40 or 64)	VIH	2.0	-	-	V
Control Input LOW ([]33, 41 or 65)	VIL	-	-	0.8	V
Output Voltage HIGH (I <sub>SOURCE</sub> = 50[]A) [Nofe 1]	VOH	2.5	-	-	V
Output Voltage LOW (I <sub>sink</sub> = 2mA) [Note 1]	V <sub>OL</sub>	-	-	0.5	V
Input Voltage Sensitivity	V <sub>in</sub>				mVpp
35 MHz		400	-	800	
50 to 225 MHz		200	-	800	
PLL Response Time [Notes 2 and 3]	<sup>t</sup> PLL	-	-	t <sub>out</sub> to 70	ns

NOTES: 1. Pin 2 connected to Pin 3.
2. tp<sub>LL</sub> = the period of time the PLL has from the prescaler rising output tranistion (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection.
3. t<sub>out</sub> = period of output waveform.

Figure 1. Generic block diagram showing prescaler connection to PLL device

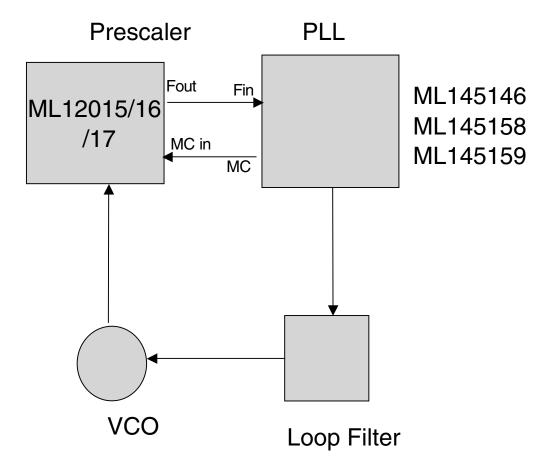
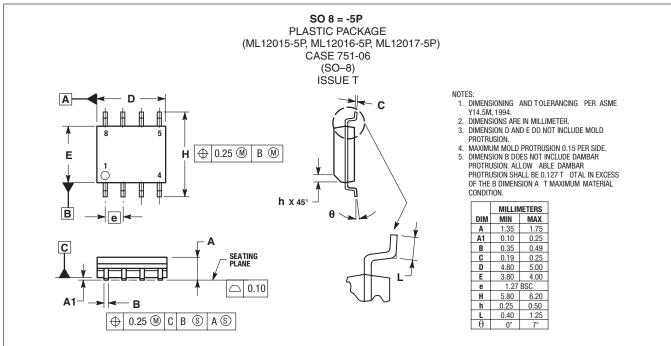
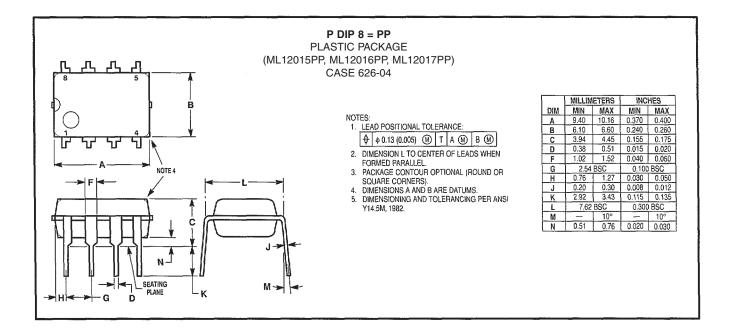


Figure 1. shows a generic block diagram for connecting a prescaler to a PLL device that supports dual modulus control. Application note AN535 decribes using a two-modulus prescaler technique.By using prescaler higher frequencies can be achieve than by a single CMOS PLL device.

#### **OUTLINE DIMENSIONS**





Lansdale Semiconductor reserves the right to make changes without further notice to any products herein to improve reliability, function or design. Lansdale does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights nor the rights of others. "Typical" parameters which may be provided in Lansdale data sheets and/or specifications can vary in different applications, and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by the customer's technical experts. Lansdale Semiconductor is a registered trademark of Lansdale Semiconductor, Inc.

Downloaded from Elcodis.com electronic components distributor

www.lansdale.com