

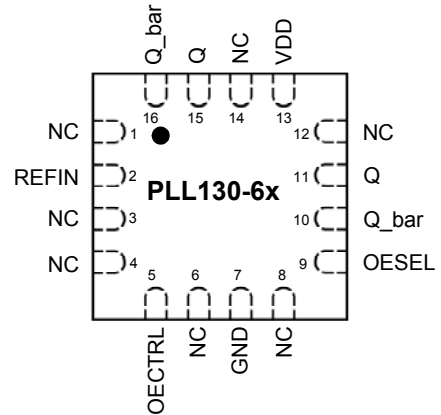
High Speed Translator Buffers: Single ended to PECL or LVDS

FEATURES

- Differential PECL (PLL130-68) or LVDS (PLL130-69) output.
- Accepts any single-ended REFIN input (with as low as 100mV swing).
- Internal AC coupling of REFIN
- Input range from 1.0MHz to 1.0 GHz.
- No Vref required.
- No external current source required.
- 2.5 to 3.3V operation.
- Available in 3x3mm QFN.

PIN CONFIGURATION

(TOP VIEW)



DESCRIPTION

The PLL130-68 and PLL130-69 are low cost, high performance, high speed, translator buffers that reproduce any input frequency from DC to 1.0GHz. They provide a pair of differential outputs (PECL for PLL130-68 or LVDS for PLL130-69). Thanks to an internal AC coupling of the reference input (REFIN), any input signal with at least 100mV swing can be used as reference signal, regardless of its DC value. These chips are ideal for conversion from clipped sine wave, TTL, CMOS, or differential signal to LVDS or PECL.

OUTPUT ENABLE LOGICAL LEVELS

PLL130-68

| OESEL | OECTRL | OUTPUT STATE |
|-------------|-------------|----------------|
| 0 (Default) | 0 (Default) | Output enabled |
| | 1 | Tri-state |
| 1 | 0 | Tri-state |
| | 1 (Default) | Output enabled |

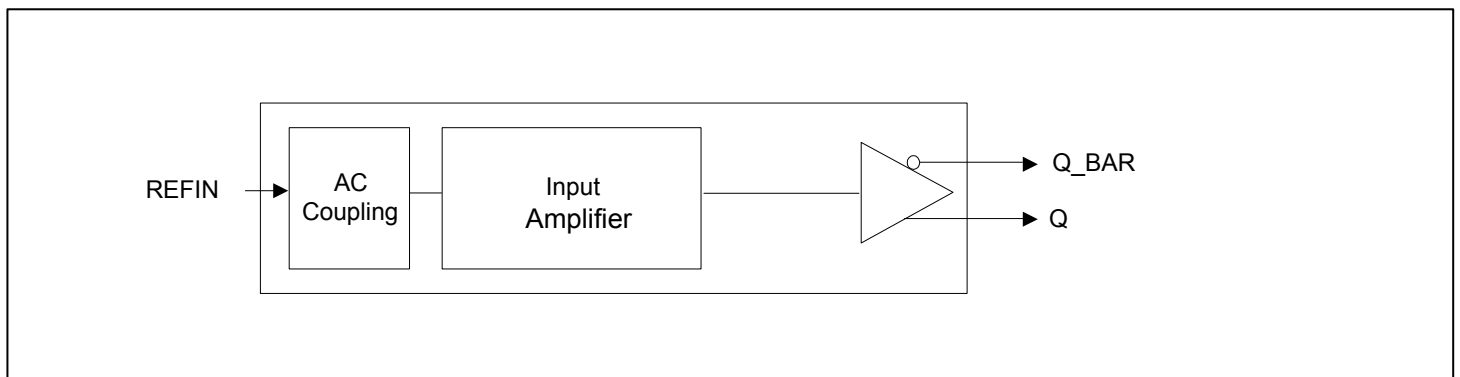
OECTRL input: Logical states defined by PECL levels.

PLL130-69

| OESEL | OECTRL | OUTPUT STATE |
|-------------|-------------|----------------|
| 0 (Default) | 0 | Tri-state |
| | 1 (Default) | Output enabled |
| 1 | 0 (Default) | Output enabled |
| | 1 | Tri-state |

OECTRL input: Logical states defined by CMOS levels.

BLOCK DIAGRAM



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PIN DESCRIPTION

| Name | Pin number | Type | Description |
|--------|-----------------------|------|--|
| NC | 1, 3, 4, 6, 8, 12, 14 | - | No connection. |
| REFIN | 2 | I | Reference input signal. The frequency of this signal will be reproduced at the output (after translation to PECL or LVDS level). |
| OCTRL | 5 | I | Output enable input (See OE Logic Table on page 1). |
| GND | 7 | P | Ground connector. |
| OESSEL | 9 | I | Output enable logic selector (See OE Logic Table on page 1). |
| Q_BAR | 10 | O | Complementary output. PECL_bar on PLL130-68, LVDS_bar on PLL130-69. |
| Q | 11 | O | True output. PECL on PLL130-68, LVDS on PLL130-69. |
| VDD | 13 | P | 3.3V Power supply. |
| Q | 15 | O | Additional true output. PECL on PLL130-68, LVDS on PLL130-69. This output is the same as pin 11. |
| Q_BAR | 16 | O | Additional complementary output. PECL_bar on PLL130-68, LVDS_bar on PLL130-69. This output is the same as pin 10. |

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

| PARAMETERS | SYMBOL | MIN. | MAX. | UNITS |
|-----------------------------------|-----------------|------|----------------------|-------|
| Supply Voltage | V _{DD} | | 4.6 | V |
| Input Voltage, dc | V _I | -0.5 | V _{DD} +0.5 | V |
| Output Voltage, dc | V _O | -0.5 | V _{DD} +0.5 | V |
| Storage Temperature | T _S | -65 | 150 | °C |
| Ambient Operating Temperature* | T _A | -40 | 85 | °C |
| Junction Temperature | T _J | | 125 | °C |
| Lead Temperature (soldering, 10s) | | | 260 | °C |
| ESD Protection, Human Body Model | | | 2 | kV |

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. General Electrical Specifications

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--------------------------------------|-----------------|------------------------|---------------|------|------|-------|
| Supply Current (both outputs loaded) | I _{DD} | Fout = 156.25MHz, PECL | 45 | 48 | 51 | mA |
| | | Fout = 156.25MHz, LVDS | 22 | 25 | 28 | |
| Operating Voltage | V _{DD} | | 2.97 | | 3.63 | V |
| Output Clock Duty Cycle | | @ Vdd – 1.3V (PECL) | Same as input | | | % |
| | | @ 1.25V (LVDS) | Same as input | | | |
| Short Circuit Current | | | | ±50 | | mA |

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3. AC Specifications

| PARAMETERS | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--------------------|-------------|------|------|------|-------|
| Input Frequency | | 0 | | 1000 | MHz |
| Input signal swing | REFIN input | 100 | | | mV |
| Output Frequency | | 0 | | 1000 | MHz |

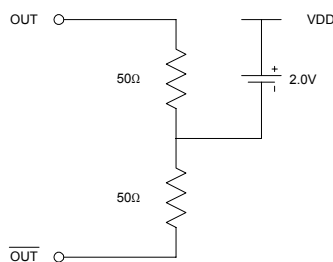
4. PECL Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | MAX. | UNITS |
|---------------------|----------|--|------------------|------------------|-------|
| Output High Voltage | V_{OH} | $R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure) | $V_{DD} - 1.025$ | $V_{DD} - 0.880$ | V |
| Output Low Voltage | V_{OL} | | $V_{DD} - 1.810$ | $V_{DD} - 1.620$ | V |

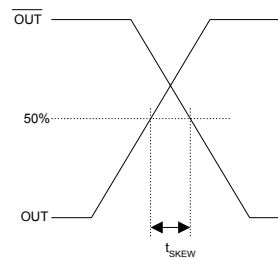
5. PECL Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------|--------|----------------|------|------|------|-------|
| Clock Rise Time | t_r | @20/80% - PECL | | 0.2 | 0.5 | ns |
| Clock Fall Time | t_f | @80/20% - PECL | | 0.2 | 0.5 | ns |

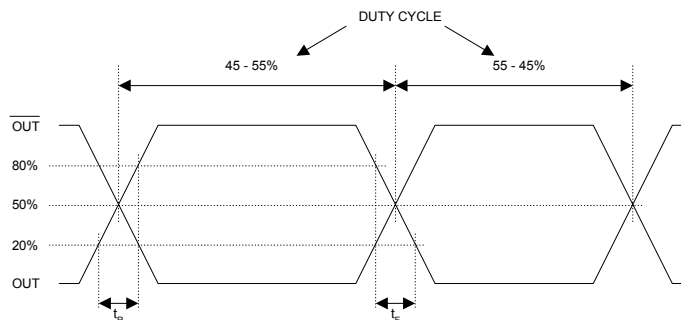
PECL Levels Test Circuit



PECL Output Skew



PECL Transition Time Waveform



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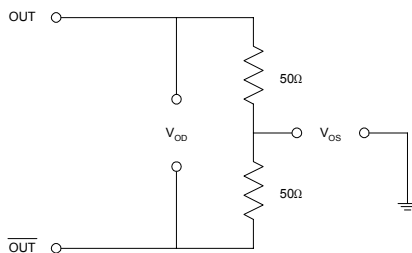
6. LVDS Electrical Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|-----------------|--|-------|---------|----------|---------|
| Output Differential Voltage | V_{OD} | $R_L = 100 \Omega$ (see figure) | 247 | 355 | 454 | mV |
| V_{DD} Magnitude Change | ΔV_{OD} | | -50 | | 50 | mV |
| Output High Voltage | V_{OH} | | 1.4 | 1.6 | V | |
| Output Low Voltage | V_{OL} | | 0.9 | 1.1 | V | |
| Offset Voltage | V_{OS} | | 1.125 | 1.2 | 1.375 | V |
| Offset Magnitude Change | ΔV_{OS} | | 0 | 3 | 25 | mV |
| Power-off Leakage | I_{OXD} | $V_{out} = V_{DD}$ or GND $V_{DD} = 0V$ | | ± 1 | ± 10 | μA |
| Output Short Circuit Current | I_{OSD} | | | -5.7 | -8 | mA |

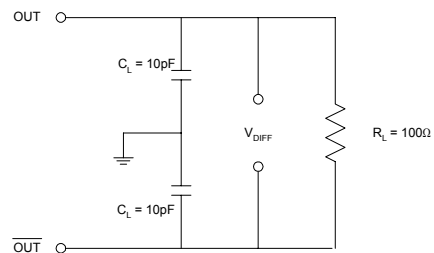
7. LVDS Switching Characteristics

| PARAMETERS | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------|---|------|------|------|-------|
| Differential Clock Rise Time | t_r | $R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure) | 0.2 | 0.5 | 1.0 | ns |
| Differential Clock Fall Time | t_f | | 0.2 | 0.5 | 1.0 | ns |

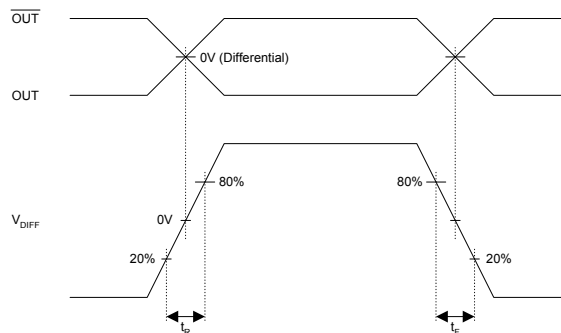
LVDS Levels Test Circuit



LVDS Switching Test Circuit

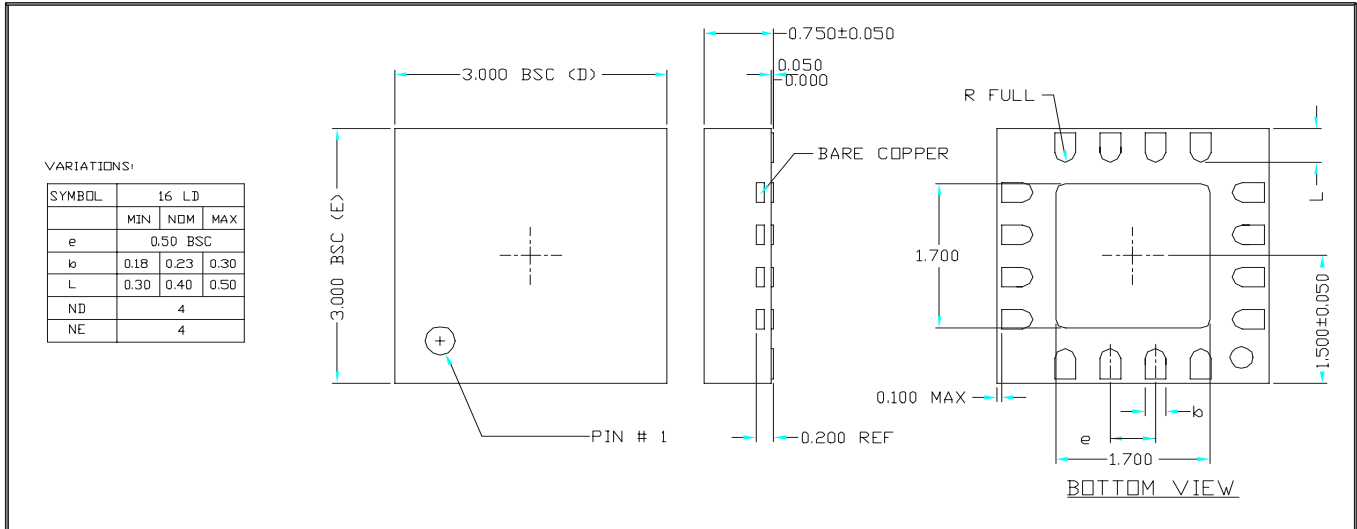


LVDS Transition Time Waveform



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PACKAGE INFORMATION



Important note: pin 1 indicator (bottom side) is metallized and connected to GND through the leadframe. Traces in contact with the pin 1 indicator may result in short circuit to GND.

ORDERING INFORMATION

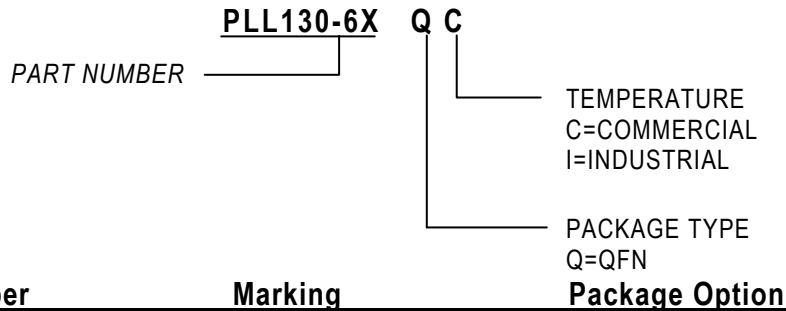
For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA

Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



| Order Number | Marking | Package Option |
|---------------|---------|---------------------|
| PLL130-68QC-R | P130-68 | QFN - Tape and Reel |
| PLL130-68QC | P130-68 | QFN - Tube |
| PLL130-69QC-R | P130-69 | QFN - Tape and Reel |
| PLL130-69QC | P130-69 | QFN - Tube |

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