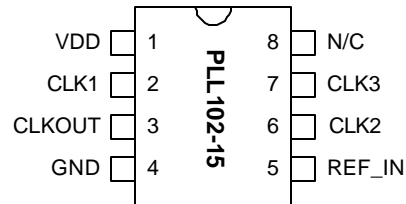


**FEATURES**

- Frequency range 25 ~ 60MHz.
- Internal phase locked loop will allow spread spectrum modulation on reference clock to pass to the outputs (up to 33kHz SST modulation).
- Zero input - output delay.
- Less than 700 ps device - device skew.
- Less than 250 ps skew between outputs.
- Less than 200 ps cycle - cycle jitter.
- Output Enable function tri-state outputs.
- 3.3V operation.
- Available in 8 -Pin 150mil SOIC.

**PIN CONFIGURATION**



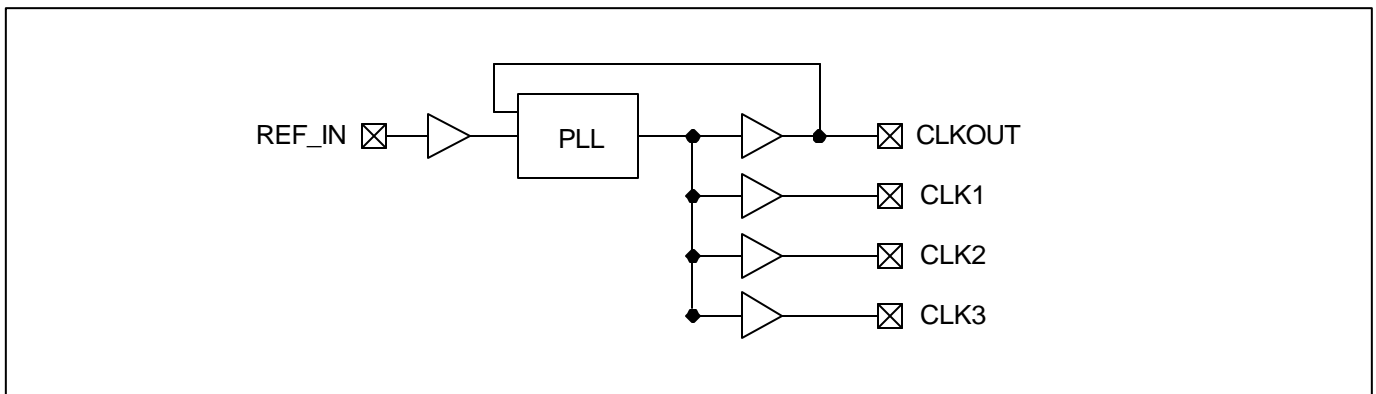
**Remark**

If REF\_IN clock is stopped for more than 10us after it has already been provided to the chip, and after power-up, the output clocks will disappear. In that instance, a full power-up reset is required in order to reactivate the output clocks.

**DESCRIPTIONS**

The PLL102-15 is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks and is available in 8-pin SOIC or TSSOP package. It has four outputs that are synchronized with the input. The synchronization is established via CLKOUT feedback to the input of the PLL. Since the skew between the input and output is less than  $\pm 350$  ps, the device acts as a zero delay buffer.

**BLOCK DIAGRAM**



### PIN DESCRIPTIONS

Name	Number	Type	Description
VDD	1	P	3.3V Power Supply.
CLK1 <sup>3</sup>	2	O	Buffered clock output.
CLKOUT <sup>3</sup>	3	O	Buffered clock output. Internal feed back on this pin.
GND	4	P	Ground.
REF_IN <sup>2</sup>	5	I	Input reference frequency. Spread spectrum modulation on this signal will be passed to the output (up to 33kHz SST modulation).
CLK2 <sup>3</sup>	6	O	Buffered clock output.
CLK3 <sup>3</sup>	7	O	Buffered clock output.
NC	8	-	No connection.

Notes: 2: Weak pull-down. 3: Weak pull-down on all outputs.

### ELECTRICAL SPECIFICATIONS

#### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V <sub>CC</sub>	-0.5	7	V
Input Voltage Range	V <sub>I</sub>	-0.5	V <sub>CC</sub> +0.5	V
Output Voltage Range	V <sub>O</sub>	-0.5	V <sub>CC</sub> +0.5	V
Soldering Temperature			260	°C
Storage Temperature	T <sub>S</sub>	-65	150	°C
Ambient Operating Temperature		0	70	°C
ESD Voltage			2	KV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

#### 2. Electrical Characteristics

V<sub>DD</sub> = 3.0~3.6V, unless otherwise stated

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V <sub>DD</sub>		2.97		3.63	V
Input Low Voltage	V <sub>IL</sub>				0.8	V
Input High Voltage	V <sub>IH</sub>		2.0			V
Input Low Current	I <sub>IL</sub>	V <sub>IN</sub> = 0V		19	50.0	μA
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>		0.10	100.0	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 50mA		0.25	0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = 50mA	2.4	2.9		V
Power Down Supply Current	I <sub>DD</sub>	REF = 0MHz		0.3	50.0	μA
Supply Current	I <sub>DD</sub>	Unloaded outputs at 60MHz, SEL inputs at V <sub>DD</sub> or GND		30.0	40.0	mA

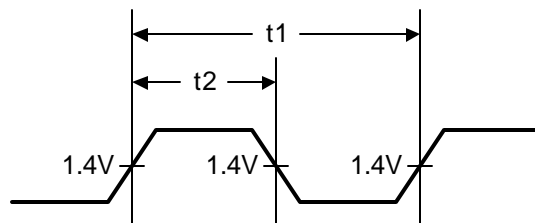
**Low Skew Output Buffer**

**3. Switching Characteristics**

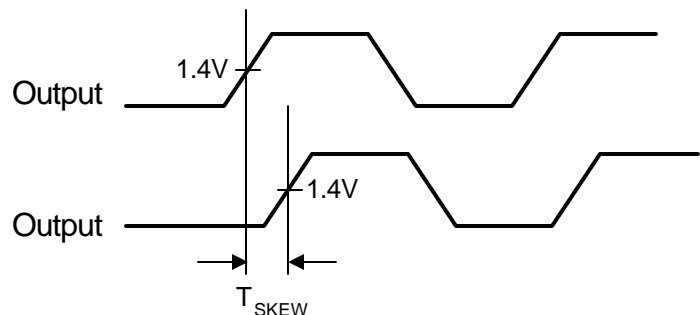
PARAMETERS	SYMBOL	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Output Frequency	$t_1$		25		60	MHz
Duty Cycle ( $t_2 \div t_1$ )	Dt1	Measured at 1.4V, $C_L=30pF$ , $F_{out} = 60MHz$	40.0	50.0	60.0	%
Duty Cycle ( $t_2 \div t_1$ )	Dt2	Measured at 1.4V	45.0	50.0	55.0	%
Rise Time	$T_r$	Measured between 0.8V and 2.0V, $C_L=30pF$		1.2	1.5	ns
Fall Time	$T_f$	Measured between 2.0V and 0.8V, $C_L=30pF$		1.2	1.5	ns
Output to Output Skew	$T_{skew}$	All outputs equally loaded, $C_L=20pF$			250	ps
Delay, REF Rising Edge to CLKOUT Rising Edge	$T_{delay}$	Measured at 1.4V		0	$\pm 350$	ps
Device to Device Skew	$T_{dsk-dsk}$	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
Cycle to Cycle Jitter	$T_{cyc-cyc}$	Loaded outputs			200	ps
PLL Lock Time	$T_{lock}$	Stable power supply, valid clock presented on REF pin			1.0	ms
Jitter; Absolute Jitter	$T_{jabs}$	At 10,000 cycles, $C_L=30pF$	-100	70	100	ps
Jitter; 1-sigma	$T_{j1-s}$	At 10,000 cycles, $C_L=30pF$		14	30	ps

**SWITCHING WAVEFORMS**

**Duty Cycle Timing**

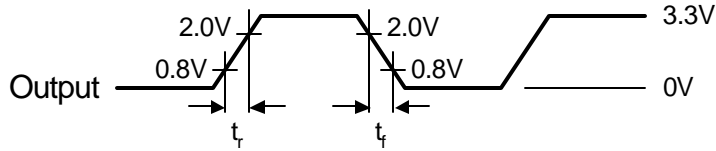


**Output - Output Skew**

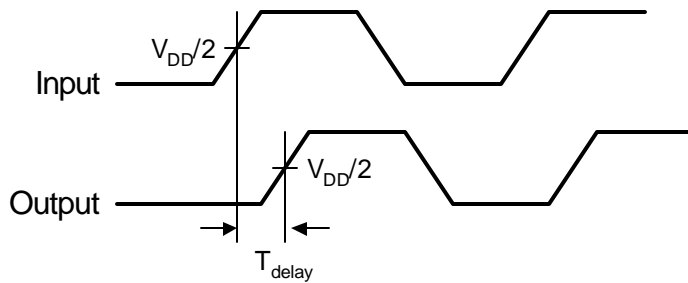


**SWITCHING WAVE FORMS**

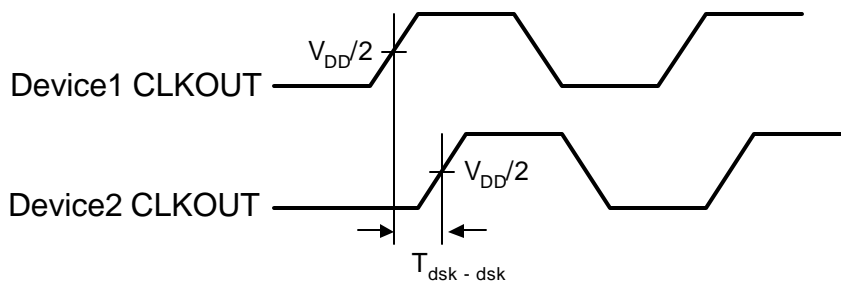
All Outputs Rise/Fall Time



Input to Output Propagation Delay



Device to Device Skew



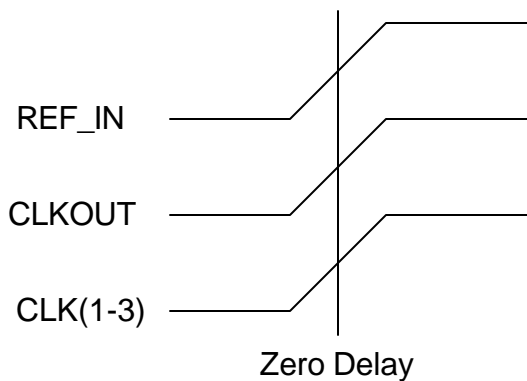
**Output-Output Skew**

The skew between CLKOUT and the CLK(1-3) outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF\_IN to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF\_IN to all outputs.

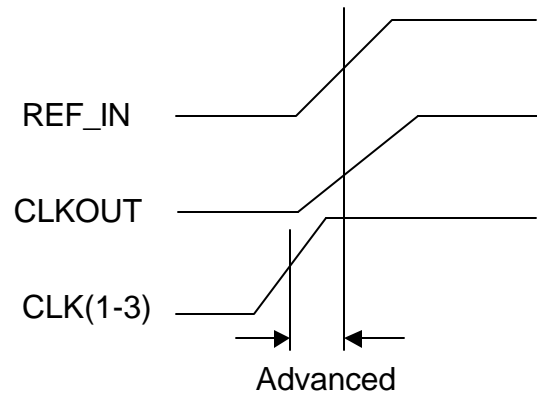
If applications requiring zero output-output skew, all the outputs must be equally loaded.

If the CLK(1-3) outputs are less loaded than CLKOUT, CLK(1-3) outputs will lead it; if the CLK(1-3) is more loaded than CLKOUT, CLK(1-3) will lag the CLKOUT.

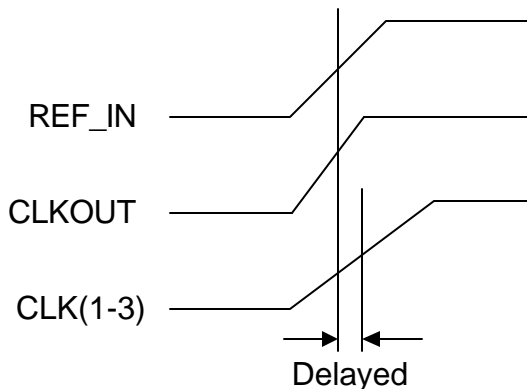
Since the CLKOUT and the CLK(1-3) outputs are identical, they all start at the same time, but difference loads cause them to have different rise times and different times crossing the measurement thresholds.



REF\_IN input and all outputs loaded equally



REF\_IN and CLK(1-3) outputs loaded equally, with CLK(1-3) less loaded than CLKOUT.



REF\_IN input and CLK(1-3) outputs loaded equally, with CLK(1-3) more loaded than CLKOUT.

**PACKAGE INFORMATION**

8 PIN Narrow SOIC ( mm )

Symbol	SOIC	
	Min.	Max.
A	1.55	1.73
A1	0.15	0.18
B	0.35	0.49
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
H	5.84	6.20
L	0.41	0.89
e	1.27 BSC	

**ORDERING INFORMATION**

*For part ordering, please contact our Sales Department:*  
 47745 Fremont Blvd., Fremont, CA 94538, USA  
 Tel: (510) 492-0990 Fax: (510) 492-0991

**PART NUMBER**

The order number for this device is a combination of the following:  
 Device number, Package type and Operating temperature range

**PLL102-15 S C**

PART NUMBER ————

- TEMPERATURE  
C=COMMERCIAL (0°~70°C)
- PACKAGE TYPE  
S=SOIC

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**REVISION HISTORY**

- 06/20/01 Created from preliminary PLL102-05 and PLL102-04 Document  
10/23/01 Removed Power Down mode in absence of REF (not supported in final version).  
11/07/01 Added VDD = 3.3V in Electrical Specs for clarity.  
11/29/01 Added Remark on REF clock absence on page 1  
10/08/02 Change pass through modulation rate from 100kHz to 33kHz.  
01/13/03 Changed Frequency range from "25-75MHz" to "25-60MHz" on Features section on page 1  
Changed Supply Current (I<sub>DD</sub>) from Unloaded outputs at "66.67MHz" to "60MHz" on page 3  
Changed Max. of Output Frequency from "75" to "60" on page 4  
Deleted "Fout < 50.0MHz" for Duty Cycle (Dt2) and "Measured at 60MHz" for Cycle to Cycle Jitter (T<sub>cyc-cyc</sub>) of Switching Characteristics section on page 4  
05/06/03 Bonding diagram modification to P102-15 (ICS553 compatible)