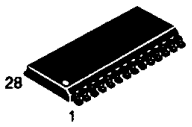
Advance Information

MC145031 Encoder
MC145032 Decoder
MC145033 Encoder/Decoder
MC145034 Encoder
MC145035 Decoder

CMOS

MC145031
MC145032
MC145033
MC145034
MC145035



DW SUFFIX
SOG PACKAGE
CASE 751F

ORDERING INFORMATION
MC14503xDW SOG Package

The encoders convert parallel address and data inputs into the Manchester code format and output the information serially via a data out pin.

The decoders revert the serial Manchester-coded input back into binary and compare the incoming address with local one. If both addresses match, an output valid signal (VD) is asserted and the proper data appears at the data out pins.

The difference between the MC145031/2 and MC145034/5 is the valid output pin, VD. The valid output of the MC145031/2 is a toggle function while the MC145034/5 is a "one shot" valid address output pulse if a correct data sequence and matched address is received.

The MC145033 encoder/decoder has a status output. The status pin, when high, indicates the device is encoding. During decoding or standby, status is low.

- Typical Applications: Remote Control, Security Systems, and Keyless Entry
- Manchester Coding
- RC Oscillator, No Crystal Required
- Binary Address and Data Inputs
- Two-Word Transmit Sequence
- Built-In Input Data Amplifier
- Schmitt-Trigger Serial Input for Excellent Noise Immunity
- Code Break Output with Adjustable Error Code Transmission Time Window
- Operating Voltage Range: 2 to 6 V
- Operating Temperature Range: –40° to 85°C
- MC145031 Encoder/MC145032 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines
- MC145033 Encoder/Decoder: 15 Address Lines
- MC145034 Encoder/MC145035 Decoder Pair: 13 Address and 4 Data Lines or 17 Address Lines

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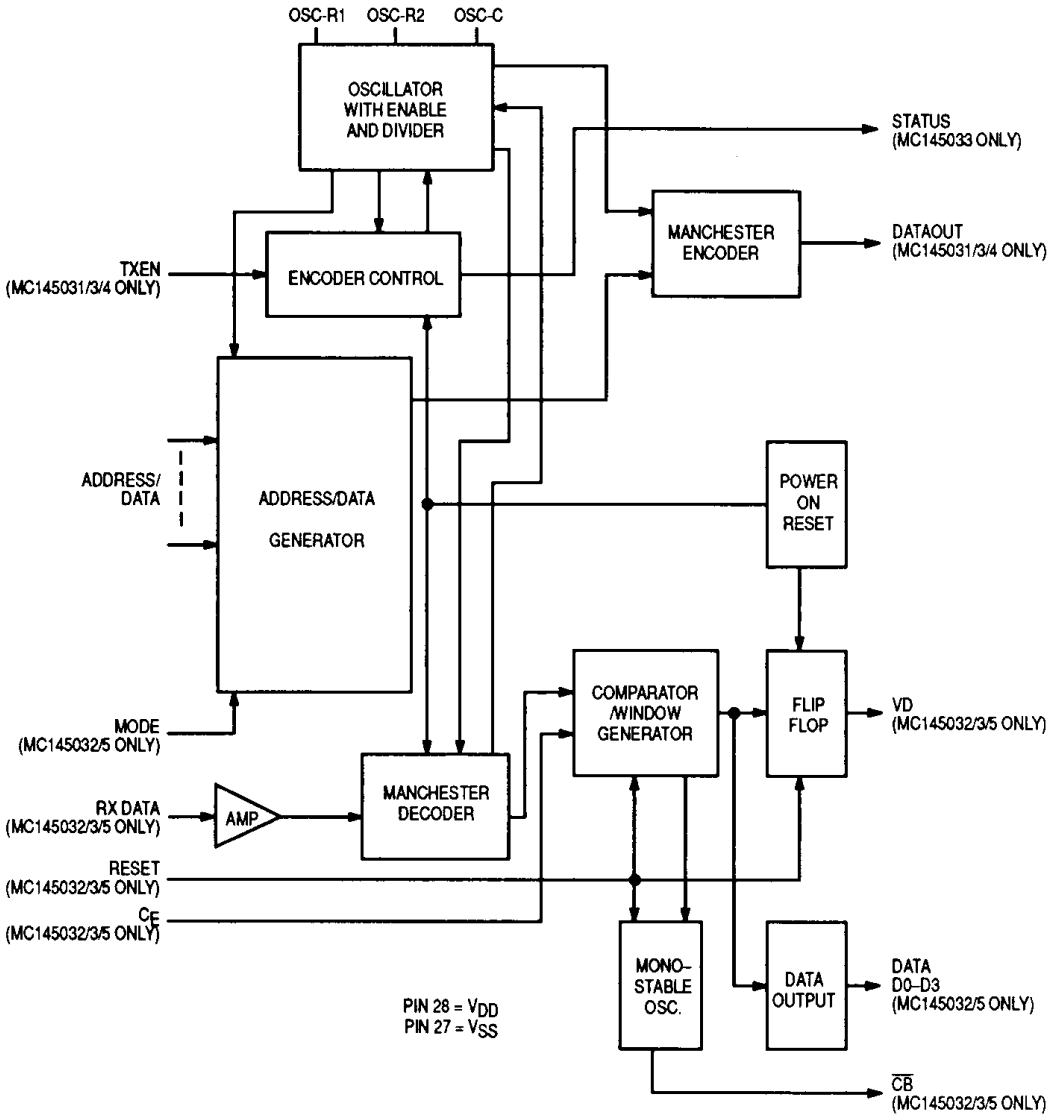
This document contains information on a new product. Specifications and information herein are subject to change without notice.

BLOCK DIAGRAM OF MC145031/2/3/4/5



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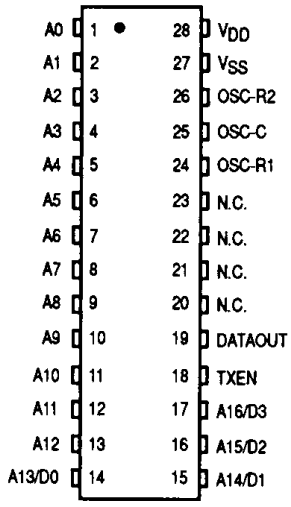
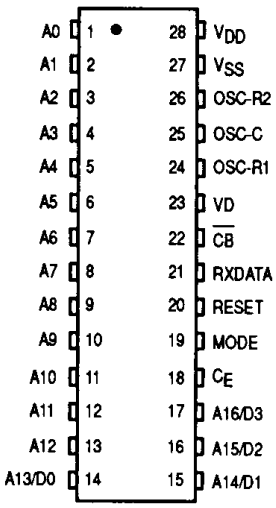
PIN ASSIGNMENTS

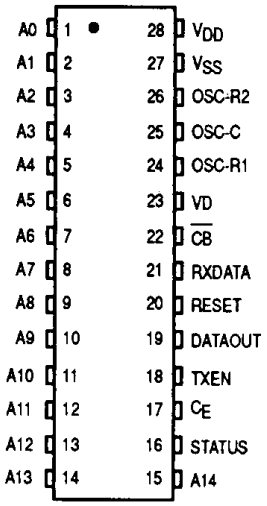
MC145031 ENCODER



MC145032 DECODER



MC145033 ENCODER/DECODER



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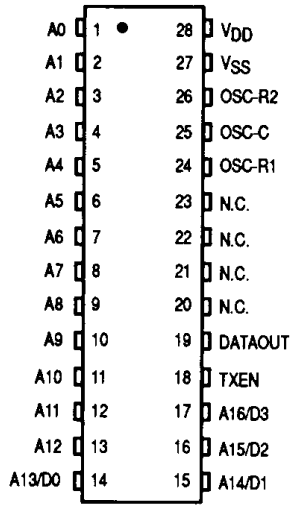
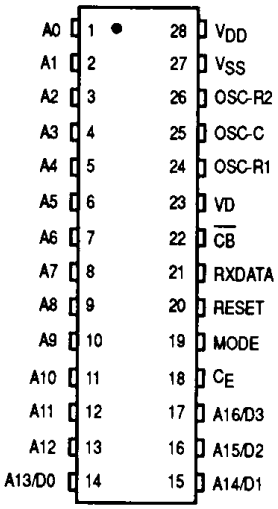
MC145034 ENCODER



MC145035 DECODER



MAXIMUM RATING* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	–0.5 to +0.7	V
V_{in}	DC Input Voltage	–0.5 to V_{DD}+0.5	V
V_{out}	DC Output Voltage	–0.5 to V_{DD}+0.5	V
I_{in}	DC Input Current, per Pin	±10	mA
I_{out}	DC Output Current, per Pin	±10	mA
I_{DD}	DC Supply Current, V_{DD} and V_{SS} Pins	±30	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	–65 to +150	°C
T_L	Lead Temperature (10-second soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
† Power Dissipation Temperature Derating
–12 mW/°C from 65°C to 85°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$.

Except for the Address inputs, unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). The Address inputs may be left open, see Pin Descriptions. Unused outputs must be left open.

ELECTRICAL CHARACTERISTICS (T_A=–40° to 85°C, C_L=50 pF, V_{DD}=2.5 to 6 V unless otherwise stated)

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		—	2.0 to 6.0	V
V_{IL}	Maximum Low-Level Input Voltage Except RXDATA		2.5 6.0	0.3 1.2	V
V_{IH}	Minimum High-Level Input Voltage Except RXDATA		2.5 6.0	1.9 4.5	V
V_{OL}	Maximum Low-Level Output Voltage	I_{out}=0 µA I_{out}=0.4 mA	2.5	0.15 0.4	V
		I_{out}=0 µA I_{out}=1.0 mA	6.0	0.15 0.4	
V_{OH}	Minimum High-Level Output Voltage	I_{out}=0 µA I_{out}=–0.4 mA	2.5	2.35 2.0	V
		I_{out}=0 µA I_{out}=–1.0 mA	6.0	5.85 5.5	
I_{in}	Maximum Input Current RXDATA TXEN, Reset, OSC-R2	V_{in}=V_{DD} or V_{SS}	6.0	±80 ±0.3	µA
I_{IH}	Maximum High-Level Input Leakage Current A0–A16	V_{in}=V_{DD}	6.0	0.3	µA
I_{IL}	Maximum Low-Level Pull–Up Current A0–A16	V_{in}=V_{SS}	6.0	–100	µA
I_{OZ}	Maximum 3–State Leakage Current Data Out	V_{out}=V_{DD} or V_{SS}	6.0	±500	nA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Device in standby mode, V_{in}=V_{DD} or V_{SS} for TXEN, Decoder in, Reset, OSC-R2. V_{in}=V_{SS}, V_{DD}, or open for A0–A16. I_{out}=0 µA	2.5 6.0	25 100	µA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	Oscillator Frequency =500 kHz. V_{in}=V_{SS} or V_{DD} for TXEN, Reset, OSC-R2. V_{in}=V_{SS}, V_{DD}, or open for A0–A16. I_{out}=0 µA	2.5 6.0	700 2500	µA
I_{OL}	Code Break Sink Current $\overline{CB}$			5	mA
V_{in}	Minimum RXDATA Input Level For Decoder	Square wave, see Figure 1	6.0	200	mV pp

AC ELECTRICAL CHARACTERISTICS (T_A=25°C, C_L=50 pF, V_{DD}=2.5 to 6 V unless otherwise stated)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{OSC}	Maximum Oscillator Frequency (50% Duty Cycle) (Figure 2)	—	500	kHz
t_d	Debounce Time, TXEN (guarantees 1 encoding sequence)	—	500	OSC cycles
t_w	Minimum Input Pulse Width, TXEN or Reset (Figure 3)	2.5 6.0	200 80	ns
C_{in}	Maximum Input Capacitance	—	10	pF

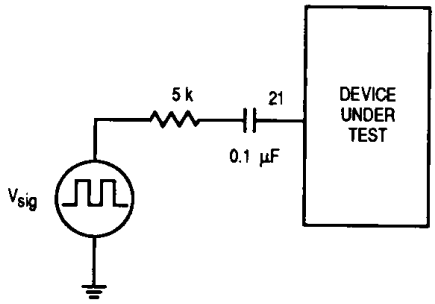


Figure 1. Decoder In Sensitivity Test

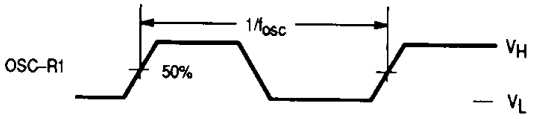


Figure 2. Switching Waveform

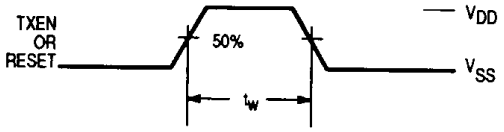


Figure 3. Switching Waveform

GENERAL DESCRIPTION

ENCODER

The encoder circuit encodes the parallel binary input address/data into manchester code and outputs the information serially.

Each transmitted word is preceded by a two-bit dead time interval. Once the TXEN (transmit enable) pin is triggered by a high level, a two-word transmit sequence following a 12-bit preamble is serially output at the DATAOUT terminal. The transmit sequences repeat continuously if the TXEN remains high. The minimum is one complete sequence; if TXEN goes low, the transmission continues until the end of the current transmit sequence.

The data rate is set at one eighth of the system clock, which is a RC oscillator.

One transmission cycle comprises:

1. 12-bit preamble
2. 2-bit dead time interval
3. First word
4. 2-bit dead time interval
5. Second word

One transmitted word consists of:

1. 2 start bits
2. The address/data bits
3. 2 stop bits

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DECODER

The decoder circuit accepts a serial manchester-coded input at the RXDATA pin. The data stream is then decoded and compared with the local address set by the parallel address inputs. When a correct transmit sequence (two identical words) is received and the incoming address matches the local one, the VD output on the MC145035 goes high and the decoded data may then be read at the data outputs D0–D3 if the mode pin is high. See the mode pin discription. The valid output VD remains high unless an erroneous address/data is detected or the transmit sequence is terminated.

For the MC145032 and MC145033, the valid data output (VD) is a toggle function. That is, VD changes state once each time a valid sequence of bits is received. If needed, VD can be reset to a low level via the reset pin.

If the decoder detects an error in the incoming transmit sequence, a time window is opened at the end of that sequence. If two consecutive erroneous transmit sequences are received within that window, the code break output $\overline{CB}$ goes low until the window's duration is over. During the opened window, the $\overline{CB}$ output can be reset by either the reset input or a correct transmit sequence that follows. The window duration is controlled by an external capacitor connected to pin C_E. The duration of the code break output is equal to TB which is half of error window time constant TE.

PIN DESCRIPTIONS

V_{DD} (Pin 28)

Power supply. This pin may range from +2 to+ 6 V with respect to V_{SS}.

V_{SS} (Pin 27)

Power supply ground.

TXEN (Pin 18)—MC145031, MC145033, and MC145034 Only

Transmit enable. A low to high transition on this pin initiates a transmit sequence. Transmission is continuous if TXEN remains high.

DATA OUT (Pin 19)—MC145031, MC145033, and MC145034 Only

Three-state encoder output. It serially outputs the manchester-coded transmit data, when initiated by TXEN.

VD (Pin 23)—MC145032 and MC145033 Only

Decoder valid address output. This "toggle" output changes state whenever correct transmit sequence is received and the address matches the local one. See Figure 4. A high level on VD can be cleared by either a correct transmit sequence that follows or the reset input.

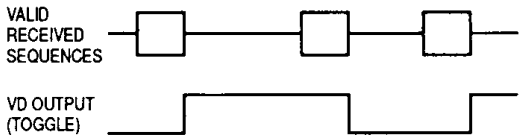

Figure 4. Valid Address Output Timing (MC145032 and MC145033)

VD (Pin 23)—MC145035 Only

Decoder valid address output. This pin goes high if and only if a correct transmit sequence is received and the address matches the local one. The valid output remains high unless an erroneous address/data is detected or the transmit sequence is terminated. The minimum duration of VD is guaranteed by an external RC. See Figures 5 and 6.

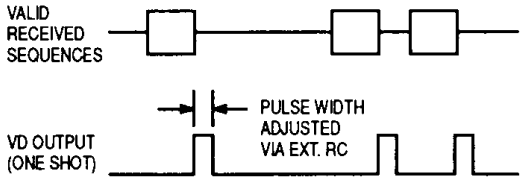

Figure 5. Valid Address Output Timing (MC145035)

RESET (Pin 20)—MC145032 and MC145033 Only

A positive pulse on this pin resets the code break output $\overline{CB}$ and valid address output VD.

RESET (Pin 20)—MC145035 Only

A positive pulse on this pin resets the code break output $\overline{CB}$ and the valid output VD. Its resets VD only when there is no RXDATA received. See Figure 6.

$\overline{CB}$ (Pin 22)—MC145032, MC145033, and MC145035 Only

Decoder code-break open-drain output. It goes low if two additional consecutive erroneous transmit sequences following the 1st error have been received within the window set by

external capacitor C_E. While in active state, it can be cleared by the reset input.

An external PNP transistor may be utilized to charge up the C_E (timing capacitor) to disable the low frequency oscillator. As a result, the TB counter stops. In this case, the $\overline{CB}$ output remains activated until a "reset" signal is applied to reset the C_E flip flop. See Figures 7 and 8.

A0 THROUGH A12 AND A13/D0 THROUGH A16/D3 (Pins 1 Through 17)—MC145031, MC145032, MC145034, and MC145035

Bidirectional address/data pins. These pins form a binary input port during encoding. The pins become a three-state data output port during decoding if the mode pin is tied to V_{DD}.

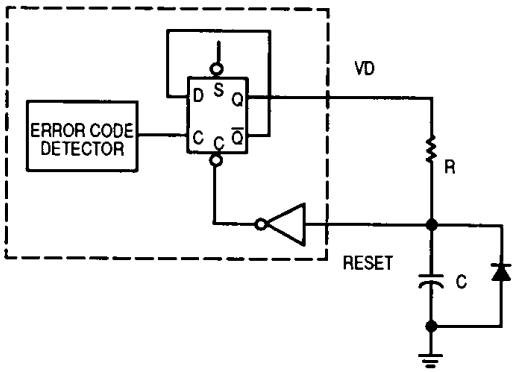

Figure 6. One Shot VD Output Circuit (MC145035)

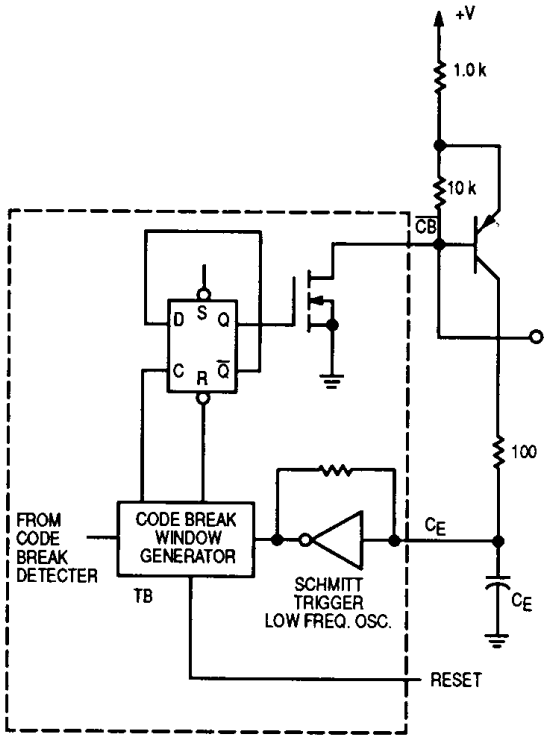

Figure 7. Code Break Window Control

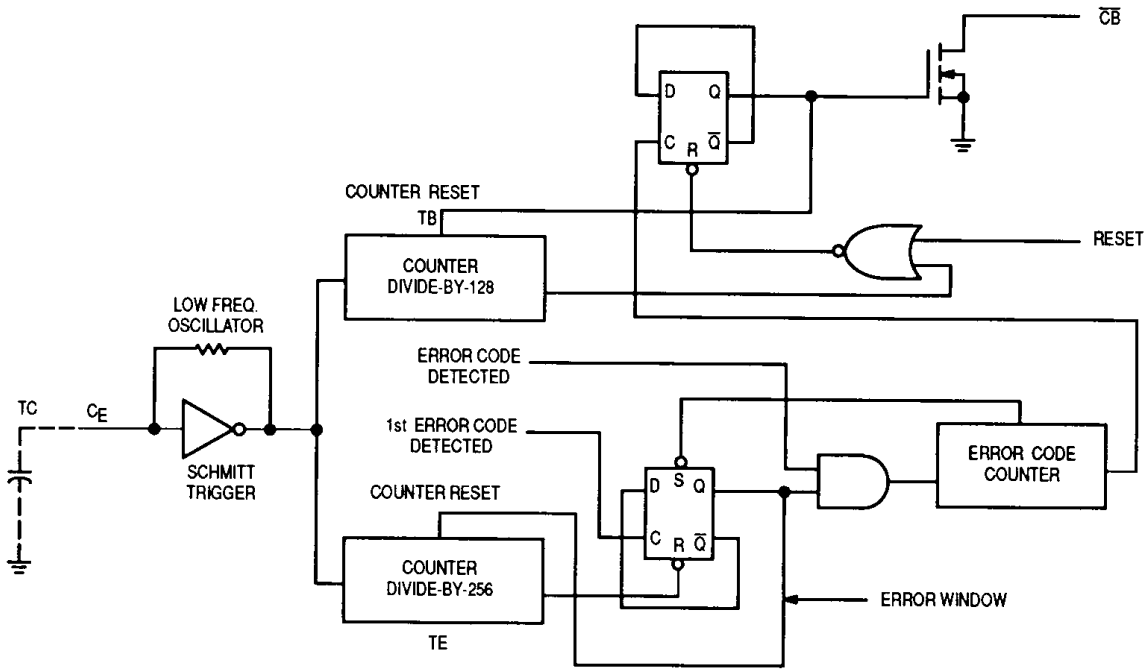

Figure 8. Error Window TE and Code Break Window Generator TB

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A0 Through A14 (Pins 1 through 15)—MC145033 Only

Binary address inputs. These pins form a binary input port during the encoding sequence. These inputs become the local address during the decoding sequence.

STATUS (Pin 16)—MC145033 Only

Encode/Decode Status. This pin is high during the encoding sequence and low during decoding or idle.

When Status is low, the DATAOUT pin is in the high-impedance state.

RXDATA (Pin 21)—MC145032, MC145033, and MC145035 Only

Serial data input to the Manchester decoder. Minimum encoded data signal level is 200 mV pp. See Figure 9.

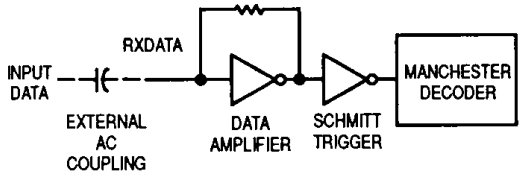
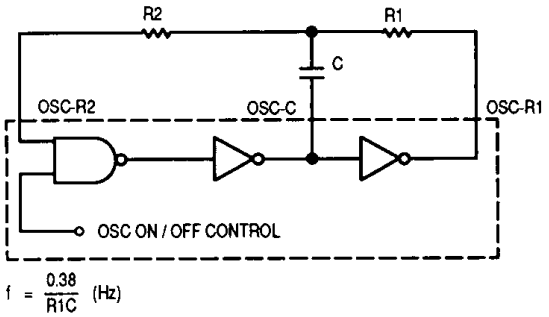


Figure 9. RXDATA Pin Coupling

OSC-R2, OSC-R1, OSC-C (Pins 26, 24, and 25)

Oscillator pins. The oscillator frequency is determined by the external RC network. See Figure 10.



for f ≤ 150 kHz where R2=2R1
The system oscillating frequency is eight times the Encoded Data Rate.

Figure 10. RC Oscillator

There is only 4% change in system oscillating frequency as the supply voltage varies from 2.0 volts to 6.0 volts.

The Encoder System Oscillating frequency can be varied ±10% with reference to Decoder system oscillator frequency for valid detection.

MODE (Pin 19)—MC145032 and MC145035

Mode select input. This pin defines the A13/D0–A16/D3 lines to be address or data lines. It is internally pulled high.

L=Address Lines
H=Data Lines

C_E (Pin 18—MC145032 and MC145035, Pin 17—MC145033)

Error window duration control input. The built-in schmitt trigger oscillator frequency is controlled by external capacitor C_E. The error window TE is equal to 256 times the internal oscillator cycle.

If an unmatched data word (error code) is detected, an internal error window TE is generated. If two or more errors are detected within the TE period, a code break signal $\overline{CB}$ is activated, signalling that an outsider is trying to break the code of this system. (Noise cannot activate the code break output.)

If only one error code is detected within the window, the window period is automatically extended from the last invalid word to check if there are two or more error codes. If so, the code break signal is activated; if not, TE is closed after a defined period. See Figures 8 and 11.

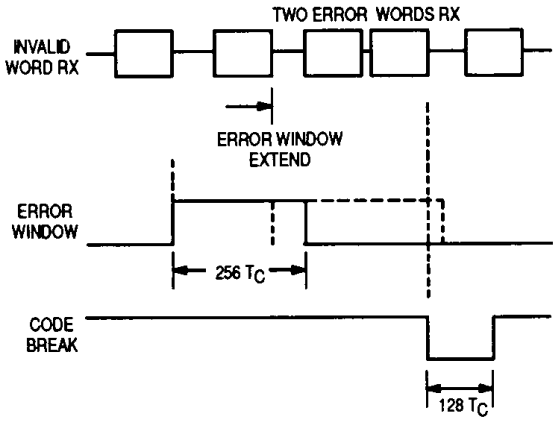


Figure 11. Error Window and Code Break Output Timing

TE and TB are generated from a schmitt-trigger low frequency oscillator of which the period (TC) is controlled by the timing capacitor C_E. The period of this low frequency oscillator is defined as TC as indicated in Figure 8.

TE is generated by an 8-stage counter.

TB is generated by an 7-stage counter.

TE=256 TC and TB=128 TC.

The relation between TC and the timing capacitor C_E is listed below with a 5.0-volt supply.

Timing Capacitor	Cycle Time TC
4.7 µF	1430 ms
1.0 µF	330 ms
0.1 µF	26 ms
0.047 µF	12 ms
0.022 µF	5.6 ms
0.01 µF	2.5 ms
0.0047 µF	1.0 ms
0.001 µF	0.3 ms

In order to minimize false $\overline{CB}$ triggers, one Error Code is allowed for every Error Window period (256 TC).

Suppose C_E = 4.7 µF, TC = 1430 ms, TE = 256 TC. On an average, it takes 2 to the power of 10 trials in order to succeed in breaking the system coding. Total time taken in breaking the system coding = # of trials x TC x 256.

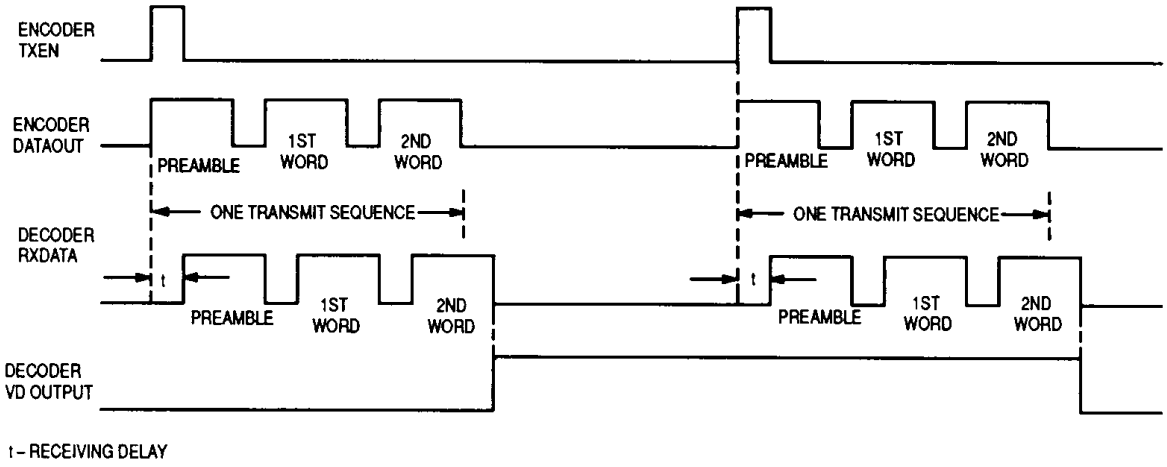


Figure 12. MC145031/2/3 Encoding and Decoding Timing Diagram

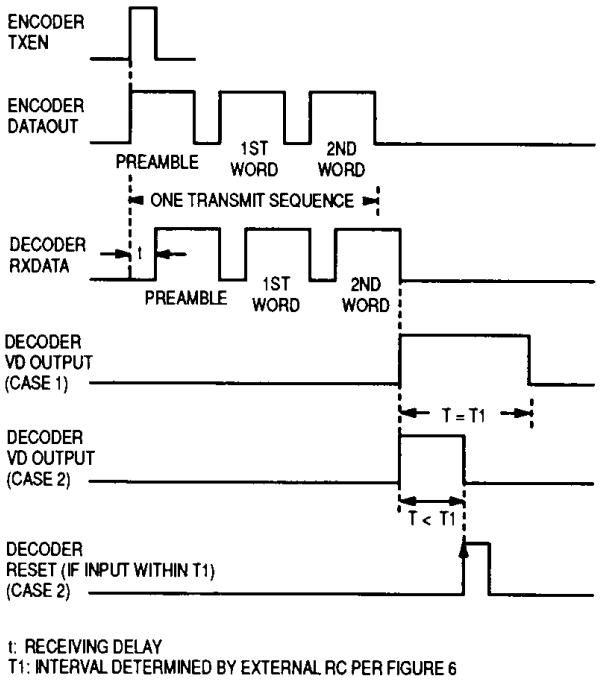


Figure 13. MC145034/5 Encoding and Decoding Timing Diagram — Single Transmission

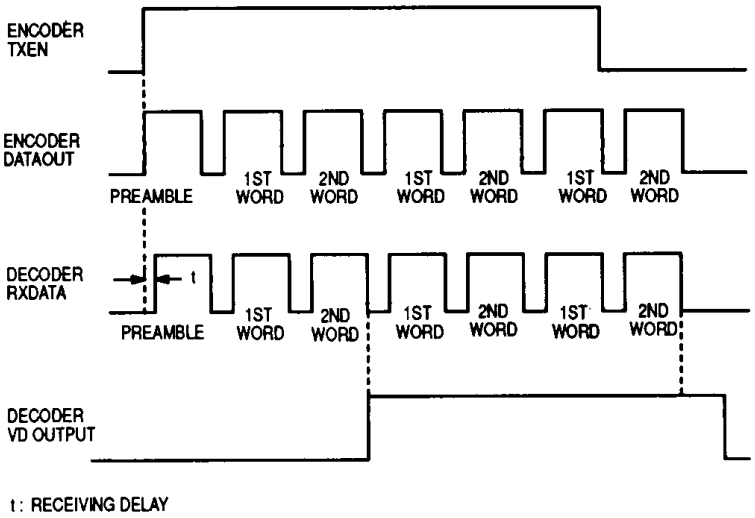


Figure 14. MC145034/5 Encoding and Decoding Timing Diagram — Continuous Transmissions

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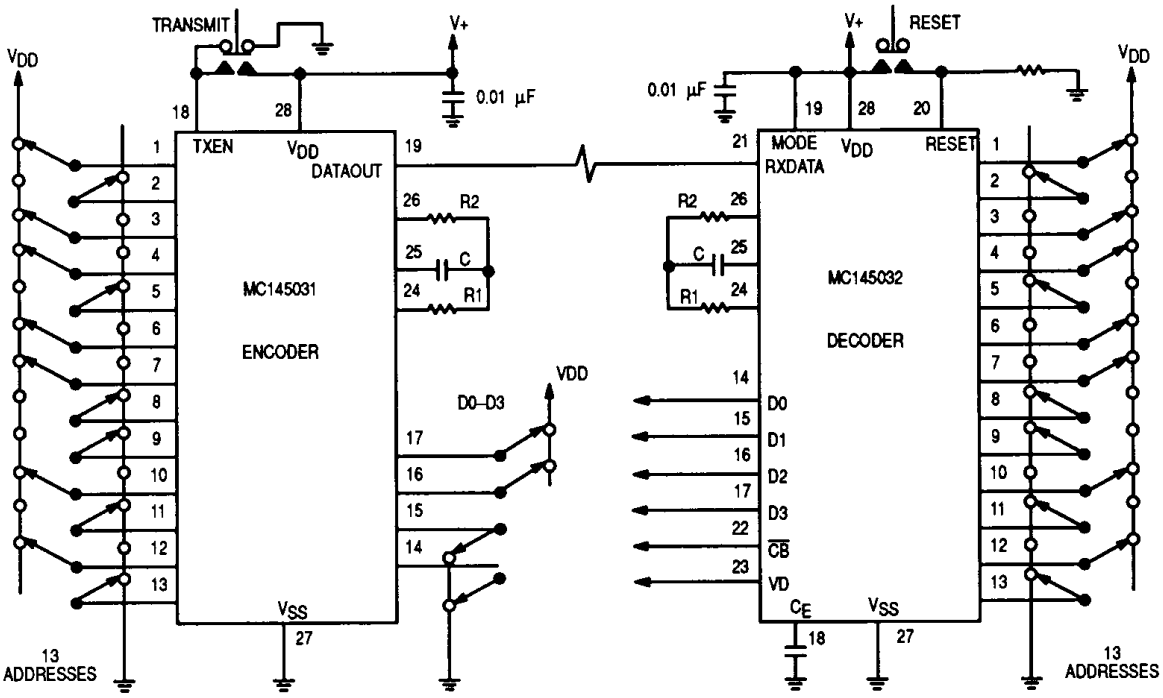

Figure 15. Typical Application