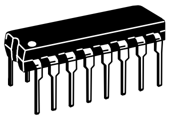
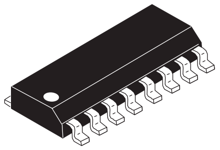
Freescale Semiconductor
Technical Data

MC145170-2/D
Rev. 5, 1/2005

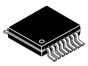
MC145170-2



Package Information
P Suffix
SOG Package
Case 648



Package Information
D Suffix
Plastic DIP Package
Case 751B



Package Information
DT Suffix
TSSOP Package
Case 948C

MC145170-2

PLL Frequency Synthesizer with Serial Interface

1 Introduction

The new MC145170-2 is pin-for-pin compatible with the MC145170-1. A comparison of the two parts is shown in Table 1 on page 2. The MC145170-2 is recommended for new designs and has a more robust power-on reset (POR) circuit that is more responsive to momentary power supply interruptions. The two devices are actually the same chip with mask options for the POR circuit. The more robust POR circuit draws approximately 20 µA additional supply current. Note that the maximum specification of 100 µA quiescent supply current has not changed.

The MC145170-2 is a single-chip synthesizer capable of direct usage in the MF, HF, and VHF bands. A special architecture makes this PLL easy to program. Either a bit- or byte-oriented format may be used. Due to the patented BitGrabber™ registers, no address/steering bits are required for *random access* of the three registers. Thus, tuning can be accomplished via a 2-byte serial transfer to the 16-bit N register.

Ordering Information

Device	Operating Temperature Range	Package
MC145170P2	T_A = -40 to 85°C	Plastic DIP
MC145170D2		SOG-16
MC145170DT2		TSSOP-16

Contents

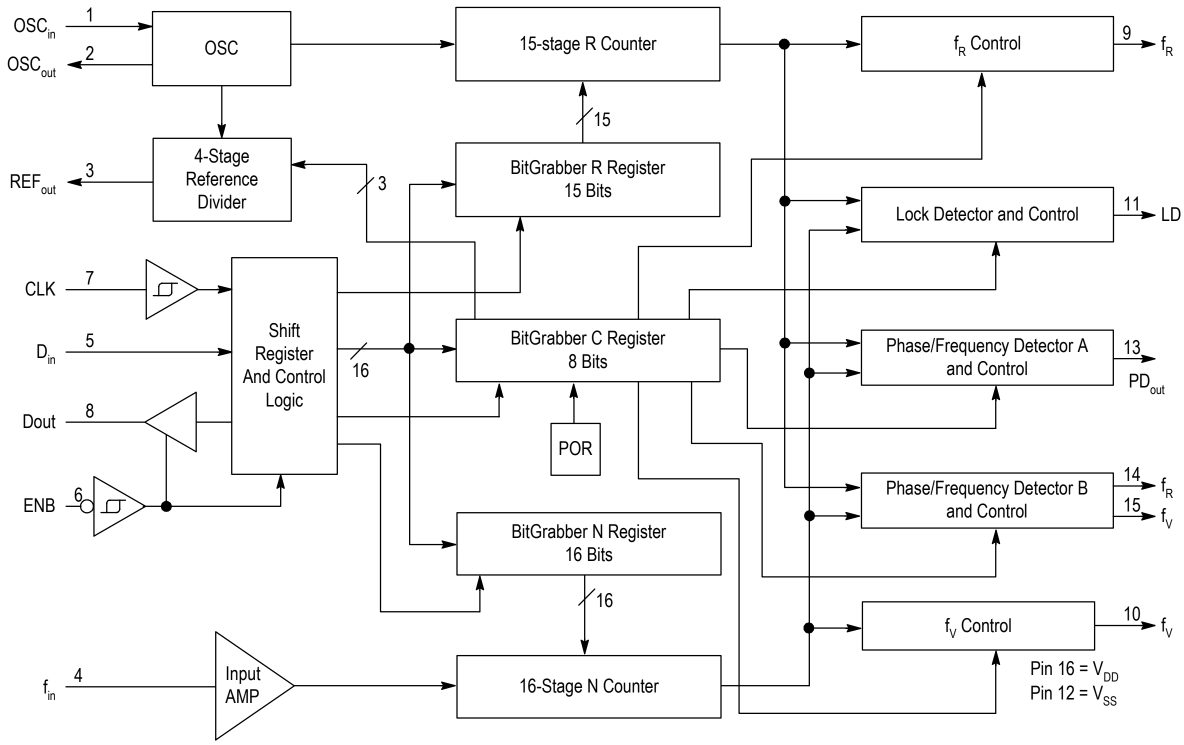
The device features fully programmable R and N counters, an amplifier at the f_{in} pin, on-chip support of an external crystal, a programmable reference output, and both single- and double-ended phase detectors with linear transfer functions (no dead zones). A configuration (C) register allows the part to be configured to meet various applications. A patented feature allows the C register to shut off unused outputs, thereby minimizing noise and interference.

In order to reduce lock times and prevent erroneous data from being loaded into the counters, a patented jam-load feature is included. Whenever a new divide ratio is loaded into the N register, both the N and R counters are jam-loaded with their respective values and begin counting down together. The phase detectors are also initialized during the jam load.

- Operating Voltage Range: 2.7 to 5.5 V
- Maximum Operating Frequency:
  185 MHz @ V_{in} = 500 mVpp, 4.5 V Minimum Supply
  100 MHz @ V_{in} = 500 mVpp, 3.0 V Minimum Supply
- Operating Supply Current:
  0.6 mA @ 3.0 V, 30 MHz
  1.5 mA @ 3.0 V, 100 MHz
  3.0 mA @ 5.0 V, 50 MHz
  5.8 mA @ 5.0 V, 185 MHz
- Operating Temperature Range: -40 to 85°C
- R Counter Division Range: 1 and 5 to 32,767
- N Counter Division Range: 40 to 65,535
- Programs through Standard Serial Peripheral Interface (SPI)
- See Application Notes AN1207/D and AN1671/D
- Contact Freescale for MC145170 control software.

Table 1. Comparision of the PLL Frequency Synthesizers

Parameter	MC145170-2	MC145170-1
Minimum Supply Voltage	2.7 V	2.5 V
Maximum Input Current, f_{in}	150 µA	120 µA
Dynamic Characteristics, f_{in} (Figure 26)	Unchanged	-
Power-On Reset Circuit	Improved	-



This device contains 4,800 active transistors.

Figure 1. Block Diagram

2 Electrical Characteristics

Table 2. Maximum Ratings (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to 5.5	V
DC Input Voltage	V_{in}	-0.5 to V_{DD} + 0.5	V
DC Output Voltage	V_{out}	-0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I_{in}	±10	mA
DC Output Current, per Pin	I_{out}	±20	mA
DC Supply Current, V_{DD} and V_{SS} Pins	I_{DD}	±30	mA
Power Dissipation, per Package	P_D	300	mW
Storage Temperature	T_{stg}	-65 to 150	°C
Lead Temperature, 1 mm from Case for 10 seconds	T_L	260	°C

Note: Maximum Ratings and ESD

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.
2. ESD data available upon request.

Table 3. Electrical Characteristics (Voltages Referenced to V_{SS}, T_A = -40 to 85°C)

Parameter	Test Condition	Symbol	V_{DD} V	Guaranteed Limit	Unit
Power Supply Voltage Range		V_{DD}	-	2.7 to 5.5	V
Maximum Low-Level Input Voltage[1] (D_{in}, CLK, $\overline{\text{ENB}}$, f_{in})	dc Coupling to f_{in}	V_{IL}	2.7 4.5 5.5	0.54 1.35 1.65	V
Minimum High-Level Input Voltage[1] (D_{in}, CLK, $\overline{\text{ENB}}$, f_{in})	dc Coupling to f_{in}	V_{IH}	2.7 4.5 5.5	2.16 3.15 3.85	V
Minimum Hysteresis Voltage (CLK, $\overline{\text{ENB}}$)		V_{Hys}	2.7 5.5	0.15 0.20	V
Maximum Low-Level Output Voltage (Any Output)	I_{out} = 20 µA	V_{OL}	2.7 5.5	0.1 0.1	V
Minimum High-Level Output Voltage (Any Output)	I_{out} = - 20 µA	V_{OH}	2.7 5.5	2.6 5.4	V
Minimum Low-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 0.3 V V_{out} = 0.4 V V_{out} = 0.5 V	I_{OL}	2.7 4.5 5.5	0.12 0.36 0.36	mA
Minimum High-Level Output Current (PD_{out}, REF_{out}, f_R, f_V, LD, ϕ_R, ϕ_V)	V_{out} = 2.4 V V_{out} = 4.1 V V_{out} = 5.0 V	I_{OH}	2.7 4.5 5.5	-0.12 -0.36 -0.36	mA
Minimum Low-Level Output Current (D_{out})	V_{out} = 0.4 V	I_{OL}	4.5	1.6	mA
Minimum High-Level Output Current (D_{out})	V_{out} = 4.1 V	I_{OH}	4.5	-1.6	mA
Maximum Input Leakage Current (D_{in}, CLK, $\overline{\text{ENB}}$, OSC_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±1.0	µA
Maximum Input Current (f_{in})	V_{in} = V_{DD} or V_{SS}	I_{in}	5.5	±150	µA
Maximum Output Leakage Current (PD_{out}) (D_{out})	V_{in} = V_{DD} or V_{SS}, Output in High-Impedance State	I_{OZ}	 5.5 5.5	 ±100 ±5.0	 nA µA
Maximum Quiescent Supply Current	V_{in} = V_{DD} or V_{SS}; Outputs Open; Excluding f_{in} Amp Input Current Component	I_{DD}	5.5	100	µA
Maximum Operating Supply Current	f_{in} = 500 mVpp; OSC_{in} = 1.0 MHz @ 1.0 Vpp; LD, f_R, f_V, REF_{out} = Inactive and No Connect; OSC_{out}, ϕ_V, ϕ_R, PD_{out} = No Connect; D_{in}, ENB, CLK = V_{DD} or V_{SS}	I_{dd}	-	[Note 2]	mA

Note: 1. When dc coupling to the OSC_{in} pin is used, the pin must be driven rail-to-rail. In this case, OSC_{out} should be floated.

2. The nominal values at 3.0 V are 0.6 mA @ 30 MHz, and 1.5 mA @ 100 MHz. The nominal values at 5.0 V are 3.0 mA @ 50 MHz, and 5.8 mA @ 185 MHz. These are not guaranteed limits.

Table 4. AC Interface Characteristics

(T_A = -40 to 85°C, C_L = 50 pF, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Serial Data Clock Frequency (Note: Refer to Clock t_w Below)	f_{clk}	2	2.7 4.5 5.5	dc to 3.0 dc to 4.0 dc to 4.0	MHz
Maximum Propagation Delay, CLK to D_{out}	t_{PLH}, t_{PHL}	2, 6	2.7 4.5 5.5	150 85 85	ns
Maximum Disable Time, D_{out} Active to High Impedance	t_{PLZ}, t_{PHZ}	3, 7	2.7 4.5 5.5	300 200 200	ns
Access Time, D_{out} High Impedance to Active	t_{PZL}, t_{PZH}	3, 7	2.7 4.5 5.5	0 to 200 0 to 100 0 to 100	ns
Maximum Output Transition Time, D_{out} CL = 50 pF	t_{TLH}, t_{THL}	2, 6	2.7 4.5 5.5	150 50 50	ns
CL = 200 pF		2, 6	2.7 4.5 5.5	900 150 150	ns
Maximum Input Capacitance - D_{in}, $\overline{\text{ENB}}$, CLK	C_{in}		-	10	pF
Maximum Output Capacitance - D_{out}	C_{out}		-	10	pF

Table 5. Timing Requirements (T_A = -40 to 85°C, Input $t_r = t_f$ = 10 ns, unless otherwise noted.)

Parameter	Symbol	Figure No.	V_{DD} V	Guaranteed Limit	Unit
Minimum Setup and Hold Times, D_{in} vs CLK	t_{su}, t_h	4	2.7 4.5 5.5	55 40 40	ns
Minimum Setup, Hold, and Recovery Times, $\overline{\text{ENB}}$ vs CLK	t_{su}, t_h, t_{rec}	5	2.7 4.5 5.5	135 100 100	ns
Minimum Inactive-High Pulse Width, $\overline{\text{ENB}}$	$t_{w(H)}$	5	2.7 4.5 5.5	400 300 300	ns
Minimum Pulse Width, CLK	t_w	2	2.7 4.5 5.5	166 125 125	ns
Maximum Input Rise and Fall Times, CLK	t_r, t_f	2	2.7 4.5 5.5	100 100 100	µs

2.1 Switching Waveforms

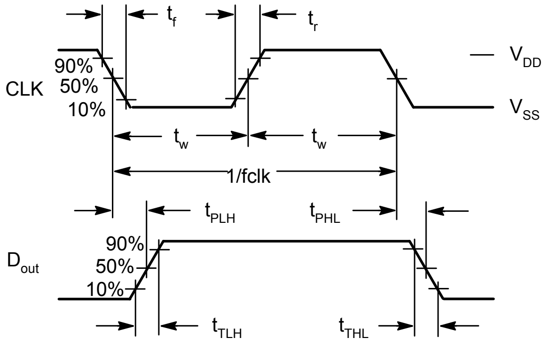


Figure 2.

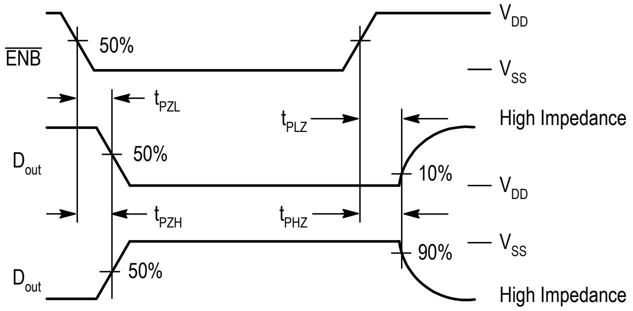


Figure 3.

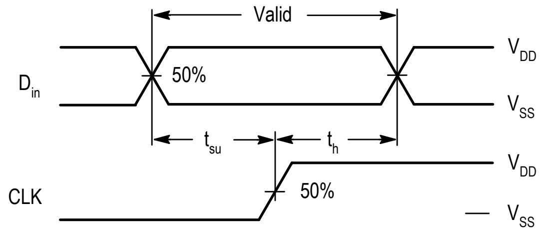


Figure 4.

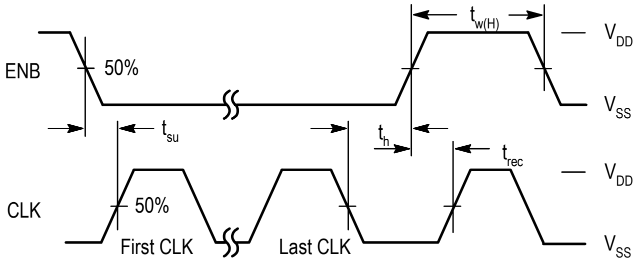
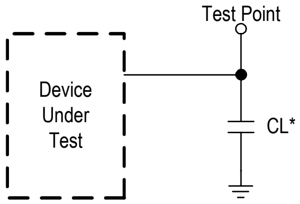
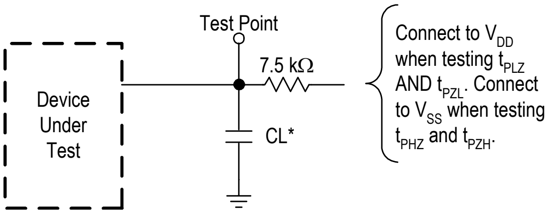


Figure 5.



* Includes all probe and fixture capacitance.

Figure 6. Test Circuit



*Includes all probe and fixture capacitance.

Figure 7. Test Circuit

Table 6. Loop Specifications (T_A = -40 to 85°C)

Parameter	Test Condition	Symbol	Figure No.	V_{DD} V	Guaranteed Range		Unit
					Min	Max	
Input Frequency, f_{in} [Note]	$V_{in} \geq$ 500 mVpp Sine Wave, N Counter Set to Divide Ratio Such that $f_V \leq$ 2.0 MHz	f	8	2.7 3.0 4.5 5.5	5.0 5.0 25 45	80 100 185 185	MHz
Input Frequency, OSC_{in} Externally Driven with ac-coupled Signal	$V_{in} \geq$ 1.0 V_{pp} Sine Wave, OSC_{out} = No Connect, R Counter Set to Divide Ratio Such that $f_R \leq$ 2 MHz	f	9	2.7 3.0 4.5 5.5	1.0* 1.0* 1.0* 1.0*	22 25 30 35	MHz
Crystal Frequency, OSC_{in} and OSC_{out}	C1 ≤ 30 pF C2 ≤ 30 pF Includes Stray Capacitance	f_{XTAL}	11	2.7 3.0 4.5 5.5	2.0 2.0 2.0 2.0	12 12 15 15	MHz
Output Frequency, REF_{out}	C_L = 30 pF	f_{out}	12, 14	2.7 4.5 5.5	dc dc dc	- 10 10	MHz
Operating Frequency of the Phase Detectors		f		2.7 4.5 5.5	dc dc dc	- 2.0 2.0	MHz
Output Pulse Width, ϕ_R, ϕ_V, and LD	f_R in Phase with f_V C_L = 50 pF	t_w	13, 14	2.7 4.5 5.5	- 20 16	- 100 90	ns
Output Transition Times, ϕ_R, ϕ_V, LD, f_R, and f_V	C_L = 50 pF	t_{TLH}, t_{THL}	13, 14	2.7 4.5 5.5	- - -	- 65 60	ns
Input Capacitance f_{in} OSC_{in}		C_{in}	- -	- -	- -	7.0 7.0	pF

* If lower frequency is desired, use wave shaping or higher amplitude sinusoidal signal in ac-coupled case. Also, see Figure 25 on page 22 for dc coupling.

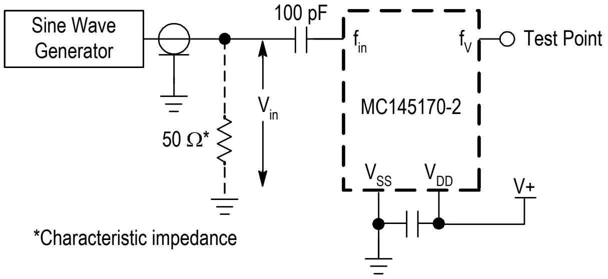


Figure 8. Test Circuit, f_{in}

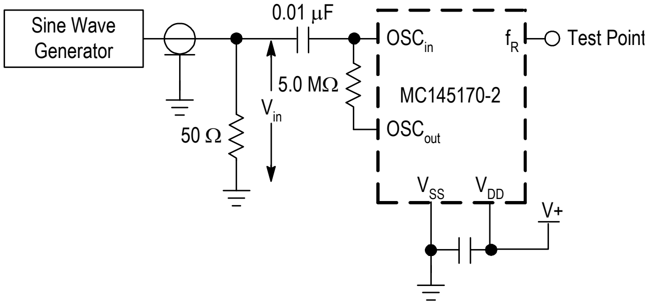


Figure 9. Test Circuit, OSC Circuitry Externally Driven [Note]

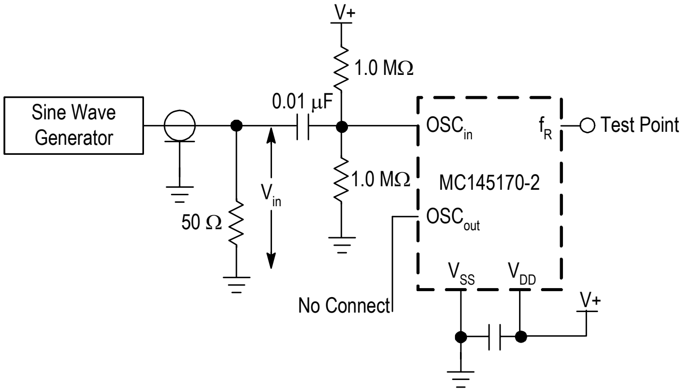


Figure 10. Circuit to Eliminate Self-Oscillation, OSC Circuitry Externally Driven [Note]

NOTE

Use the circuit of Figure 10 to eliminate self-oscillation of the OSC_{in} pin when the MC145170-2 has power applied with no external signal applied at V_{in}. (Self-oscillation is not harmful to the MC145170-2 and does not damage the IC.)

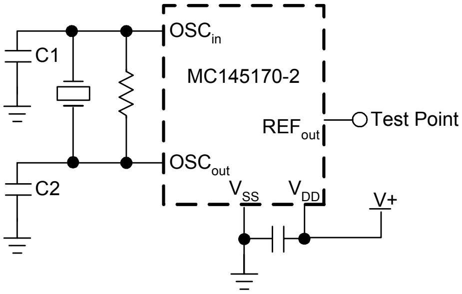


Figure 11. Test Circuit, OSC Circuit with Crystal

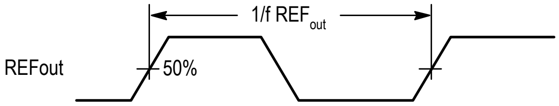


Figure 12. Test Circuit

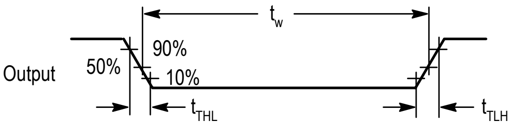
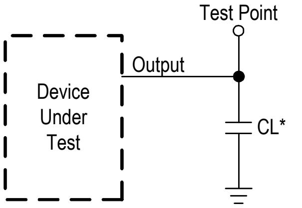


Figure 13. Switching Waveform



*Includes all probe and fixture capacitance.

Figure 14. Test Load Circuit

3 Pin Connections

3.1 Digital Interface Pins

D_{in}
Serial Data Input (Pin 5)

The bit stream begins with the most significant bit (MSB) and is shifted in on the low-to-high transition of CLK. The bit pattern is 1 byte (8 bits) long to access the C or configuration register, 2 bytes (16 bits) to access the N register, or 3 bytes (24 bits) to access the R register. Additionally, the R register can be accessed with a 15-bit transfer (see Table 7). An optional pattern which resets the device is shown in Figure 15. The values in the C, N, and R registers do not change during shifting because the transfer of data to the registers is controlled by $\overline{\text{ENB}}$.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the three registers. Random access of any register is provided (i.e., the registers may be accessed in any sequence). Data is retained in the registers over a supply range of 2.7 to 5.5 V. The formats are shown in Figures 15, 16, 17, and 18.

D_{in} typically switches near 50% of V_{DD} to maximize noise immunity. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail-to-rail. When interfacing to NMOS or TTL devices, either a level shifter (MC74HC14A, MC14504B) or pull-up resistor of 1 to 10 kΩ must be used. Parameters to consider when sizing the resistor are worst-case I_{OL} of the driving device, maximum tolerable power consumption, and maximum data rate.

Table 7. Register Access
(MSBs are shifted in first, C0, N0, and R0 are the LSBs)

Number of Clocks	Accessed Register	Bit Nomenclature
9 to 13	See Figure 15	(Reset)
8	C Register	C7, C6, C5, …, C0
16	N Register	N15, N14, N13, …, N0
15 or 24	R Register	R14, R13, R12, …, R0
Other Values ≤ 32	None	
Values > 32	See Figures 27 to 34	

CLK
Serial Data Clock Input (Pin 7)

Low-to-high transitions on Clock shift bits available at D_{in}, while high-to-low transitions shift bits from D_{out}. The chip's 16-1/2-stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode.

Four to eight clock cycles followed by five clock cycles are needed to reset the device; this is optional. Eight clock cycles are required to access the C register. Sixteen clock cycles are needed for the N register. Either 15 or 24 cycles can be used to access the R register (see Table 7 and Figures 15, 16, 17, and 18). For cascaded devices, see Figures 27 to 34.

CLK typically switches near 50% of V_{DD} and has a Schmitt-triggered input buffer. Slow CLK rise and fall times are allowed. See the last paragraph of $\mathbf{D_{in}}$ for more information.

NOTE

> To guarantee proper operation of the power-on reset (POR) circuit, the CLK pin must be held at the potential of either the V_{SS} or V_{DD} pin during power up. That is, the CLK input should not be floated or toggled while the V_{DD} pin is ramping from 0 to at least 2.7 V. If control of the CLK pin is not practical during power up, the initialization sequence shown in Figure 15 must be used.

$\overline{\text{ENB}}$
Active-Low Enable Input (Pin 6)

This pin is used to activate the serial interface to allow the transfer of data to/from the device. When $\overline{\text{ENB}}$ is in an inactive high state, shifting is inhibited, D_{out} is forced to the high-impedance state, and the port is held in the initialized state. To transfer data to the device, $\overline{\text{ENB}}$ (which must start inactive high) is taken low, a serial transfer is made via Din and CLK, and ENB is taken back high. The low-to-high transition on $\overline{\text{ENB}}$ transfers data to the C, N, or R register depending on the data stream length per Table 7.

NOTE

> Transitions on $\overline{\text{ENB}}$ must not be attempted while CLK is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{\text{ENB}}$ is high and CLK is low.

This input is also Schmitt-triggered and switches near 50% of V_{DD}, thereby minimizing the chance of loading erroneous data into the registers. See the last paragraph of D_{in} for more information.

D_{out}
Three-State Serial Data Output (Pin 8)

Data is transferred out of the 16-1/2-stage shift register through Dout on the high-to-low transition of CLK. This output is a No Connect, unless used in one of the manners discussed below.

Dout could be fed back to an MCU/MPU to perform a wrap-around test of serial data. This could be part of a system check conducted at power up to test the integrity of the system's processor, PC board traces, solder joints, etc.

The pin could be monitored at an in-line QA test during board manufacturing.

Finally, D_{out} facilitates troubleshooting a system and permits cascading devices.

3.2 Reference Pins

OSC_{in}/OSC_{out}
Reference Oscillator Input/Output (Pins 1, 2)

These pins form a reference oscillator when connected to terminals of an external parallel-resonant crystal. Frequency-setting capacitors of appropriate values as recommended by the crystal supplier are connected from each pin to ground (up to a maximum of 30 pF each, including stray capacitance). An external feedback resistor of 1.0 to 5.0 MΩ is connected directly across the pins to ensure linear operation of the amplifier. The required connections for the components are shown in Figure 11.

5 MΩ is required across the OSC_{in} and OSC_{out} pins in the ac-coupled case (see Figure 9 or alternate circuit Figure 10). *OSC_{out} is an internal node on the device and should not be used to drive any loads* (i.e., OSC_{out} is unbuffered). However, the buffered REF_{out} is available to drive external loads.

The external signal level must be at least 1 Vpp; the maximum frequencies are given in Table 6, the **Loop Specifications** table on page 7. These maximum frequencies apply for R Counter divide ratios as indicated in the table. For very small ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum input frequency of 2 MHz.)

If an external source is available which swings virtually rail-to-rail (V_{DD} to V_{SS}), then dc coupling can be used. In the dc-coupled case, no external feedback resistor is needed. OSC_{out} must be a No Connect to avoid loading an internal node on the device, as noted above. *For frequencies below 1 MHz, dc coupling must be used.* The R counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the OSC_{in} pin. See Figure 25.

Each rising edge on the OSC_{in} pin causes the R counter to decrement by one.

REF_{out}
Reference Frequency Output (Pin 3)

This output is the buffered output of the crystal-generated reference frequency or externally provided reference source. This output may be enabled, disabled, or scaled via bits in the C register (see Figure 16).

REF_{out} can be used to drive a microprocessor clock input, thereby saving a crystal. Upon power up, the on-chip power-on-initialize circuit forces REF_{out} to the OSC_{in} divided-by-8 mode.

REF_{out} is capable of operation to 10 MHz; see the **Loop Specifications** table. Therefore, divide values for the reference divider are restricted to two or higher for OSC_{in} frequencies above 10 MHz.

If unused, the pin should be floated and should be disabled via the C register to minimize dynamic power consumption and electromagnetic interference (EMI).

3.3 Counter Output Pins

f_R
R Counter Output (Pin 9)

This signal is the buffered output of the 15-stage R counter. f_R can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_R signal can be used to verify the R counter's divide ratio. This ratio extends from 5 to 32,767 and is determined by the binary value loaded into the R register. Also, direct access to the phase detector via the OSC_{in} pin is allowed by choosing a divide value of 1 (see Figure 17). The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_R must not exceed 2 MHz.

When activated, the f_R signal appears as normally low and pulses high. The pulse width is 4.5 cycles of the OSC_{in} pin signal, except when a divide ratio of 1 is selected. When 1 is selected, the OSC_{in} signal is buffered and appears at the f_R pin.

f_V
N Counter Output (Pin 10)

This signal is the buffered output of the 16-stage N counter. f_V can be enabled or disabled via the C register (patented). The output is disabled (static low logic level) upon power up. If unused, the output should be left disabled and unconnected to minimize interference with external circuitry.

The f_V signal can be used to verify the N counter's divide ratio. This ratio extends from 40 to 65,535 and is determined by the binary value loaded into the N register. The maximum frequency which the phase detectors operate is 2 MHz. Therefore, the frequency of f_V must not exceed 2 MHz.

When activated, the f_V signal appears as normally low and pulses high.

3.4 Loop Pins

f_{in}
Frequency Input (Pin 4)

This pin is a frequency input from the VCO. This pin feeds the on-chip amplifier which drives the N counter. This signal is normally sourced from an external voltage-controlled oscillator (VCO), and is ac-coupled into f_{in}. A 100 pF coupling capacitor is used for measurement purposes and is the minimum size recommended for applications (see Figure 25). The frequency capability of this input is dependent on the supply voltage as listed in Table 6, Loop Specifications. For small divide ratios, the maximum frequency is limited to the divide ratio times 2 MHz. (Reason: the phase/frequency detectors are limited to a maximum frequency of 2 MHz.)

For signals which swing from at least the V_{IL} to V_{IH} levels listed in Table 3, the Electrical Characteristics table on page 4, dc coupling may be used. Also, for low frequency signals (less than the minimum frequencies shown in Table 6 on page 7), dc coupling is a requirement. The N counter is a static counter and may be operated down to dc. However, wave shaping by a CMOS buffer may be required to ensure fast rise and fall times into the f_{in} pin. See Figure 25.

Each rising edge on the f_{in} pin causes the N counter to decrement by 1.

PD_{out}
Single-Ended Phase/Frequency Detector Output (Pin 13)

This is a three-state output for use as a loop error signal when combined with an external low-pass filter. Through use of a patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: negative pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: positive pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: positive pulses from high impedance

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: negative pulses from high impedance

Frequency and Phase of $f_V = f_R$: essentially high-impedance state; voltage at pin determined by loop filter

This output can be enabled, disabled, and inverted via the C register. If desired, PD_{out} can be forced to the high-impedance state by utilization of the disable feature in the C register (patented).

ϕ_R and ϕ_V
Double-Ended Phase/Frequency Detector Outputs (Pins 14, 15)

These outputs can be combined externally to generate a loop error signal. Through use of a patented technique, the detector's dead zone has been eliminated. Therefore, the phase/frequency detector is characterized by a linear transfer function. The operation of the phase/frequency detector is described below and is shown in Figure 19.

POL bit (C7) in the C register = low (see Figure 16)

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_V = negative pulses, ϕ_R = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_V = essentially high, ϕ_R = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

POL bit (C7) = high

Frequency of $f_V > f_R$ or Phase of f_V Leading f_R: ϕ_R = negative pulses, ϕ_V = essentially high

Frequency of $f_V < f_R$ or Phase of f_V Lagging f_R: ϕ_R = essentially high, ϕ_V = negative pulses

Frequency and Phase of $f_V = f_R$: ϕ_V and ϕ_R remain essentially high, except for a small minimum time period when both pulse low in phase

These outputs can be enabled, disabled, and interchanged via the C register (patented).

LD
Lock Detector Output (Pin 11)

This output is essentially at a high level with narrow low-going pulses when the loop is locked (f_R and f_V of the same phase and frequency). The output pulses low when f_V and f_R are out of phase or different frequencies (see Figure 19).

This output can be enabled and disabled via the C register (patented). Upon power up, on-chip initialization circuitry disables LD to a static low logic level to prevent a false “lock” signal. If unused, LD should be disabled and left open.

3.5 Power Supply

V_{DD}
Most Positive Supply Potential (Pin 16)

This pin may range from 2.7 to 5.5 V with respect to V_{SS}.

For optimum performance, V_{DD} should be bypassed to V_{SS} using low-inductance capacitor(s) mounted very close to the device. Lead lengths on the capacitor(s) should be minimized. (The very fast switching speed of the device causes current spikes on the power leads.)

V_{SS}
Most Negative Supply Potential (Pin 12)

This pin is usually ground. For measurement purposes, the V_{SS} pin is tied to a ground plane.

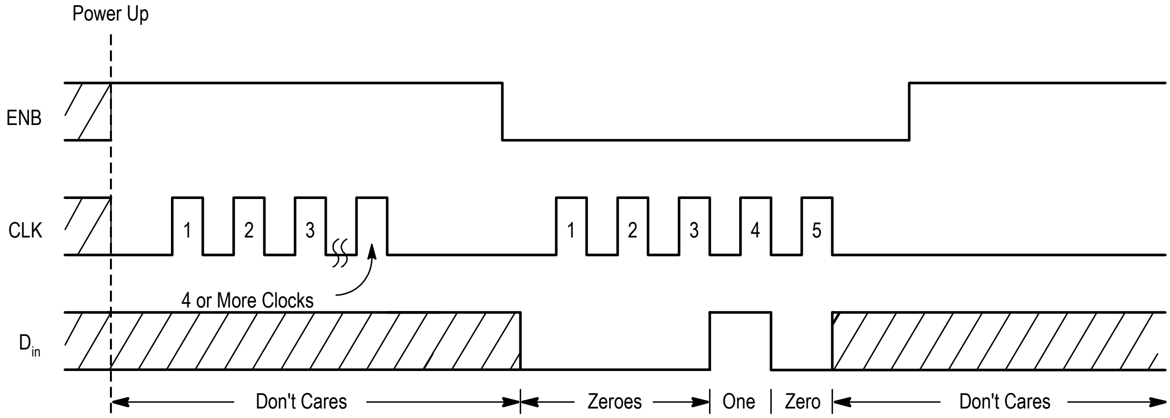
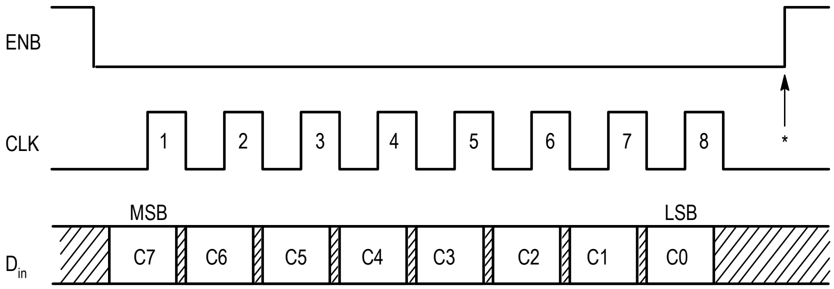


Figure 15. Reset Sequence

NOTES: This initialization sequence is usually not necessary because the on-chip power-on reset circuit performs the initialization function. However, this initialization sequence must be used immediately after power up if control of the CLK pin is not possible. That is, if CLK (Pin 7) toggles or floats upon power up, use the above sequence to reset the device. Also, use this sequence if power is momentarily interrupted such that the supply voltage to the device is reduced to below 2.7 V, but not down to at least 1 V (for example, the supply drops down to 2 V). This is necessary because the on-chip power-on reset is only activated when the supply ramps up from a voltage below approximately 1.0 V.



* At this point, the new byte is transferred to the C register and stored. No other registers are affected.

C7 - POL: Select the output polarity of the phase/frequency detectors. When set high, this bit inverts PD_{out} and interchanges the ϕ_R function with ϕ_V as depicted in Figure 19. Also see the phase detector output pin descriptions for more information. This bit is cleared low at power up.

C6 - PDA/B: Selects which phase/frequency detector is to be used. When set high, enables the output of phase/frequency detector A (PD_{out}) and disables phase/frequency detector B by forcing ϕ_R and ϕ_V to the static high state. When cleared low, phase/frequency detector B is enabled (ϕ_R and ϕ_V) and phase/frequency detector A is disabled with PD_{out} forced to the high-impedance state. This bit is cleared low at power up.

C5 - LDE: Enables the lock detector output when set high. When the bit is cleared low, the LD output is forced to a static low level. This bit is cleared low at power up.

C4 - C2, OSC2 - OSC0:

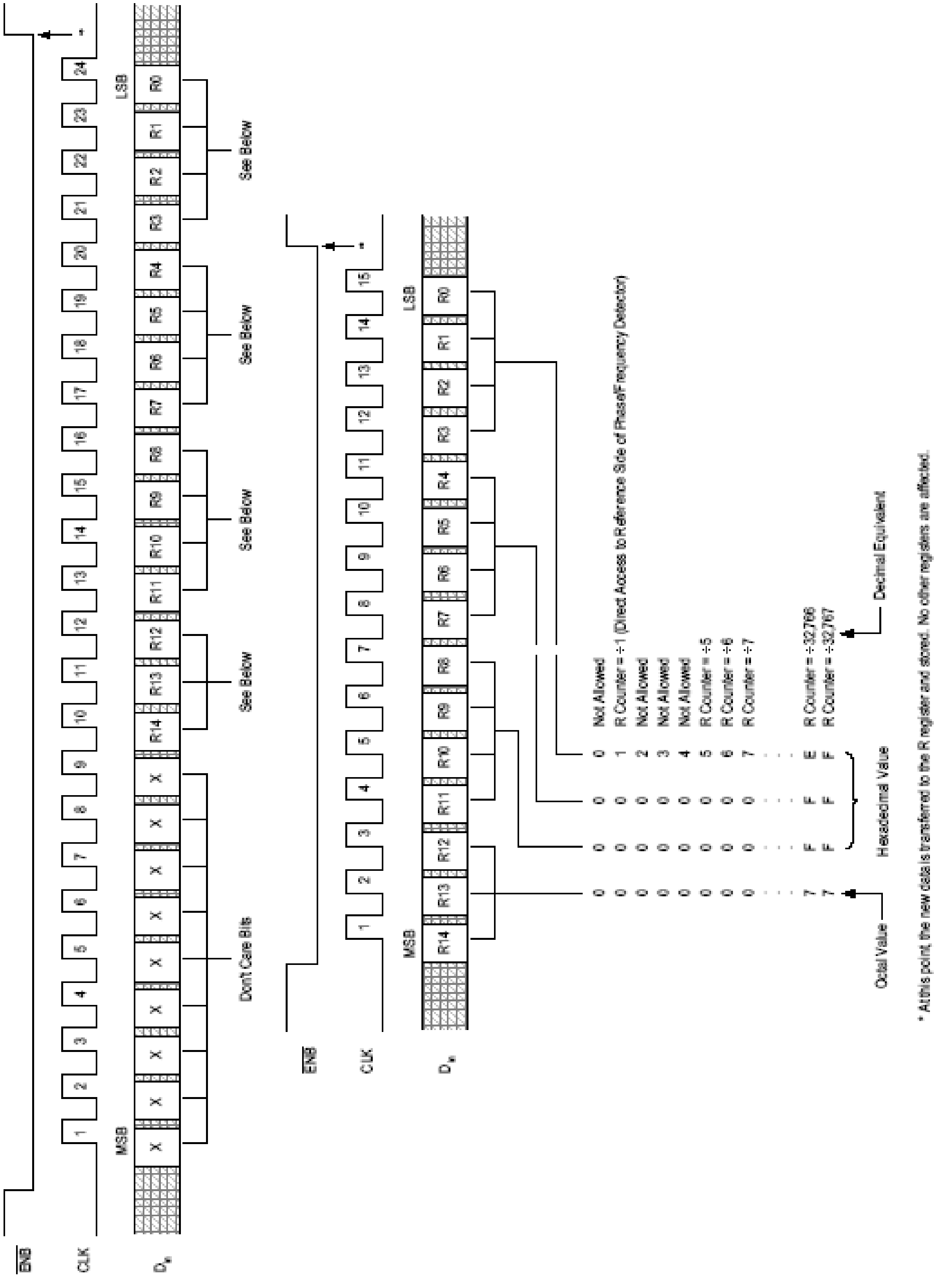
Reference output controls which determines the REF_{out} characteristics as shown below. Upon power up, the bits are initialized such that $OSC_{in}/8$ is selected.

C4	C3	C2	REF_{out} Frequency
0	0	0	dc (Static Low)
0	0	1	OSC_{in}
0	1	0	$OSC_{in}/2$
0	1	1	$OSC_{in}/4$
1	0	0	$OSC_{in}/8$ (POR Default)
1	0	1	$OSC_{in}/16$
1	1	0	$OSC_{in}/8$
1	1	1	$OSC_{in}/16$

C1 - f_VE: Enables the f_V output when set high. When cleared low, the f_V output is forced to a static low level. The bit is cleared low upon power up.

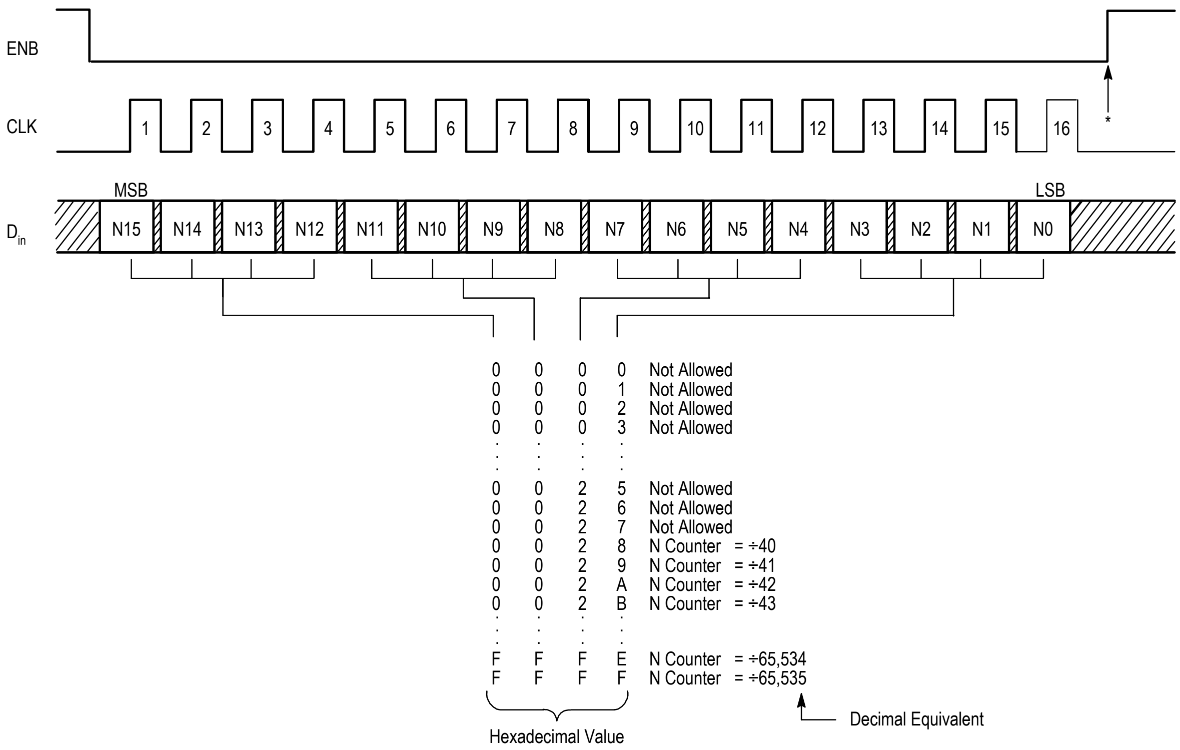
C0 - f_RE: Enables the f_R output when set high. When cleared low, the f_R output is forced to a static low level. The bit is cleared low upon power up.

Figure 16. C Register Access and Format (8 Clock Cycles are Used)



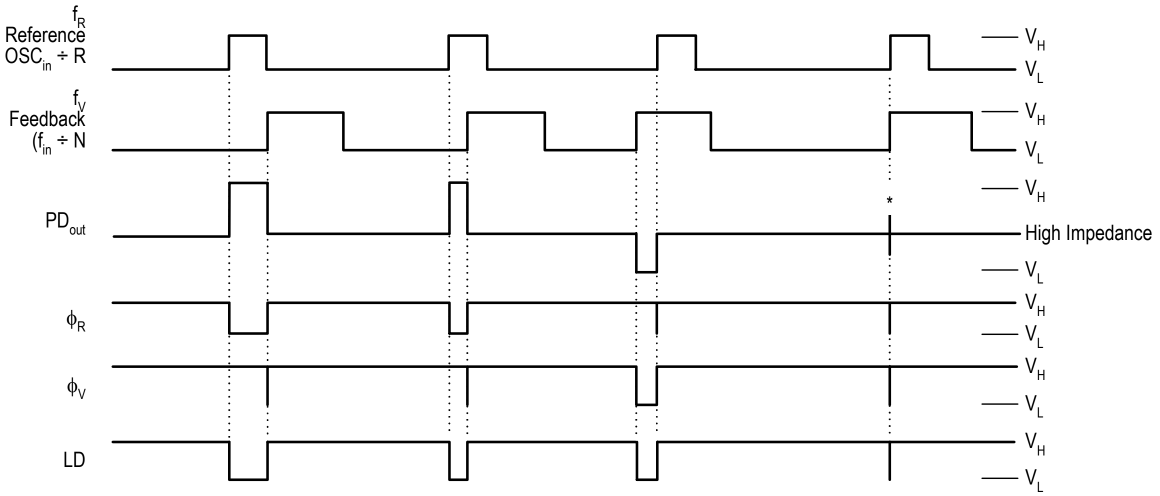
* At this point, the new data is transferred to the R register and stored. No other registers are affected.

Figure 17. R Register Access and Formats (Either 24 or 15 Clock Cycles Can Be Used)



* At this point, the two new bytes are transferred to the N register and stored. No other registers are affected. In addition, the N and R counters are jam-loaded and begin counting down together.

Figure 18. N Register Access and Format (16 Clock Cycles Are Used)



V_H = High voltage level
V_L = Low voltage level
*At this point, when both f_R and f_V are in phase, both the sinking and sourcing output FETs are turned on for a very short internal.

Note: The PD_{out} generates error pulses during out-of-lock conditions. When locked in phase and frequency, the output is high impedance and the voltage at that pin is determined by the low-pass filter capacitor. PDout, ϕ_R and ϕ_V are shown with the polarity bit (POL) = low; see Figure 16 for POL.

Figure 19. Phase/Frequency Detector and Lock Detector Output Waveforms

4 Design Considerations

4.1 Crystal Oscillator Considerations

The following options may be considered to provide a reference frequency to our CMOS frequency synthesizers.

4.1.1 Use of a Hybrid Crystal Oscillator

Commercially available temperature-compensated crystal oscillators (TCXOs) or crystal-controlled data clock oscillators provide very stable reference frequencies. An oscillator capable of CMOS logic levels at the output may be direct or dc coupled to OSC_{in}. If the oscillator does not have CMOS logic levels on the outputs, capacitive or ac coupling to OSC_{in} may be used (see Figures 9 and 10).

For additional information about TCXOs, visit *www.freescale.com* on the world wide web.

4.1.2 Use of the On-Chip Oscillator Circuitry

The on-chip amplifier (a digital inverter) along with an appropriate crystal may be used to provide a reference source frequency. A fundamental mode crystal, parallel resonant at the desired operating frequency, should be connected as shown in Figure 20.

The crystal should be specified for a loading capacitance (C_L) which does not exceed 20 pF when used at the highest operating frequencies listed in Table 6, **Loop Specifications**. Larger C_L values are possible for lower frequencies. Assuming R1 = 0 Ω, the shunt load capacitance (C_L) presented across the crystal can be estimated to be:

$$C_L = \frac{C_{in}C_{out}}{C_{in} + C_{out}} + C_a + C_{stray} + \frac{C1 \times C2}{C1 + C2}$$

where

C_{in} = 5.0 pF (see Figure 21)
C_{out} = 6.0 pF (see Figure 21)
C_a = 1.0 pF (see Figure 21)
C1 and C2 = external capacitors (see Figure 21)
C_{stray} = the total equivalent external circuit stray capacitance appearing across the crystal terminals

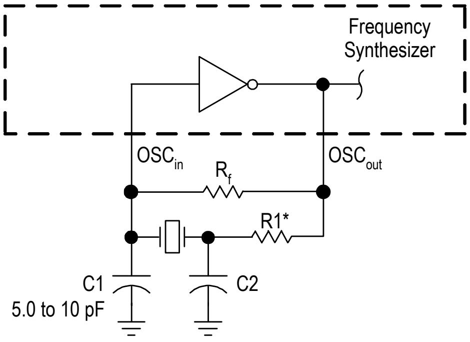
The oscillator can be “trimmed” on-frequency by making a portion or all of C1 variable. The crystal and associated components must be located as close as possible to the OSC_{in} and OSC_{out} pins to minimize distortion, stray capacitance, stray inductance, and startup stabilization time. Circuit stray capacitance can also be handled by adding the appropriate stray value to the values for C_{in} and C_{out}. For this approach, the term C_{stray} becomes 0 in the above expression for C_L.

A good design practice is to pick a small value for C1, such as 5 to 10 pF. Next, C2 is calculated. C1 < C2 results in a more robust circuit for start-up and is more tolerant of crystal parameter variations.

Power is dissipated in the effective series resistance of the crystal, R_e, in Figure 22. The maximum drive level specified by the crystal manufacturer represents the maximum stress that the crystal can withstand without damage or excessive shift in operating frequency. R1 in Figure 20 limits the drive level. The use of R1 is not necessary in most cases.

To verify that the maximum dc supply voltage does not cause the crystal to be overdriven, monitor the output frequency at the REF_{out} pin (OSC_{out} is not used because loading impacts the oscillator). The frequency should increase very slightly as the dc supply voltage is increased. An overdriven crystal decreases in frequency or becomes unstable with an increase in supply voltage. The operating supply voltage must be reduced or R1 must be increased in value if the overdriven condition exists. The user should note that the oscillator start-up time is proportional to the value of R1.

Through the process of supplying crystals for use with CMOS inverters, many crystal manufacturers have developed expertise in CMOS oscillator design with crystals. Discussions with such manufacturers can prove very helpful.



* May be needed in certain cases. See text.

Figure 20. Pierce Crystal Oscillator Circuit

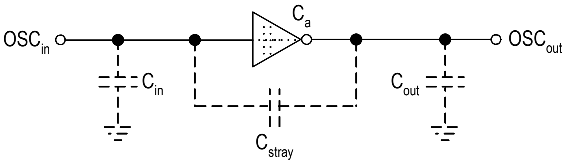
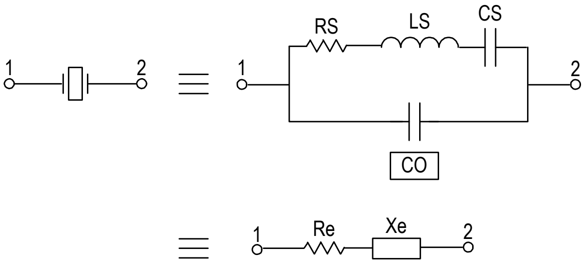
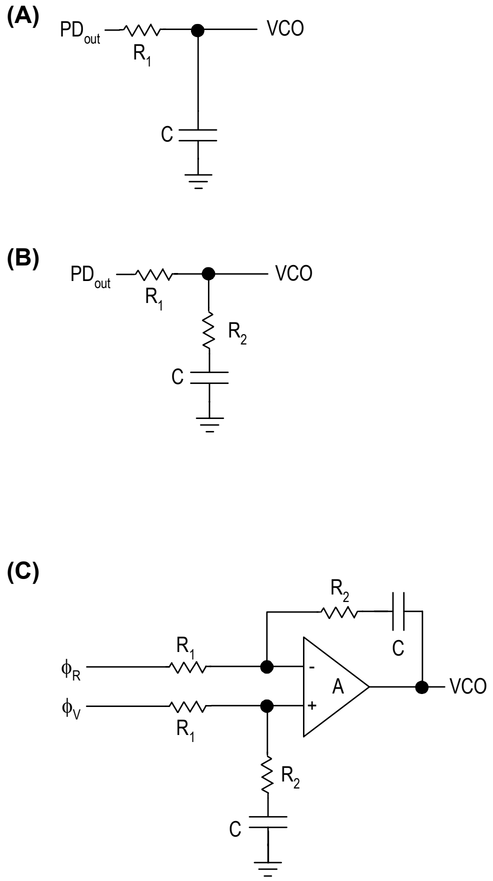


Figure 21. Parasitic Capacitances of the Amplifier and C_{stray}



NOTE: Values are supplied by crystal manufacturer (parallel resonant crystal).

Figure 22. Equivalent Crystal Networks



$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NR_1C}}$$

$$\zeta = \frac{N\omega_n}{2K_\phi K_{VCO}}$$

$$F(s) = \frac{1}{R_1sC + 1}$$

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NC(R_1 + R_2)}}$$

$$\zeta = 0.5\omega_n\left(R_2C + \frac{N}{K_\phi K_{VCO}}\right)$$

$$F(s) = \frac{R_2sC + 1}{(R_1 + R_2)sC + 1}$$

$$\omega_n = \sqrt{\frac{K_\phi K_{VCO}}{NCR_1}}$$

$$\zeta = \frac{\omega_n R_2 C}{2}$$

$$F(s) = \frac{R_2sC + 1}{R_1sC}$$

NOTES:

1. For (C), R_1 is frequently split into two series resistors; each resistor is equal to R_1 divided by 2. A capacitor C_C is then placed from the midpoint to ground to further filter the error pulses. The value of C_C should be such that the corner frequency of this network does not significantly affect ω_n.
2. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp.

Denifitions:

N = Total Division Ratio in Feedback Loop

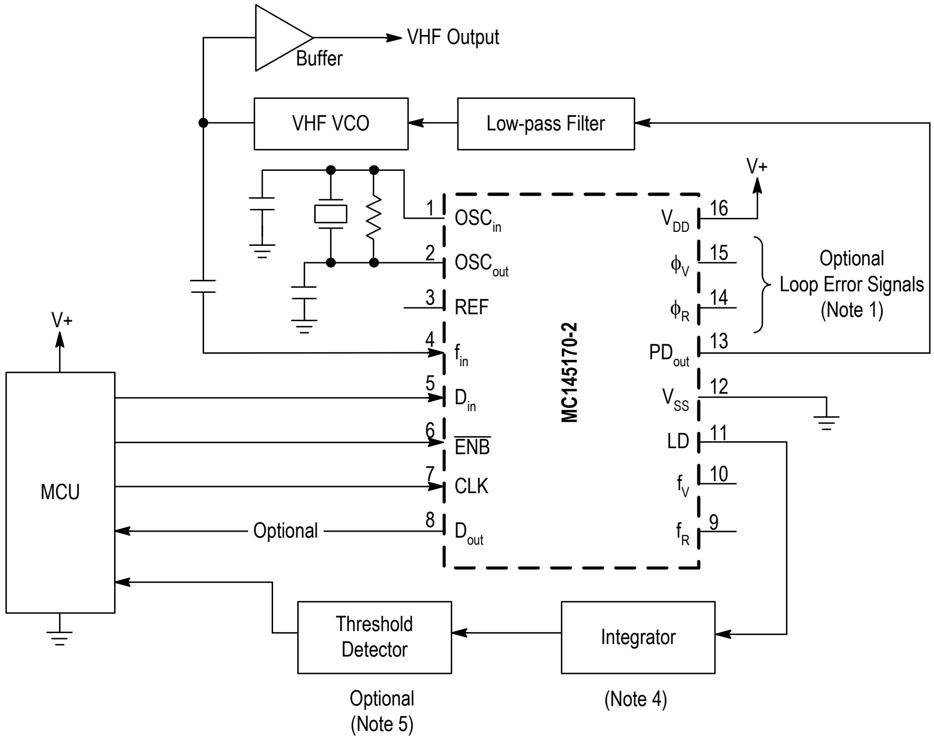
K_ϕ (Phase Detector Gain) = VDD/4p volts per radian for PDout

K_ϕ (Phase Detector Gain) - VDD/2p volts per radian for fV and fR

$$K_{VCO}(\text{VCO Gain}) = \frac{2\pi\Delta f_{VCO}}{\Delta V_{VCO}}$$

For a nominal design starting point, the user might consider a damping factor $\zeta = 0.7$ and a natural loop frequency $\omega_n = (2\pi f_R/50)$ where f_R is the frequency at the phase detector input. Larger ω_n values result in faster loop lock times and, for similar sideband filtering, higher f_R-related VCO standards.

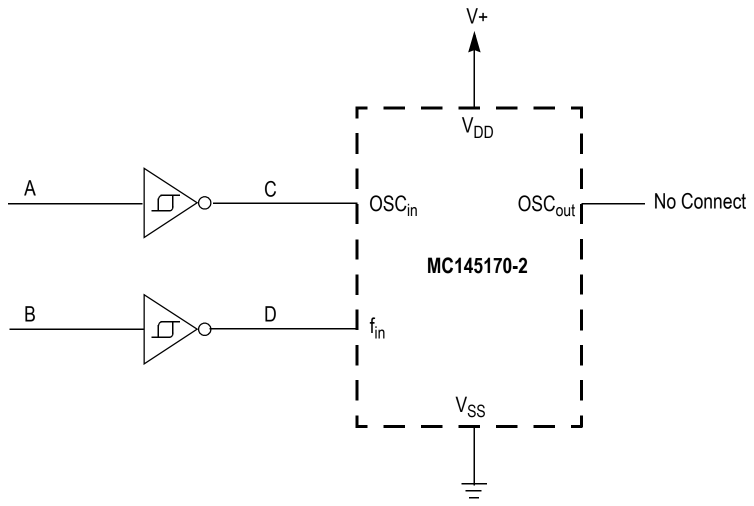
Figure 23. Phase-Locked Loop - Low Pass Filter Design



NOTES:

1. The ϕ_R and ϕ_V outputs are fed to an external combiner/loop filter. See the Phase-Locked Loop — Low-Pass Filter Design page for additional information. The ϕ_R and ϕ_V outputs swing rail-to-rail. Therefore, the user should be careful not to exceed the common mode input range of the op amp used inthe combiner/loop filter.
2. For optimum performance, bypass the V_{DD} pin to V_{SS} (GND) with one or more low-inductance capacitors.
3. The R counter is programmed for a divide value = OSC_{in}/f_R. Typically, f_R is the tuning resolution required for the VCO. Also, the VCO frequency divided by f_R = N, wher e N is the divide value of the N counter.
4. May be an R-C low-pass filter.
5. May be a bipolar transistor.

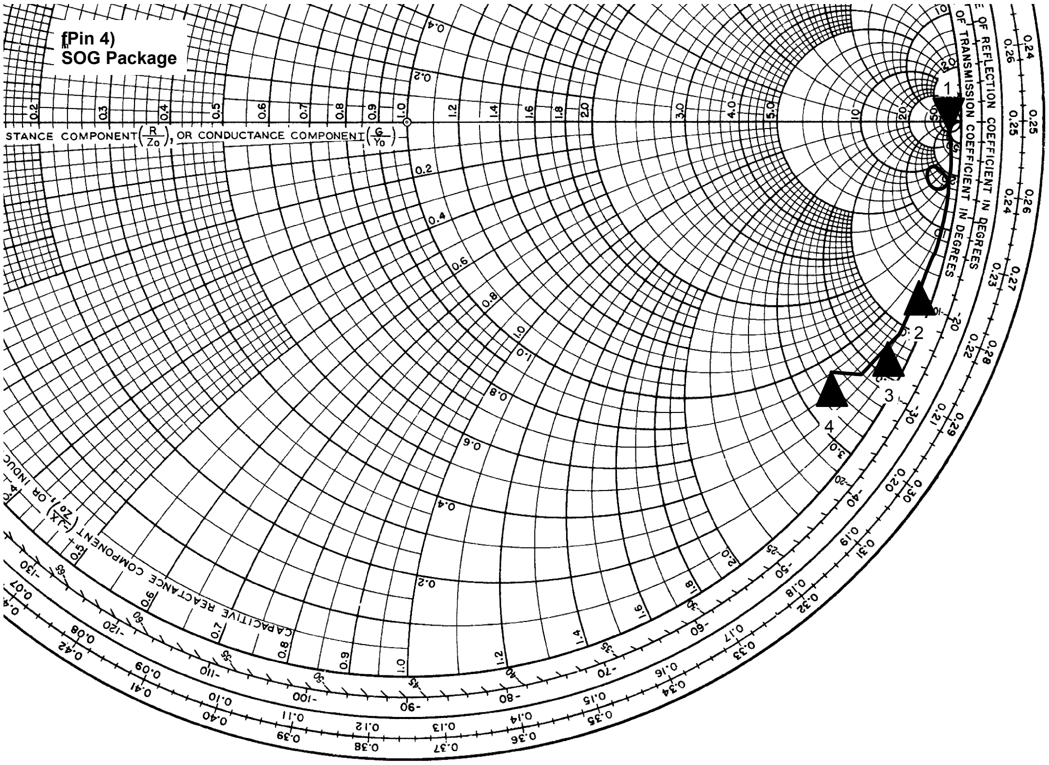
Figure 24. Example Application



NOTE:

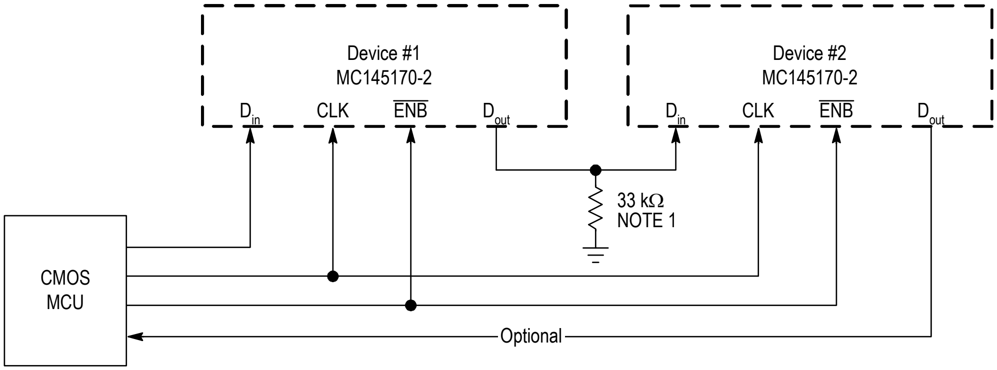
The signals at Points A and B may be low-frequency sinusoidal or square waves with slow edge rates or noisy signal edges. At Points C and D, the signals are cleaned up, have sharp edge rates, and rail-to-rail signal swings. With signals as described at Points C and D, the MC145170-2 is guaranteed to operate down to a frequency as low as dc.

Figure 25. Low Frequency Operation Using DC Coupling



Marker	Frequency (MHz)	Resistance (Ω)	Reactance (Ω)	Capacitance (pF)
1	5	2390	-5900	5.39
2	100	39.2	-347	4.58
3	150	25.8	-237	4.48
4	185	42.6	-180	4.79

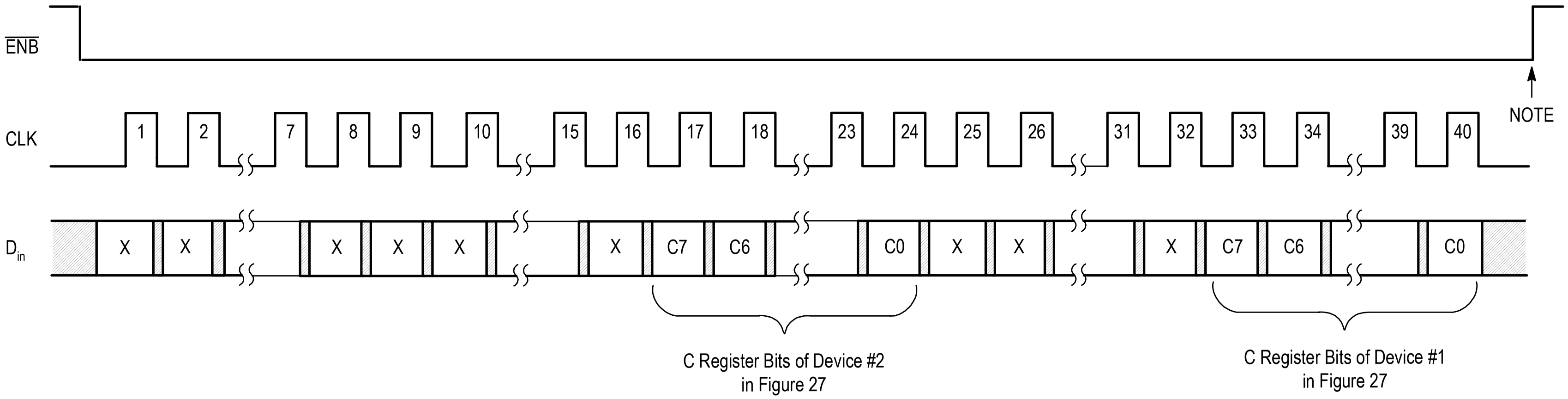
Figure 26. Input Impedance at fin - Series Format (R + jX)
(5.0 MHz to 185 MHz)



NOTES:

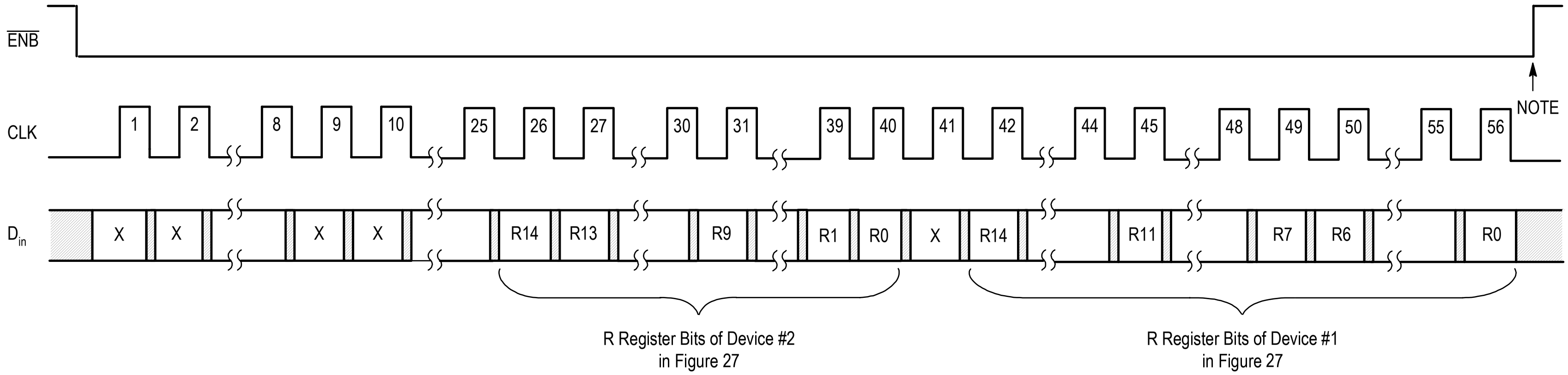
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.
2. See related Figures 28, 29, and 30.

Figure 27. Cascading Two MC145170-2 Devices



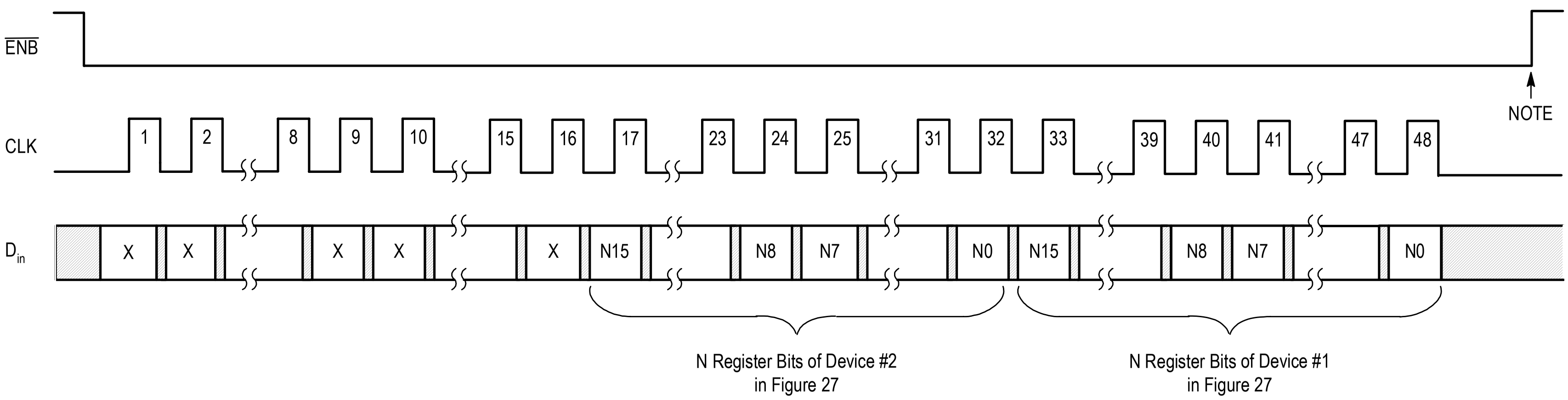
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 28. Accessing the C Registers of Two Cascaded MC145170-2 Devices



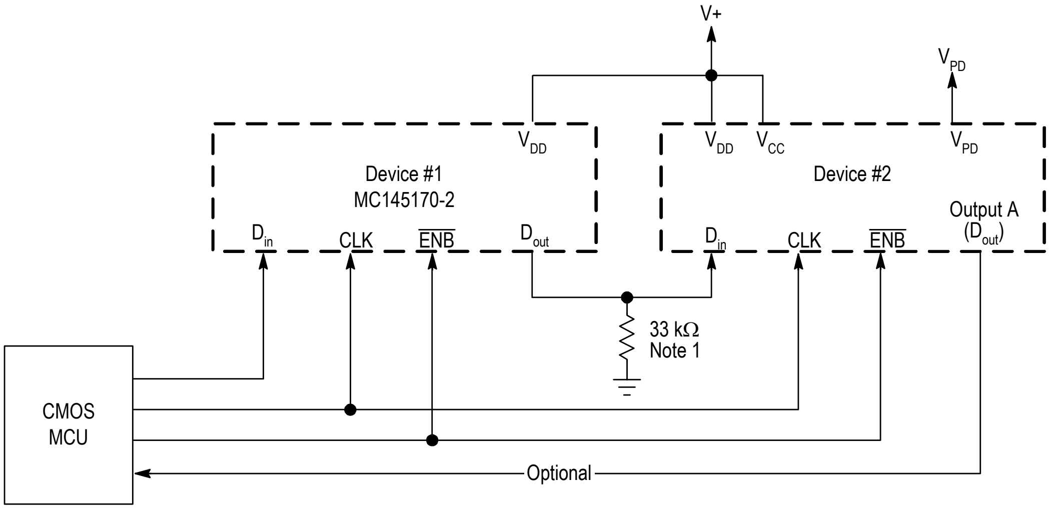
NOTE: At this point, the new data is transferred to the R registers of both devices and stored. No other registers are affected.

Figure 29. Accessing the R Registers of Two Cascaded MC145170-2 Devices



NOTE: At this point, the new data is transferred to the N registers of both devices and stored. No other registers are affected.

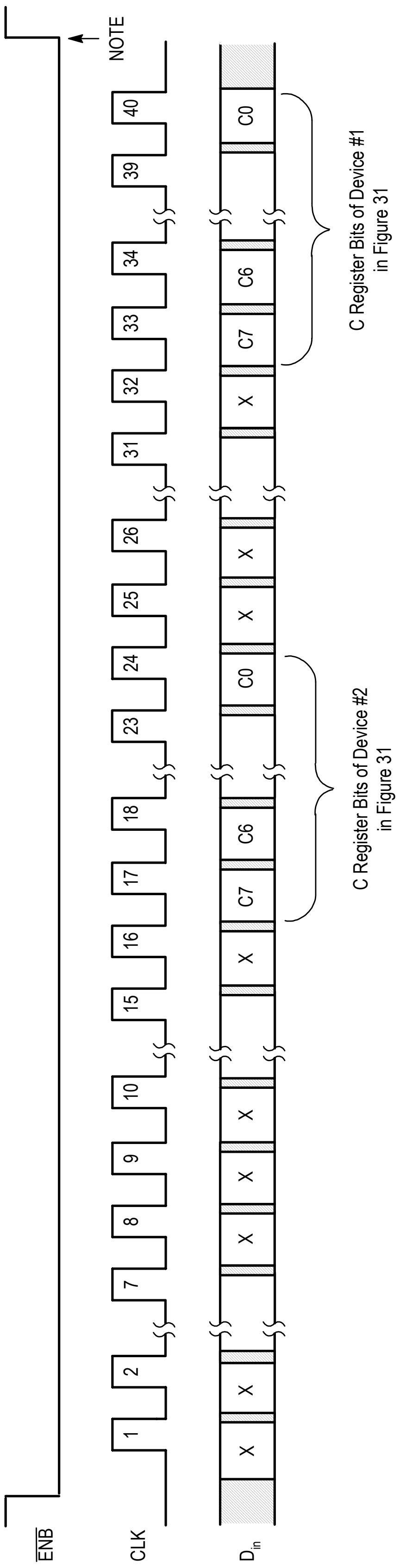
Figure 30. Accessing the N Registers of Two Cascaded MC145170-2 Devices



NOTES:

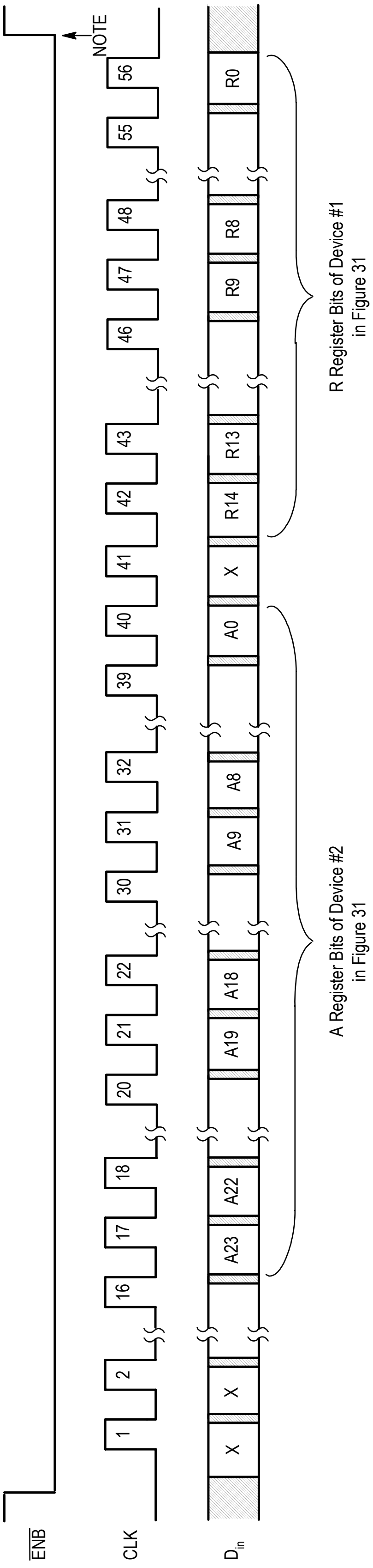
1. The 33 kΩ resistor is needed to prevent the D_{in} pin from floating. (The D_{out} pin is a three-state output.
2. See related Figures 32, 33, and 34.

Figure 31. Cascading Two Different Device Types



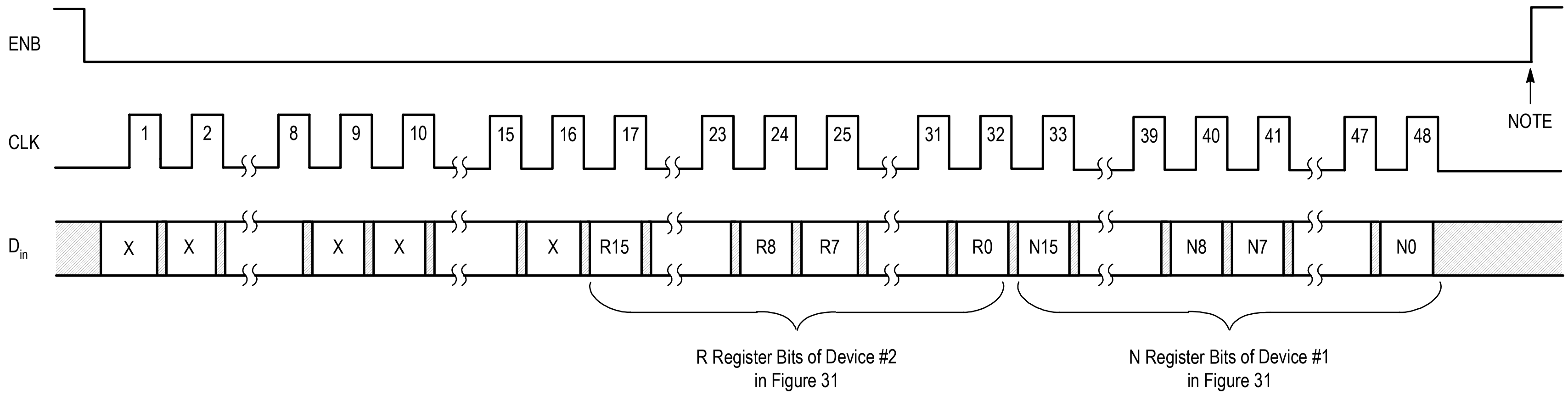
NOTE: At this point, the new data is transferred to the C registers of both devices and stored. No other registers are affected.

Figure 32. Accessing the C Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the A register of Device #2 and R register of Device #1 and stored. No other registers are affected.

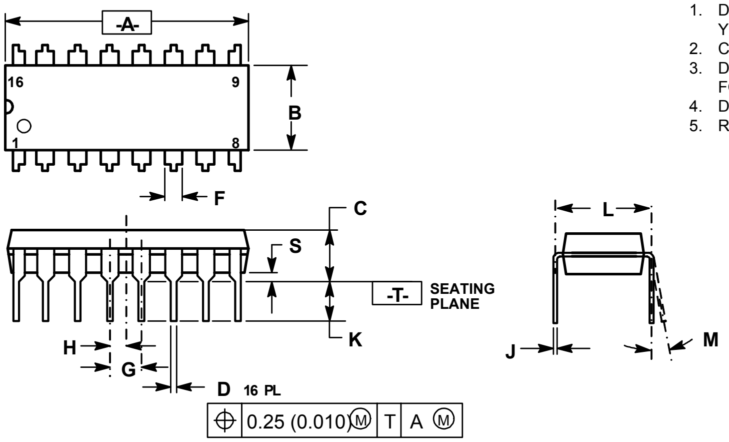
Figure 33. Accessing the A and R Registers of Two Different Device Types



NOTE: At this point, the new data is transferred to the R register of Device #2 and N register of Device #1 and stored. No other registers are affected.

Figure 34. Accessing the R and N Registers of Two Different Device Types

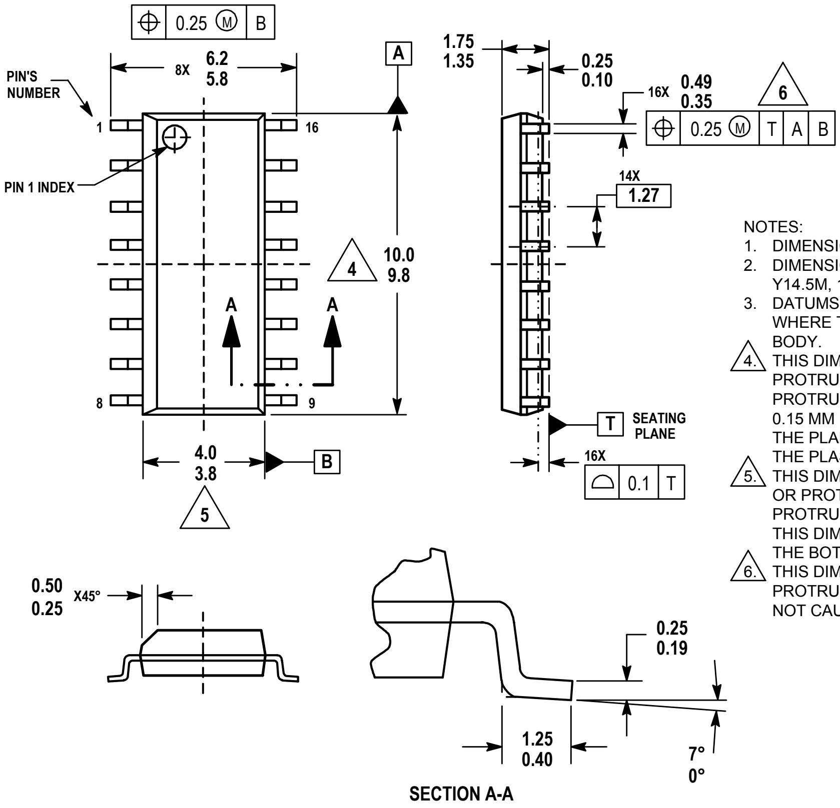
5 Packaging



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

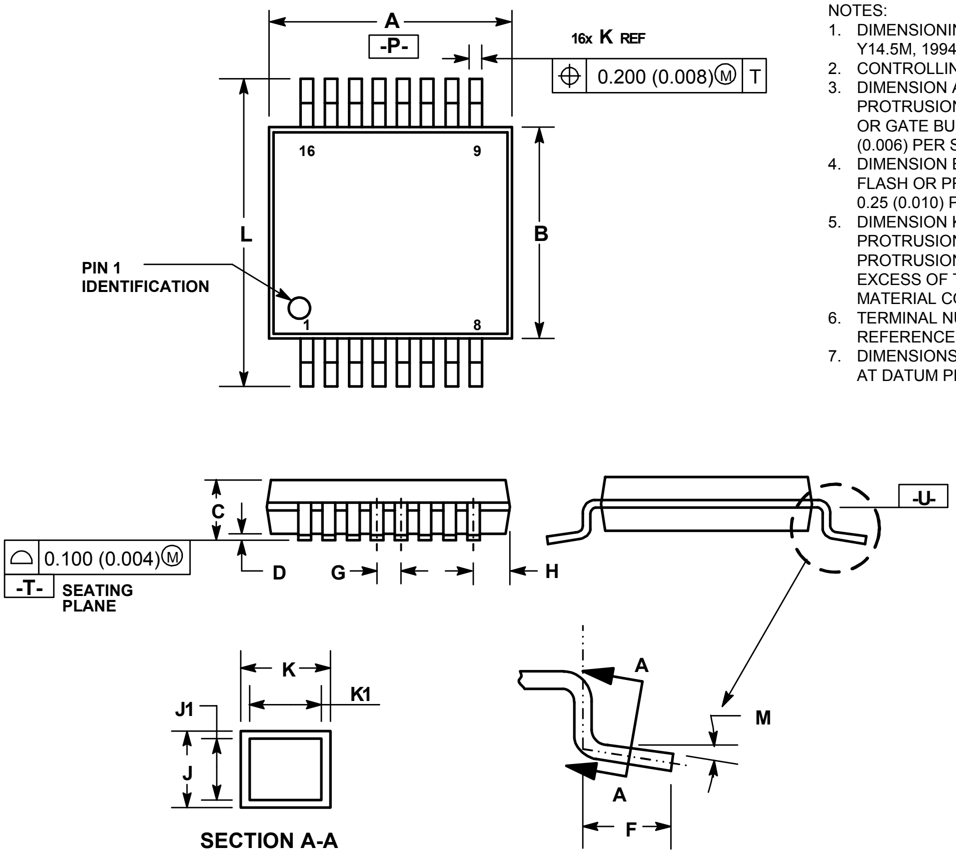
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0	10	0	10
S	0.020	0.040	0.51	1.01

Figure 35. Outline Dimensions for P Suffix, DIP-16 (Case 648-08, Issue R)



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS, MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62 MM.

Figure 36. Outline Dimensions for D Suffix, SOG-16 (Case 751B-05, Issue K)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -U-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	5.10	---	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0047
D	0.05	0.25	0.002	0.010
F	0.45	0.55	0.018	0.022
G	0.65 BSC		0.026 BSC	
H	0.22	0.23	0.009	0.010
J	0.09	0.24	0.004	0.009
J1	0.09	0.18	0.004	0.007
K	0.16	0.32	0.006	0.013
K1	0.16	0.26	0.006	0.010
L	6.30	6.50	0.248	0.256
M	0°	10°	0°	10°

Figure 37. Outline Dimensions for DT Suffix, TSSOP-16
(Case 948C-03, Issue B)

NOTES

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