# 3.3 VOLT COMMUNICATIONS CLOCK PLL

# MK2049-45A

## Description

The MK2049-45A is a dual Phase-Locked Loop (PLL) device which can provide frequency synthesis and jitter attenuation. The first PLL is VCXO based and uses a pullable crystal to track signal wander and attenuate input jitter. The second PLL is a translator for frequency multiplication. Basic configuration is determined by a Mode/Frequency Selection Table. Loop bandwidth and damping factor are programmable via external loop filter component selection.

Buffer Mode accepts a 10 to 50 MHz input and will provide a jitter attenuated output at 0.5 x ICLK, 1 x ICLK or 2 x ICLK. In this mode the MK2049-45A is ideal for filtering jitter from high frequency clocks.

In External Mode, ICLK accepts an 8 kHz clock and will produce output frequencies from a table of common communciations clock rates, CLK and CLK/2. This allows for the generation of clocks frequency-locked to an 8 kHz backplane clock, simplifying clock synchronization in communications systems.

The MK2049-45A can be dynamically switched between T1, E1, T3, E3 outputs with the same 24.576 MHz crystal.

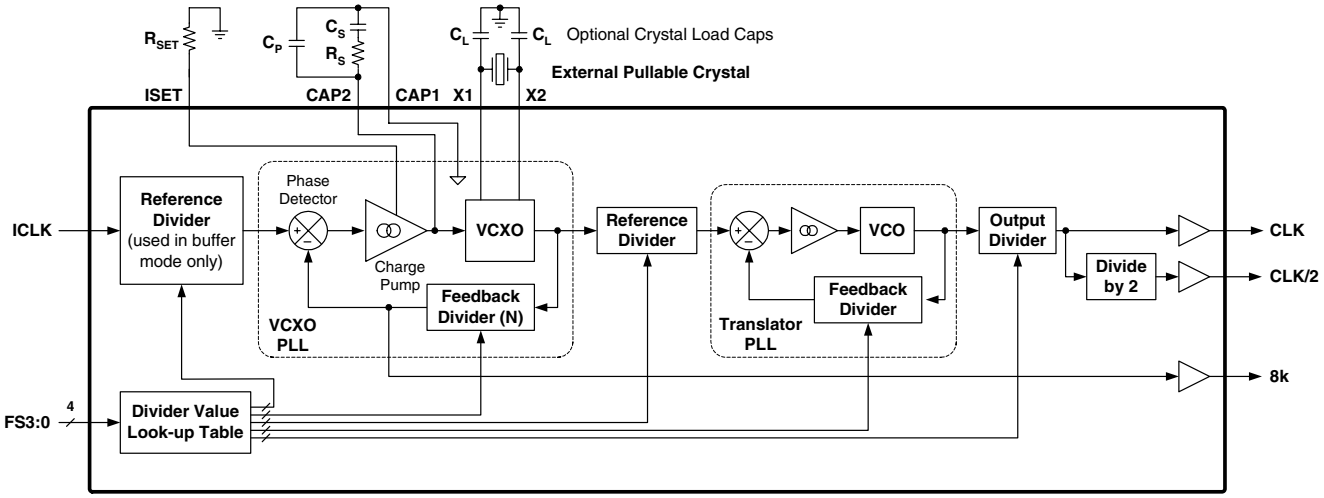
IDT can customize these devices for many other different frequencies. Contact your IDT representative for more details.

## Features

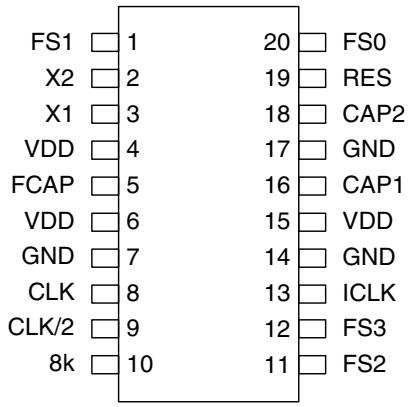
- Packaged in 20-pin SOIC
- 3.3 V ± 5% operation
- Meets the TR62411, ETS300 011, and GR-1244 specification for MTIE, Pull-in/Hold-in Range, Phase Transients, and Jitter Generation for Stratum 3, 4, and 4E
- Accepts multiple inputs: 8 kHz backplane clock, or 10 to 50 MHz
- Locks to 8 kHz ± 100 ppm (External mode)
- Buffer Mode allows jitter attenuation of 10 - 50 MHz input and x1 / x0.5 or x1 / x2 outputs
- Exact internal ratios enable zero ppm error
- Output rates include T1, E1, T3, E3, and OC3 submultiples
- Available in Pb (lead) free package
- See also the MK2049-34 and MK2049-36

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01***

## Block Diagram



## Pin Assignment




## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | FS1 | Input | Frequency select 1. Determines CLK input/outputs per table on page 2. Internal pull-up resistor. |
| 2 | X2 | Input | Crystal connection. Connect to a MHz crystal as shown in table on page 2. |
| 3 | X1 | Input | Crystal connection. Connect to a MHz crystal as shown in table on page 2. |
| 4 | VDD | Power | Power supply. Connect to +3.3 V. |
| 5 | FCAP | - | Filter capacitor. Connect a 1000 pF ceramic capacitor to ground. |
| 6 | VDD | Power | Power supply. Connect to +3.3 V. |
| 7 | GND | Power | Connect to ground |
| 8 | CLK | Output | Clock output determined by status of FS3:0 per tables on page 2. |
| 9 | CLK/2 | Output | Clock output determined by status of FS3:0 per tables page 2. Always 1/2 of CLK. |
| 10 | 8k | Output | Recovered 8 kHz clock output. |
| 11 | FS2 | Input | Frequency select 2. Determines CLK input/outputs per table on page 2. Internal pull-up resistor. |
| 12 | FS3 | Input | Frequency select 3. Determines CLK input/outputs per table on page 2. Internal pull-up resistor. |
| 13 | ICLK | Input | Input clock connection. Connect to 8 kHz backplane or MHz clock. |
| 14 | GND | Power | Connect to ground. |
| 15 | VDD | Power | Power Supply. Connect to +3.3 V. |
| 16 | CAP1 | Loop Filter | Connect the loop filter capacitors and resistor between this pin and CAP2. |
| 17 | GND | Power | Connect to ground. |

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 18 | CAP2 | Loop Filter | Connect the loop filter capacitors and resistor between this pin and CAP1. |
| 19 | RES | - | Connect a resistor to ground. See table. |
| 20 | FS0 | Input | Frequency select 0. Determines CLK input/outputs per table on page 2. Internal pull-up resistor. |

## Output Decoding Table - External Mode (MHz)

| ICLK | FS3 | FS2 | FS1 | FS0 | CLK/2 | CLK | 8k | Crystal Used (MHz) | N |
|---|---|---|---|---|---|---|---|---|---|
| 8 kHz | 0 | 0 | 0 | 0 | 1.544 | 3.088 | 8 kHz | 24.576 | 3072 |
| 8 kHz | 0 | 0 | 0 | 1 | 2.048 | 4.096 | 8 kHz | 24.576 | 3072 |
| 8 kHz | 0 | 0 | 1 | 0 | 22.368 | 44.736 | 8 kHz | 24.576 | 3072 |
| 8 kHz | 0 | 0 | 1 | 1 | 17.184 | 34.368 | 8 kHz | 24.576 | 3072 |
| 8 kHz | 0 | 1 | 0 | 0 | 19.44 | 38.88 | 8 kHz | 19.44 | 2430 |
| 8 kHz | 0 | 1 | 0 | 1 | 12.8 | 25.6 | 8 kHz | 25.6 | 3200 |
| 8 kHz | 0 | 1 | 1 | 0 | 25.92 | 51.84 | 8 kHz | 17.28 | 2160 |
| 8 kHz | 0 | 1 | 1 | 1 | 4.096 | 8.192 | 8 kHz | 16.384 | 2048 |
| 8 kHz | 1 | 0 | 0 | 0 | 18.528 | 37.056 | 8 kHz | 24.704 | 3088 |
| 8 kHz | 1 | 0 | 0 | 1 | 12.352 | 24.704 | 8 kHz | 24.704 | 3088 |
| 8 kHz | 1 | 0 | 1 | 0 | 24.576 | 49.152 | 8 kHz | 16.384 | 2048 |
| 8 kHz | 1 | 0 | 1 | 1 | 16.384 | 32.768 | 8 kHz | 16.384 | 2048 |
| 8 kHz | 1 | 1 | 0 | 0 | 17.28 | 34.56 | 8 kHz | 17.28 | 2160 |
| 8 kHz | 1 | 1 | 0 | 1 | 62.5 | 125 | 8 kHz | 25 | 3125 |

## Output Decoding Table - Buffer Mode (MHz)

| ICLK | FS3 | FS2 | FS1 | FS0 | CLK/2 | CLK | 8k | Crystal | N |
|---|---|---|---|---|---|---|---|---|---|
| 20 - 50 | 1 | 1 | 1 | 0 | ICLK | 2*ICLK | N/A | ICLK/2 | 3 |
| 10 - 25 | 1 | 1 | 1 | 1 | ICLK/2 | ICLK | N/A | ICLK | 3 |

0 = connect directly to ground, 1 = connect directly to VDD
Crystal is connected to pins 2 and 3; clock input is applied to pin 13.

## Functional Description

The MK2049-45A is a clock generator IC that generates an output clock directly from an internal VCXO circuit which works in conjunction with an external quartz crystal. The VCXO is controlled by an internal PLL (Phase Locked Loop) circuit, enabling the device to perform clock regeneration from an input reference clock. The MK2049-45A is configured to provide a high frequency communications reference clock output from an 8 kHz input clock or to jitter attenuate and buffer a high frequency input clock. There are 14 selectable output frequencies and two buffer mode selections. Please refer to the Output Clock Selection Table on Page 2.

Most typical PLL clock devices use an internal VCO (Voltage Controlled Oscillator) for output clock generation. By using a VCXO with an external crystal, the MK2049-45A is able to

generate a low jitter, low phase-noise output clock within a low bandwidth PLL. This serves to provide input clock jitter attenuation and enables stable operation with a low frequency reference clock.

The VCXO circuit requires an external pullable crystal for operation. External loop filter components enable a PLL configuration with low loop bandwidth.

# Application Information

## Output Frequency Configuration

The MK2049-45A is configured to generate a set of output frequencies from an 8 kHz input clock. Please refer to the Output Clock Selection Table on Page 2. Input bits FS3:0 are set according to this table, as is the external crystal frequency. Please refer to the Quartz Crystal section on this page regarding external crystal requirements.

## Quartz Crystal

It is important that the correct type of quartz crystal is used with the MK2049-45A. Failure to do so may result in reduced frequency pullability range, inability of the loop to lock, or excessive output phase jitter.

The MK2049-45A operates by phase-locking the VCXO circuit to the input signal of the selected ICLK input. The VCXO consists of the external crystal and the integrated VCXO oscillator circuit. To achieve the best performance and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the PCB Layout Recommendations section must be followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the external load capacitance. The MK2049-45A incorporates variable load capacitors on-chip which “pull”, or change, the frequency of the crystal. The crystals specified for use with the MK2049-45A are designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF. To achieve this, the layout should use short traces between the MK2049-45A and the crystal.

A complete description of the recommended crystal parameters in the IDT application note, MAN05.

To obtain a list of qualified crystal devices please visit our website.

## PLL Loop Filter Components

All analog PLL circuits use a loop filter to establish operating stability. The MK2049-45A uses external loop filter components for the following reasons:

1) Larger loop filter capacitor values can be used, allowing a lower loop bandwidth. This enables the use of lower input clock reference frequencies and also input clock jitter attenuation capabilities. Larger loop filter capacitors also allow higher loop damping factors when less passband peaking is desired.

2) The loop filter values can be user selected to optimize loop response characteristics for a given application.

Referencing the External Component Schematic on this page, the external loop filter is made up of components $R_S$, $C_S$ and $C_P$. $R_{SET}$ establishes PLL charge pump current and therefore influences loop filter characteristics.

Tools for optimizing the values of these four components can be found on our web site.

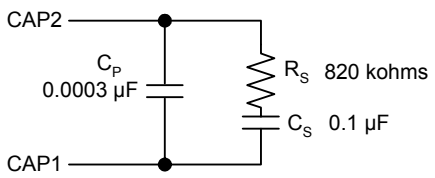



**Figure 3. Typical Loop Filter**

## Charge Pump Current Table

| $R_{SET}$ (kΩ) | Charge Pump Current ($I_{CP}$) (µA) |
|---|---|
| 13.02 | 139 |
| 15 | 125 |
| 16 | 119 |
| 18 | 109 |
| 20 | 100 |
| 22 | 93 |
| 24 | 86 |
| 27 | 68 |
| 36 | 56 |
| 47 | 43 |
| 56 | 35 |
| 75 | 28 |
| 100 | 22 |
| 150 | 15 |
| 200 | 12 |

Special considerations must be made in choosing loop components $C_S$ and $C_P$. These recommendations can be found on our web site.

### Series Termination Resistor

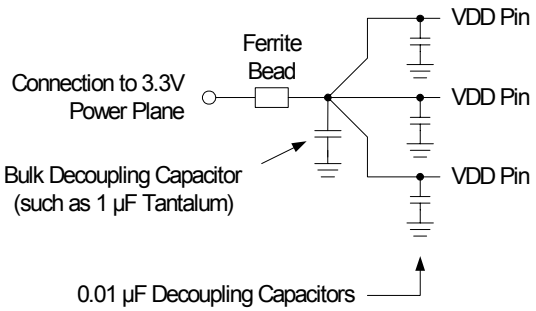
Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω (The optional series termination resistor is not shown in the External Component Schematic.)

### Decoupling Capacitors

As with any high performance mixed-signal IC, the MK2049-45A must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the MK2049-45A should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

## Recommended Power Supply Connection for Optimal Device Performance




### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground, shown as $C_L$ in the External Component Schematic. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device.

Please refer to MAN05 for the procedure to determine capacitor values.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please also refer to the Recommended PCB Layout drawing on Page 7.

1) Each 0.01 µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No via's should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The loop filter components must also be placed close to the CHGP and VIN pins. $C_P$ should be closest to the device. Coupling of noise from other system signal traces should be

minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.

3) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

4) To minimize EMI the 33 Ω series termination resistor, if needed, should be placed close to the clock output.

5) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2049-45A. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

MAN05 may also be referenced for additional suggestions on layout of the crystal section.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2049-45A. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| Supply Voltage, VDD | 7 V |
| All Inputs and Outputs | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 250° C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | -40 | | +85 | ° C |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.15 | 3.3 | 3.45 | V |
| Supply Current | IDD | Clock outputs unloaded, VDD =3.3 V | | 25 | | mA |
| Input High Voltage | $V_{IH}$ | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input High Current | $I_{IH}$ | $V_{IH}$ = VDD | -10 | | +10 | µA |
| Input Low Current | $I_{IL}$ | $V_{IL}$ = 0 | -10 | | +10 | µA |
| Input Capacitance, except X1 | $C_{IN}$ | | | 7 | | pF |
| Output High Voltage (CMOS Level) | $V_{OH}$ | $I_{OH}$ = -4 mA | VDD-0.4 | | | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -8 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8 mA | | | 0.4 | V |
| Short Circuit Current | $I_{OS}$ | | | ±50 | | mA |
| VIN, VCXO Control Voltage | $V_{XC}$ | | 0 | | VDD | V |

## AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VCXO Crystal Pull Range | $f_{XP}$ | Using Recommended Crystal | -115 | | +115 | ppm |
| Input Jitter Tolerance | $t_{ji}$ | In reference to input clock period | | | 0.4 | UI |
| Input pulse width (1) | $t_{pi}$ | | 10 | | | ns |
| Output Duty Cycle (% high time) | $t_{OD}$ | Measured at VDD/2, $C_L$=15 pF | 40 | | 60 | % |
| Output Rise Time | $t_{OR}$ | 0.8 to 2.0 V, $C_L$=15 pF | | 1.0 | | ns |
| Output Fall Time | $t_{OF}$ | 2.0 to 0.8 V, $C_L$=15 pF | | 1.0 | | ns |
| Skew, ICLK to Output Clock Note 2 | $t_{IO}$ | All output clock selections except 1.544 and 2.048 MHz | -5 | | +5 | ns |
| Timing Jitter, Filtered 500 Hz-1.3 MHz (OC-3) | $t_{jf}$ | Referenced to Mitel/Zarlink MT9045, Note 3 | | 400 | | ps |

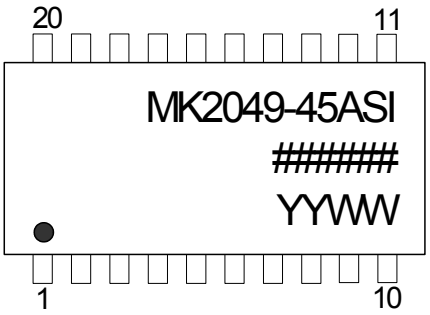
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Timing Jitter, Filtered 65 kHz-1.3 MHz (OC-3) | $t_{jf}$ | Referenced to Mitel/Zarlink MT9045, Note 3 | | 230 | | ps |
| Frequency Error | | Relative to ICLK | | 0 | | ppm |
| Nominal Output Impedance | $Z_{OUT}$ | | | 20 | | Ω |

Note 1: Minimum high or low time of input clock.

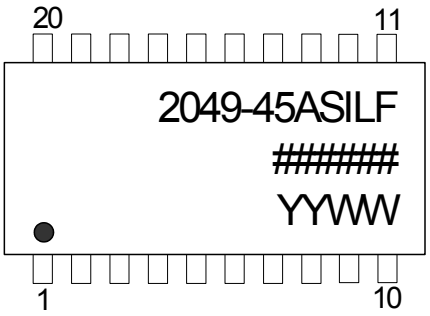
Note 2: For the 1.544 MHz and 2.048 MHz output selections, the input to output clock skew is not controlled nor predictable and will change between power up cycles. Because it is dependent on the phase relationship between the output and feedback divider states following power up, the input to output clock skew will remain stable during a given power up cycle. If controlled input to output skew is desired for this output clock frequency please refer to the MK2049 or MK2069 products.

Note 3: Input reference is the 8 kHz output from a Mitel/Zarlink MT9045 device in freerun mode (SEL2:0 = 100, 19.44 MHz external crystal).

## Marking Diagram




## Marking Diagram (Pb free)

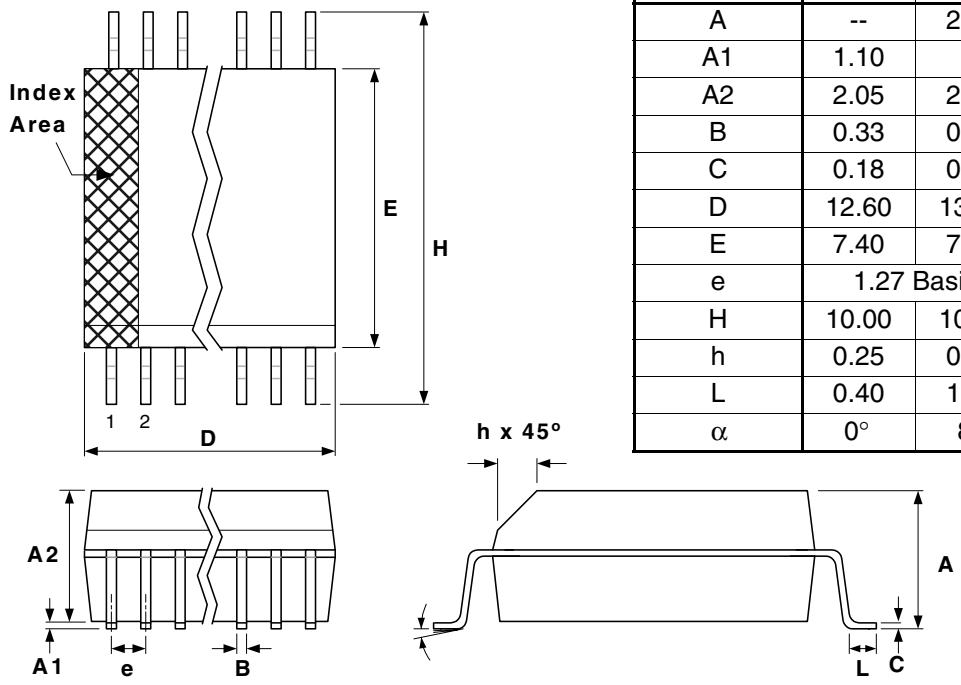



Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and the week that the part was assembled.
3. “LF” designates Pb (lead) free package.
4. Bottom marking: country of origin.

## Package Outline and Package Dimensions (20-pin SOIC, 300 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | -- | 2.65 | -- | 0.104 |
| A1 | 1.10 | -- | 0.0040 | -- |
| A2 | 2.05 | 2.55 | 0.081 | 0.100 |
| B | 0.33 | 0.51 | 0.013 | 0.020 |
| C | 0.18 | 0.32 | 0.007 | 0.013 |
| D | 12.60 | 13.00 | 0.496 | 0.512 |
| E | 7.40 | 7.60 | 0.291 | 0.299 |
| e | 1.27 Basic | | 0.050 Basic | |
| H | 10.00 | 10.65 | 0.394 | 0.419 |
| h | 0.25 | 0.75 | 0.010 | 0.029 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| MK2049-45ASI* | see page 8 | Tubes | 20-pin SOIC | -40 to +85° C |
| MK2049-45ASITR* | | Tape and Reel | 20-pin SOIC | -40 to +85° C |
| MK2049-45ASILF | | Tubes | 20-pin SOIC | -40 to +85° C |
| MK2049-45ASILFTR | | Tape and Reel | 20-pin SOIC | -40 to +85° C |

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

**Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

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