

DATA SHEET

SKY74092-11: Dual-Band LNA for CDMA, Femtocell, and PCS Mobile Handset Applications

Applications

- Femtocell systems
- Dual-band cellular handsets
- CDMA and PCS phones

Features

- Wide voltage range for both digital and analog supply voltages, 2.7 V to 3.3 V
- Cellular band IS95/IS2000 LNA with four gain steps and programmable current
- Four-step gain control for CDMA and PCS bands
- PCS band IS95/IS2000 LNA with four gain steps and programmable current
- Three-wire serial bus for device programming
- LGA (16-pin, 3 x 3 x 1 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

NEW

Skyworks offers lead (Pb)-free RoHS (Restriction of Hazardous Substances) compliant packaging.



Description

The SKY74092-11 is a dual-band Low Noise Amplifier (LNA) intended for use in Code Division Multiple Access (CDMA) portable phones in both cellular and Personal Communications Service (PCS) bands. The device provides low noise amplification with high linearity to achieve high dynamic range.

Together with Skyworks SKY74100 direct conversion receiver, the SKY74092-11 offers a cost effective, high performance RF-to-baseband radio solution. By cascading the SKY74092-11 with the SKY74100 DCR™, Printed Circuit Board (PCB) layout can easily be optimized for small areas and easy routing.

Different modes, currents, and gain steps of low noise amplification are controlled by a serial three-wire bus interface. The device requires external supply filtering capacitors, one bias resistor, and various external components to match input and output impedance to 50 Ω. The SKY74092-11 is provided in a 3 x 3 mm Land Grid Array (LGA) package.

The device package and pinout for the 16-pin LGA are shown in Figure 1 and a block diagram of the SKY74092-11 is shown in Figure 2.

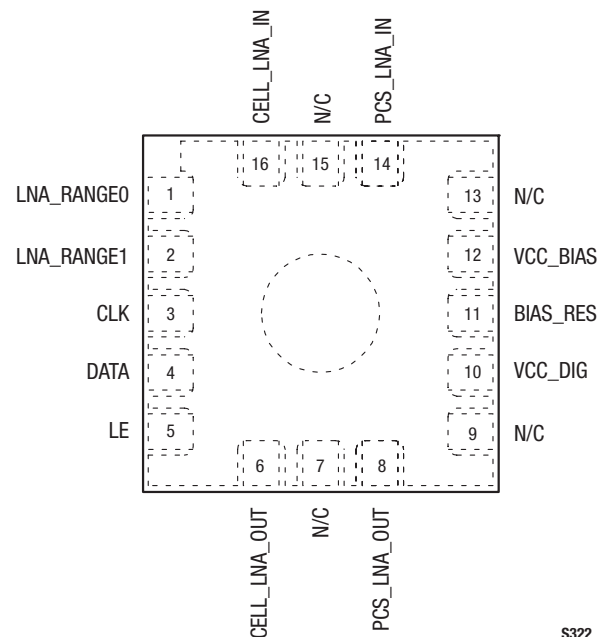


Figure 1. SKY74092-11 Pinout – 16-Pin LGA Package (Top View)

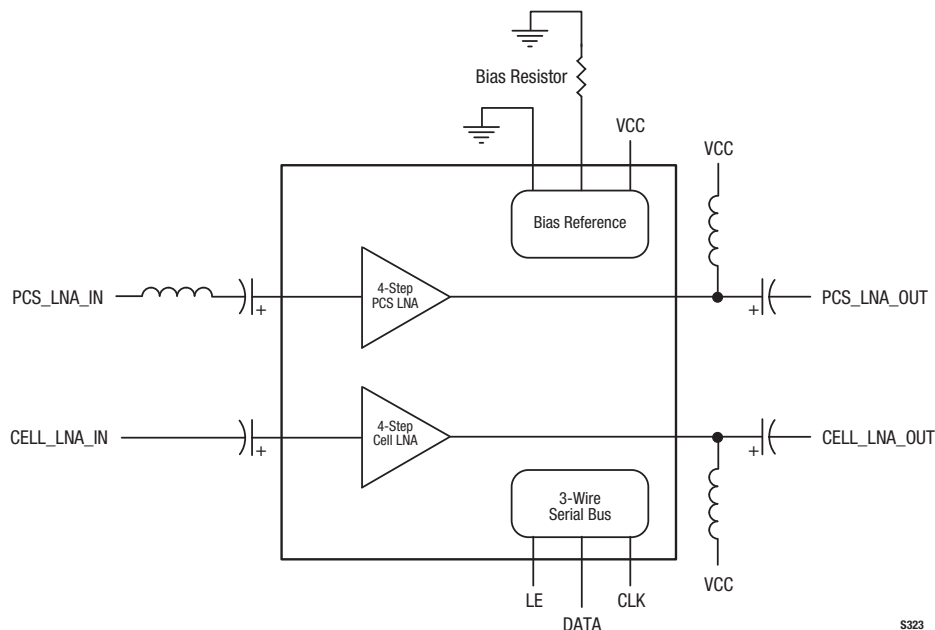


Figure 2. SKY74092-11 LNA Block Diagram

Technical Description

Bias Reference

LNA bias currents are derived from an on-chip bandgap voltage reference. The voltage reference requires a 10 k Ω external resistor.

Cellular Band LNA

The cellular band LNA requires an off-chip matching network at input and output terminals. The LNA is designed to provide a low Noise Figure (NF) and high 3rd order Input Intercept Point (IIP3) to achieve the maximum dynamic range.

The cellular LNA has four gain steps to optimize gain, linearity, and noise at various input signal levels: high gain, mid-gain, bypass, and high attenuation.

PCS Band LNA

The PCS band LNA requires an off-chip matching network at input and output terminals. The PCS LNA is designed to provide a low NF and high IIP3 to achieve the maximum dynamic range.

The PCS LNA has four gain steps to optimize gain, linearity, and noise at various input signal levels: high gain, mid-gain, bypass, and high attenuation.

Serial Interface

A three-wire serial bus is used to control the operation mode, gain, and current of the LNAs. The CLK, DATA, and LE signals

(pins 3, 4, and 5, respectively) provide the control inputs. The SKY74092-11 provides the following control and test registers:

- Mode Selection
- Gain Control
- Current Selection

The SKY74092-11 supports two types of fixed-length data transfers: 9-bit and 27-bit. Data is latched starting from the second high-to-low transition on the CLK signal after LE goes low. The first high-to-low transition of the CLK signal is ignored.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY74100 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for RFLGA Packages*, document number 103147.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Electrical and Mechanical Specifications

Signal pin assignments and functional pin descriptions are described in Table 1. The absolute maximum ratings of the SKY74092-11 are provided in Table 2. The recommended operating conditions are specified in Table 3 and electrical specifications are provided in Tables 4 and 5. Tables 6 through 8 provide the control logic for the SKY74092-11.

An application schematic diagram for the SKY74092-11 is shown in Figure 3. The package dimensions for the 16-pin LGA are shown in Figure 4, and the tape and reel dimensions are provided in Figure 5.

Table 1. SKY74092-11 Pin Assignments and Signal Descriptions

Pin #	Name	Description
1	LNA_RANGE0	LNA gain control input (bit 0). Hardware control disabled. Needs to be grounded with software control.
2	LNA_RANGE1	LNA gain control input (bit 1). Hardware control disabled. Needs to be grounded with software control.
3	CLK	Clock for the three-wire bus
4	DATA	Data for the three-wire bus
5	LE	Latch enable for the three-wire bus
6	CELL_LNA_OUT	Externally matched cellular LNA output
7	N/C	No connection
8	PCS_LNA_OUT	Externally matched PCS LNA output
9	N/C	No connection
10	VCC_DIG	Supply voltage for digital circuitry
11	BIAS_RES	External 10 k Ω bias resistor
12	VCC_BIAS	Supply voltage for bias circuitry
13	N/C	No connection
14	PCS_LNA_IN	Externally matched PCS LNA input
15	N/C	No connection
16	CELL_LNA_IN	Externally matched cellular LNA input

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	VDD	0		5.0	V
DC voltage at control ports	V _{CNTL}	0		0.3 + VDD	V
Power into LNA inputs	P _{IN} , LNA			-5.0	dBm
Operating temperature	T _A	-30		+85	°C
Storage temperature	T _{STG}	-40		+125	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal values.

CAUTION: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. With the exception of the input pins, the SKY74092-11 ESD threshold level, with respect to ground, is ± 2.0 kV using Human Body Model (HBM) testing. The HBM ESD withstand threshold value for input pins is 900 V.

Table 3. Recommended Operating Conditions (@ +25 °C, VCC = 2.85 V)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage		2.7	2.85	3.3	V
RF frequency range (cellular band)		869		894	MHz
RF frequency range (PCS)		1930		1990	MHz
Operating temperature range		–30	+25	+85	°C

Table 4. Electrical Characteristics: Cellular LNA Mode Settings (869-894 MHz) (Note 1)
(TA = +25 °C, VCC = 2.85 V, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
LNA High Gain						
Gain			15	16	16.8	dB
Noise Figure				1.2	1.5	dB
IIP3			7.5	9.0		dBm
1 dB compression point at input			–8	–7		dBm
Input/output return loss (Note 2)	Zs/L = 50 Ω			–12	–10	dB
Reverse isolation			20	21		dB
Current			8	9	12	mA
LNA Mid-Gain						
Gain			6.5	7.5	8.5	dB
Noise Figure				4.2	5.2	dB
IIP3			9.5	11		dBm
1 dB compression point at input			–2	–1		dBm
Input/output return loss (Note 2)	Zs/L = 50 Ω			–10	–8	dB
Reverse isolation			15	16		dB
Current			6	8	10	mA
LNA Bypass						
Gain			–4	–3	–2	dB
Noise Figure				3	4	dB
IIP3			18.5	20.0		dBm
1 dB compression point at input			2.5	3.5		dBm
Input/output return loss (Note 2)	Zs/L = 50 Ω			–8	–7	dB
Reverse isolation			2	3		dB
Current				200	240	μA
LNA High Attenuation						
Gain			–18	–17	–16	dB
Noise Figure				17	18	dB
IIP3			20.5	22.0		dBm
1 dB compression point at input			4	5		dBm
Input/output return loss (Note 2)	Zs/L = 50 Ω			–12	–10	dB
Reverse isolation			16	17		dB
Current				200	240	μA

Note 1: Performance is guaranteed only under the conditions listed in this Table.**Note 2:** Input and output externally matched to 50 Ω.

Table 5. Electrical Characteristics: PCS LNA Mode Settings (1930-1990 MHz) (Note 1)
(T_A = +25 °C, V_{CC} = 2.85 V, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
LNA High Gain						
Gain			15	16	16.8	dB
Noise Figure				1.3	1.6	dB
IIP3			7.0	8.5		dBm
1 dB compression point at input			−12.0	−10.5		dBm
Input/output return loss (Note 2)	Z _{S/L} = 50 Ω			−11.5	−10.0	dB
Reverse isolation			20.0	21.5		dB
Current			9.0	11.1	13.0	mA
LNA Mid-Gain						
Gain			6.0	7.0	7.8	dB
Noise Figure				4.3	5.3	dB
IIP3			7.5	9.0		dBm
1 dB compression point at input			−4.5	−3.0		dBm
Input/output return loss (Note 2)	Z _{S/L} = 50 Ω			−7	−6	dB
Reverse isolation			14.0	15.5		dB
Current			7.0	8.5	11	mA
LNA Bypass						
Gain			−5	−4	−3	dB
Noise Figure				4	5	dB
IIP3			20.5	22.0		dBm
1 dB compression point at input			3.0	4.5		dBm
Input/output return loss (Note 2)	Z _{S/L} = 50 Ω			−10	−8	dB
Reverse isolation			3	4		
Current				200	240	μA
LNA High Attenuation						
Gain			−18	−17	−16	dB
Noise Figure				17	18	dB
IIP3			23.5	25.0		dBm
1 dB compression point at input			4	5		dBm
Input/output return loss (Note 2)	Z _{S/L} = 50 Ω			−9	−7	dB
Reverse isolation			16	17		dB
Current				200	240	μA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: Input and output externally matched to 50 Ω.

Table 6. Mode Selection Register

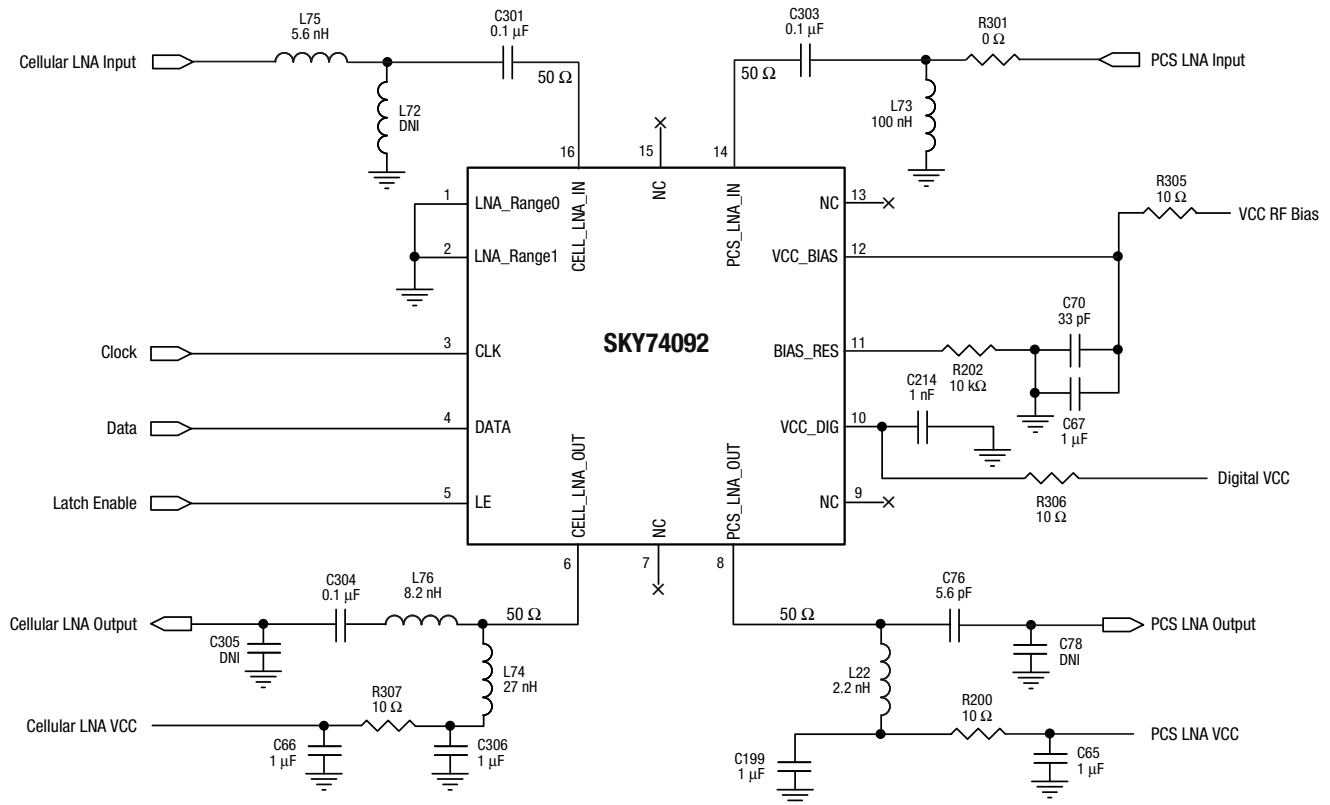
Bit Range	Description
[2:0]	Bits [2:0]: Not configurable – must be set to 1 1 1
[4:3]	Bits [4:3]: LNA mode control 0 0 = Cellular mode 0 1 = Not used 1 0 = Not used 1 1 = PCS mode
[7:5]	Bits [7:5]: Not configurable – must be set to 1 0 0
[8]	Bit [8]: LNA enable 0 = LNA off 1 = LNA on
[26:9]	Bits [26:9]: Not configurable – must be set to 0 1 0 0 0 1 0 1 1 0 0 0 0 0 1 0 0

Table 7. Gain Control Register

Bit Range	Description
[3:0]	Bits [3:0]: Not configurable – must be set to 0 0 0 0
[5:4]	Bits [5:4]: LNA gain control: 0 0 = High gain 0 1 = Mid-gain 1 0 = Bypass 1 1 = High attenuation
[8:6]	Bits [8:6]: Not configurable – must be set to 0 0 1

Table 8. Current Selection Register

Bit Range	Description
[0]	Bit [0]: Not configurable – must be set to 1
[3:1]	Bits [3:1]: CDMA LNA current selection (high gain setting only) 0 0 0 = 5.862 mA 1 0 0 = 10.944 mA 0 0 1 = 7.159 mA 1 0 1 = 12.246 mA 0 1 0 = 8.427 mA 1 1 0 = 13.503 mA 0 1 1 = 9.735 mA 1 1 1 = 14.795 mA Note that the current can also be adjusted with the external bias resistor.
[6:4]	Bits [6:4]: PCS LNA current selection (high gain setting only) 0 0 0 = 5.590 mA 1 0 0 = 11.030 mA 0 0 1 = 6.990 mA 1 0 1 = 12.146 mA 0 1 0 = 8.360 mA 1 1 0 = 12.749 mA 0 1 1 = 9.736 mA 1 1 1 = 13.098 mA Note that the current can also be adjusted with the external bias resistor.
[26:7]	Bits [26:7]: Not configurable – must be set to 0 1 0 0 0 1 0 1 1 0 0 0 0 0 1 0 1 0 0 1



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Figure 3. SKY74092-11 Schematic Diagram

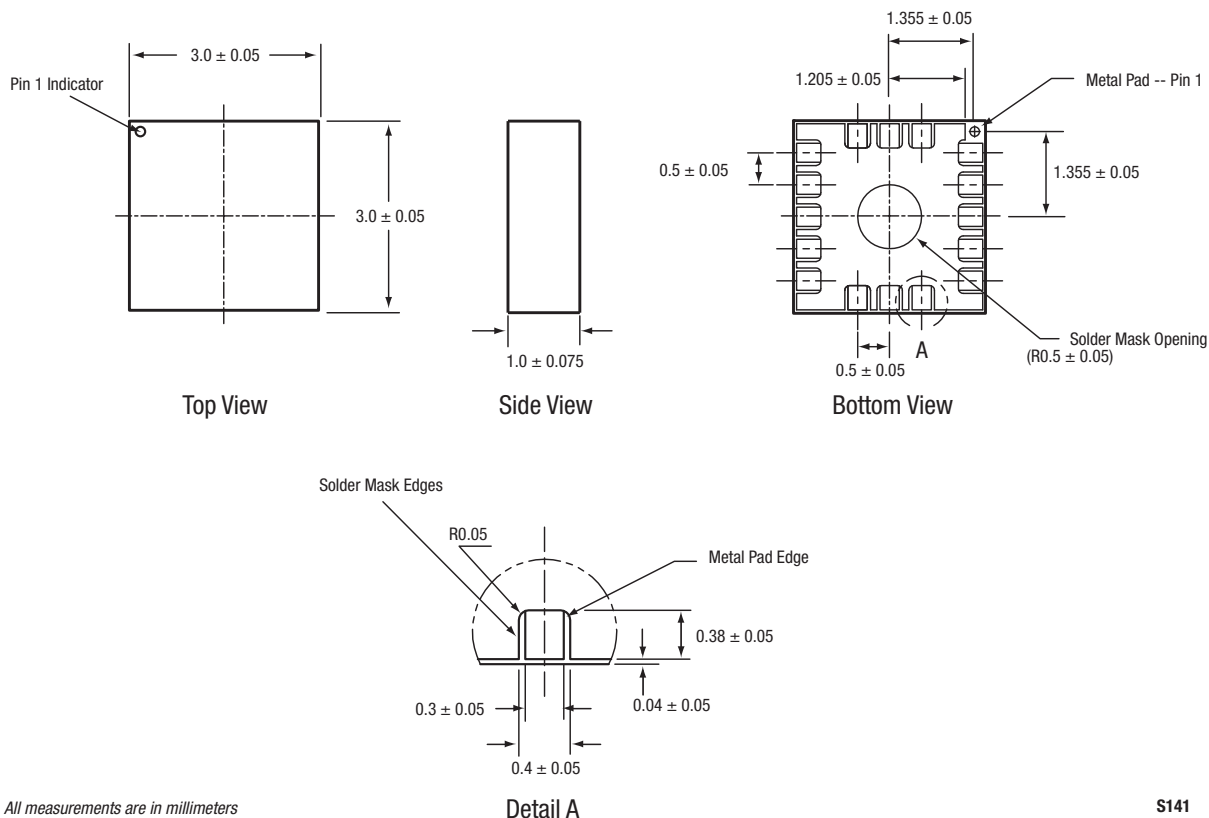


Figure 4. SKY74092-11 16-Pin LGA Package Dimensions

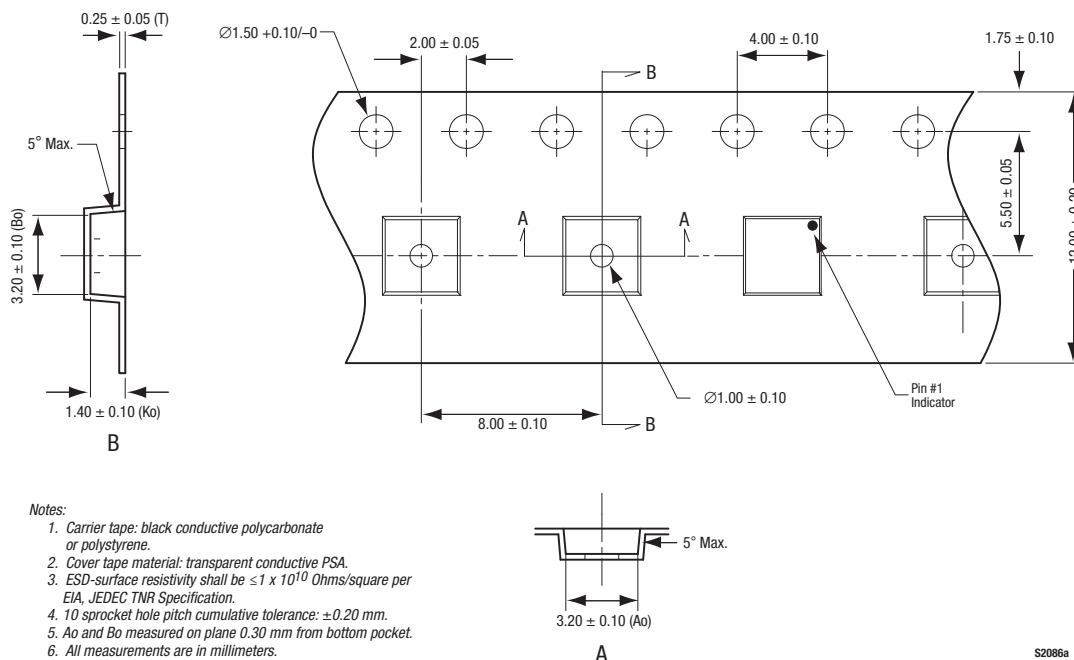


Figure 5. SKY74092-11 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY74092-11 LNA	SKY74092-11	*** TBD ***

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