PRELIMINARY DATA SHEET

SKY73134-11: Wideband PLL Frequency Synthesizer

Applications

- Cellular base station systems: GSM/EDGE, CDMA2000, WCDMA, TD-SCDMA, LTE
- Other wireless communication systems

Features

- Output frequency range: 0.35 to 6.0 GHz
- Integer-N frequency synthesizer
- Low phase noise VCO
- Four integrated VCOs with automatic digital frequency calibration
- Automatic VCO selection based on the target RF output
- Programmable VCO division by 1, 2, 3, 4, or 8
- VCO divide-by-three with 50% duty cycle
- Integrated input/output RF buffer
- Device provides both divided and direct VCO outputs
- Programmable RF output power levels
- Low RF output comparison spurs
- Programmable 18-bit N-counter and 11-bit R-counter
- Dual modulus 7 GHz prescaler (selectable 64/65 or 32/33)
- Programmable charge pump current
- Flexible configuration allows connection to external VCO or PLL
- Bidirectional read/write three-wire serial to parallel interface
- Digital lock detect
- Digital output used as a loop filter component switch
- Optional adjustment of the core, divider, and charge pump current by external resistor
- Power supply: 3.3 V
- Small, RFLGA (32-pin, 5 x 5 mm) package (MSL3, 260 °C per JEDEC J-STD-020)

NEW

Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances) compliant packaging.

Description

The SKY73134-11 is a wideband integer-N frequency synthesizer with an approximately 6 GHz locking range.

The device includes four differential Voltage Controlled Oscillators (VCOs), which cover the output frequency range from 2.8 GHz to 6.0 GHz. By applying internal VCO division by 1, 2, 3, 4, or 8, the output frequency range can be increased from 0.35 GHz to 6.0 GHz, monitored at the RF output.

The direct, non-divided internal VCO frequency can also be monitored at the bidirectional VCO pins. The VCO selection can be automatic based on the target RF output. The flexible SKY73134-11 configuration allows the loop to be locked by an external VCO or external Phase Locked Loop (PLL), or the device can use the divider chain only. The SKY73134-11 is controlled by a bidirectional read/write serial to parallel interface.

The SKY73134-11 frequency synthesizer is manufactured with a BiCMOS 0.18 µm SiGe process and provided in a compact, 32-pin RF Land Grid Array (RFLGA). The pin configuration and package are shown in Figure 1. A functional block diagram is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

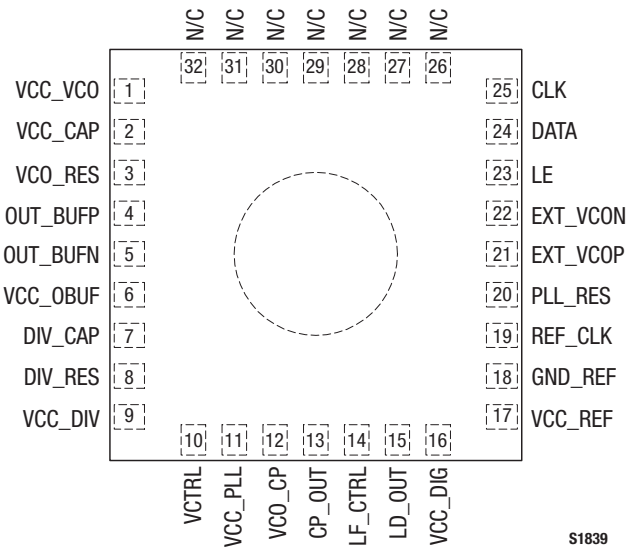


Figure 1. SKY73134-11 Pinout – 32-Pin RFLGA (Top View)

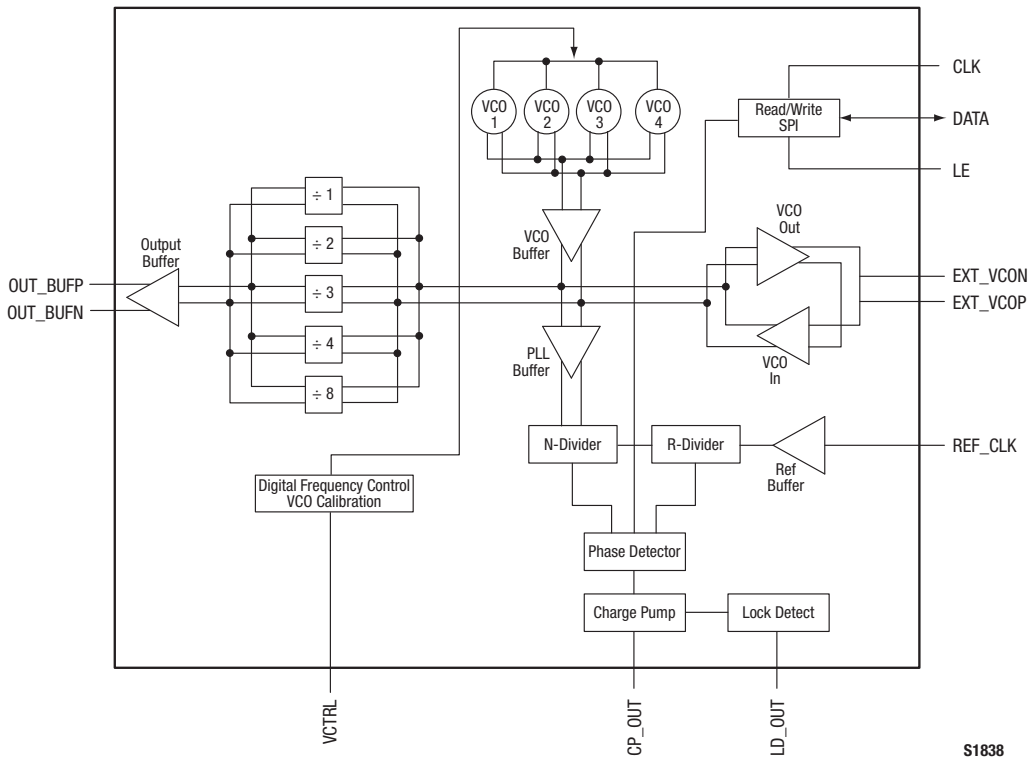


Figure 2. SKY73134-11 Block Diagram

Table 1. SKY73134-11 Signal Descriptions

Pin #	Name	Description	Pin #	Name	Description
1	VCC_VCO	Supply for VCO	17	VCC_REF	Supply for reference buffer
2	VCC_CAP	External capacitor for VCO bias connected to VCC_VCO pin	18	GND_REF	Reference buffer ground
3	VCO_RES	External 15 kΩ resistor to set VCO bias	19	REF_CLK	Reference clock input
4	OUT_BUFP	Positive LO output	20	PLL_RES	External 24 kΩ resistor for the PLL/charge pump bias
5	OUT_BUFN	Negative LO output	21	EXT_VCOP	Positive, external VCO input
6	VCC_OBUF	Supply for output buffer	22	EXT_VCON	Negative, external VCO input
7	DIV_CAP	External capacitor for the divider bias connected to the VCC_DIV pin	23	LE	Latch enable input for the SPI
8	DIV_RES	External 60 kΩ resistor to set the divider bias	24	DATA	Data input for the SPI
9	VCC_DIV	Supply for dividers	25	CLK	Clock input for the SPI
10	VCTRL	VCO tuning voltage	26	N/C	No connection
11	VCC_PLL	PLL supply	27	N/C	No connection
12	VCC_CP	Supply for charge pump	28	N/C	No connection
13	CP_OUT	Charge pump output	29	N/C	No connection
14	LF_CTRL	Loop filter component switch control	30	N/C	No connection
15	LD_OUT	Lock detect output	31	N/C	No connection
16	VCC_DIG	Supply for digital blocks	32	N/C	No connection

Functional Description

The SKY73134-11 is comprised of seven main functional blocks:

1. N-divider
2. R-divider
3. Phase detector
4. Charge pump
5. VCO and digital frequency VCO calibration
6. VCO dividers
7. Lock detect

N-Divider

The N-divider consists of a selectable 32/33 prescaler, 13-bit main counter, and 5-bit swallow counter. The 18-bit N-divider ratio is calculated as:

$$N = P \times M + S$$

Where: P = Prescaler value
M = Main counter value
S = Swallow counter value

The N-divider range is from P^2 to 2^{18}, or it can vary from 1024 to 262144. For the 4 GHz VCO output, the minimum and maximum comparison frequency are defined as:

$$F_{COMP\_MIN} = VCO/N_{MAX} = 4\ GHz/2^{18} \approx 15\ kHz$$

$$F_{COMP\_MAX} = VCO/N_{MIN} = 4\ GHz/2^{10} \approx 3.906\ MHz$$

R-Divider

The 11-bit programmable R-divider divides the reference input frequency and generates the reference input for the phase detector. The R-divider range varies from 1 to 2^{11} (2048).

Since $F_{COMP} = F_{REF}/R\text{-}divider$ for a comparison frequency of 100 kHz, the maximum reference frequency could be 204.8 MHz.

Phase Detector

The phase detector is an edge-controlled digital circuit. The circuit has two inputs: the reference signal (*Ref*) and the N-divider output. There are two digital outputs (*Up* and *Dn*) that drive the charge pump.

When the input phase difference is positive, the *Up* output is pulled up to VDD. When the input phase difference is negative, the *Dn* output is pulled down to ground. This type of phase detector acts only on the positive edges of the input signals.

Charge Pump

The charge pump is used to convert the logic levels of the *Up* and *Dn* pulses, carrying the phase error between the reference and the divided signal into analog quantities/current pulses.

The output of the SKY73134-11 charge pump is programmable and varies between 0.9 mA and 5.4 mA. Additional adjustment of the charge pump current can be accomplished by changing the value of the external PLL bias resistor.

VCO and Digital Frequency VCO Calibration

The SKY73134-11 incorporates four VCOs. Each VCO covers a different frequency range between 2.8 and 6.0 GHz:

- VCO 1: 2.8 to 3.4 GHz
- VCO 2: 3.3 to 4.2 GHz
- VCO 3: 3.8 to 4.8 GHz
- VCO 4: 4.7 to 6.0 GHz

The VCOs are designed to generate the LO signal with the tuning function controlled by the synthesizer. Each VCO uses a switch capacitor array and an analog varactor for digital tuning. The digital auto-tuning loop provides the proper 7-bit coarse tuning setting for the VCO switch capacitors. This sets the oscillation frequency as close to target as possible before starting fine analog tuning.

When VCO auto-tuning is enabled, the PLL performs a seven-step successive approximation process to digitally tune the VCO close to the final programmed frequency. Once that is complete, analog tuning is enabled to lock the VCO to the programmed frequency.

The auto-tuning loop is designed to compensate process variation so that the VCO fine tuning range can be reduced to cover temperature variation only. It significantly reduces VCO gain (Kv), which reduces the VCO phase noise. This ensures that the PLL is always locked.

VCO Dividers

The divider chain consists of dividers and LO drivers. Any VCO can be divided by 2, 3, 4, or 8, which improves the LO phase noise by 6 dB, 9.5 dB, 12 dB, and 18 dB, respectively.

Using frequency division, the overall VCO range of the device is widened from 0.35 to 6.0 GHz.

The output RF buffer has a programmable current that provides variation in the output RF level from –4 to +4 dBm. The direct non-divided VCO output can be monitored at the additional bidirectional internal/external VCO pins. The divider chain and the internal PLL can be locked by an external VCO.

Lock Detect

The lock detect circuit is activated when the phase difference between the *Up* and *Dn* phase detector signals for a given number of comparison cycles is shorter than a fixed delay. The CMOS output is active high when the loop is locked.

Bidirectional Digital Interface

A three-wire Serial Programmable Interface (SPI) with read/write capability provides mode and bias control, and control of the PLL. The serial interface consists of three signals: the bus clock (CLK), latch enable (LE), and the serial, bidirectional data line (DATA).

Write Mode. A write data stream consists of 25 bits:

Bits[15:0] provide the 16-bit data block.

Bits[20:16] provide the register address.

Bit[21] is the read/write bit (0 = read, 1 = write).

Bits[24:22] provide the device address (the SKY73134-11 is 011b).

Read Mode. The read data stream is almost identical to the write data stream. Following the 5-bit register address, a “turn around” cycle is inserted so the baseband can disable its drive of the data line and the addressed device on the bus can activate its data output driver.

When the baseband addresses a device connected to the serial bus, the bus enable signal (LE) goes low half a clock cycle before the CLK signal becomes active. Data on the DATA line is clocked into the SKY73134-11 on the rising edge of the clock.

Data from the SKY73134-11 to the baseband is clocked at the falling edge of the clock. The enable line goes high at the end of the data transfer. The clock becomes inactive one clock pulse after the enable signal goes high. The CLK signal is always disabled for at least one equivalent cycle between subsequent accesses.

A timing diagram for the SPI read/write cycle is shown in Figure 3.

Serial Bus Timing

The SPI bus speed is programmable. Timing requirements for the CLK, DATA, and LE signals are provided in Table 2. A serial data input timing diagram is shown in Figure 4.

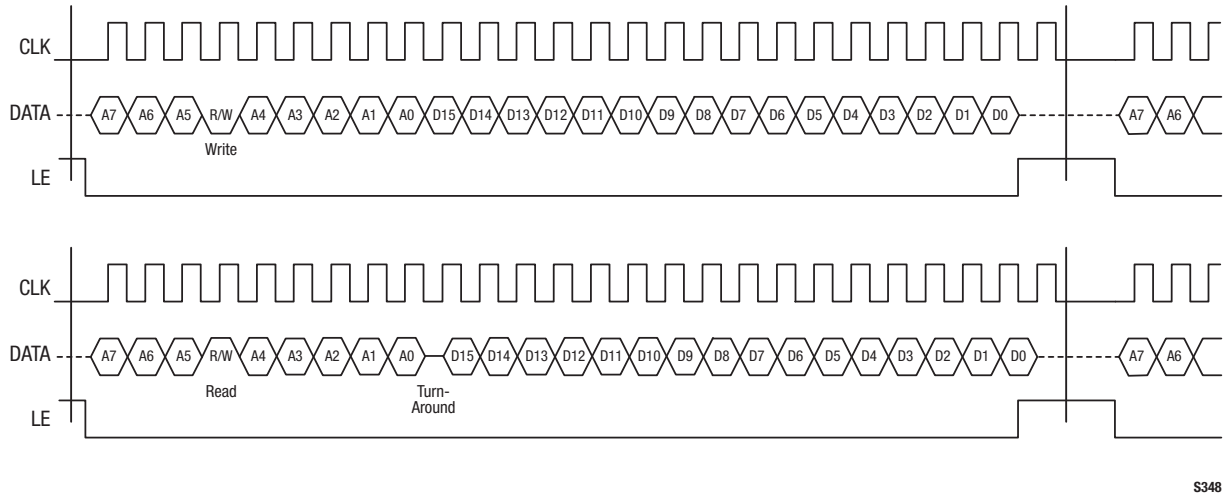


Figure 3. Read/Write SPI Cycles

Table 2. SPI Timing Requirements

Parameter	Description	Minimum Time (ns)
t_{period}	Clock period	25
t_{high}	Clock high time	10
t_{su}	Data setup to clock rise	5
t_{hld}	Data hold from clock rise	5
t_{es}(a)	Clock rise to enable high	10
t_{es}(b)	Enable high to clock high	10
t_{el}(a)	Enable to clock rise	10
t_{width}	Enable high width	20
t_{es}(c)	Clock fall to enable high	0
t_{el}(b)	Clock rise to enable low	10

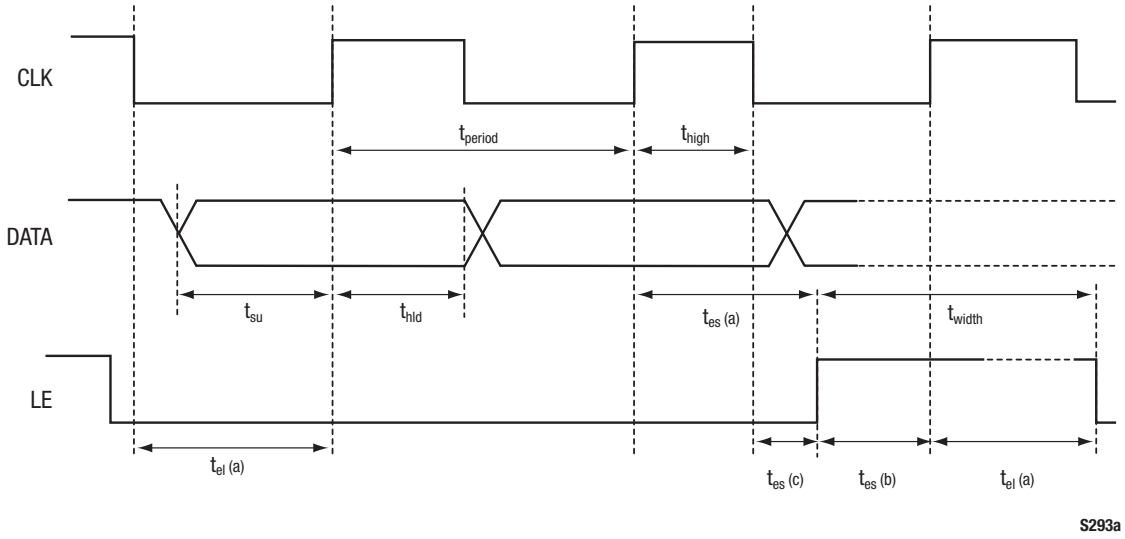


Figure 4. SPI Timing Diagram

PLL Control Registers (R-Divider and N-Divider)

There are three digital PLL control registers that are used to store the R-divider and N-divider values: R_DIV, N_DIV1, and N_DIV2. By default, all registers are 25 bits wide. Bit[21] is the read/write bit, cleared when writing to the device. Bits[20:16] are the address bits of the registers. The 16 least significant bits (LSBs) represent the data bits.

Three values are needed to calculate the three PLL dividers, R_DIV, N_DIV1 and N_DIV2: the desired frequency (F_{RF}), the VCO divider (D), and the frequency step size (F_{STEP}).

The VCO frequency (F_{VCO}) has a range of 2.8 GHz to 6.0 GHz, and is defined by the product of the desired frequency (F_{RF}) and the VCO divider, D:

$$F_{VCO} = F_{RF} \times D \quad (1)$$

The VCO divider (equal to 1, 2, 3, 4, or 8) is chosen so that the product of $F_{RF} \times D$ is within the specified VCO range.

The frequency step size (F_{STEP}) is a user defined value. Given F_{STEP} and D, the comparison frequency (F_{COMP}) can be calculated by:

$$F_{COMP} = F_{STEP} \times D \quad (2)$$

The R_DIV register stores the value of the 11-bit R-divider that produces the desired comparison frequency (F_{COMP}) for the RF PLL according to the following equation:

$$R = \frac{F_{REF}}{F_{COMP}} \quad (3)$$

Where F_{REF} is the reference frequency provided to the device.

The N_DIV1 and N_DIV2 registers store the value of the N-divider according to the following equation:

$$N = \frac{F_{VCO}}{F_{REF}} \times R \quad (4)$$

Bits[1:0] of the N_DIV2 register are the most significant bits (MSBs) of the 18-bit representation of the N number.

Bits[15:0] of the N_DIV1 register are the LSBs of the 18-bit binary representation of the N number.

The calculated R-divider and N-divider values are programmed into the SKY73134-11 using the SPI interface.

Additional programming information is provided in the document, *Skyworks Wideband Integer-N, Phase-Locked Loop Programming Guide*, document number 201322.

Example:

A desired RF output frequency of 2000 MHz is required using a reference frequency of 38.4 MHz and a desired frequency step size of 100 kHz. If the VCO divider is equal to 2, the VCO frequency is 4000 MHz from Equation 1 and the comparison frequency is equal to 200 kHz from Equation 2.

From Equations 3 and 4, the R and N values become:

R = 192 = 11000000b

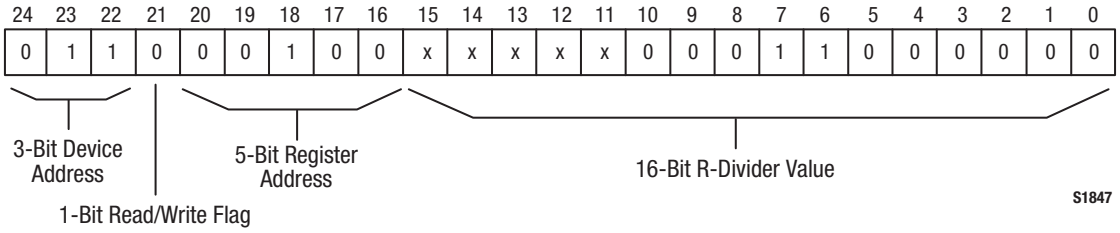
N = 20000 = 100111000100000b

These values would be programmed through the SPI interface.

Figure 5 represents the bits of the R_DIV register with the value of R = 192. Figures 6 and 7 represent the bits of the N_DIV1 and N_DIV2 registers, respectively, with the value of N = 20000.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY73134-11 are provided in Table 3. The recommended operating conditions are specified in Table 4 and electrical specifications are provided in Tables 5 through 7.



Note: Value of bits [15:11] can vary. Refer to *SKY73134-11 Frequency Synthesizer Programming Guide*, document number ***** TBD *****

Figure 5. R_DIV Register Showing an R-Divider Value of 192

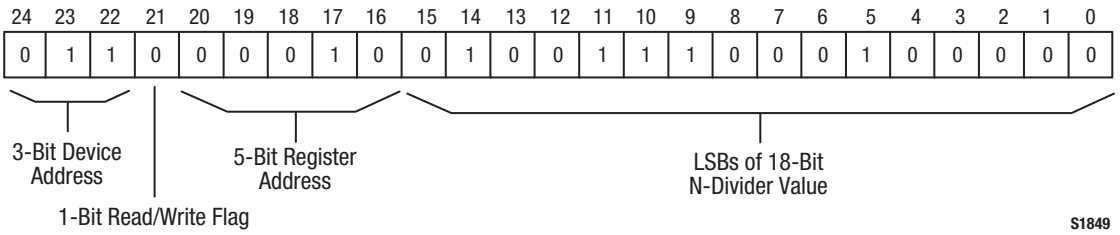
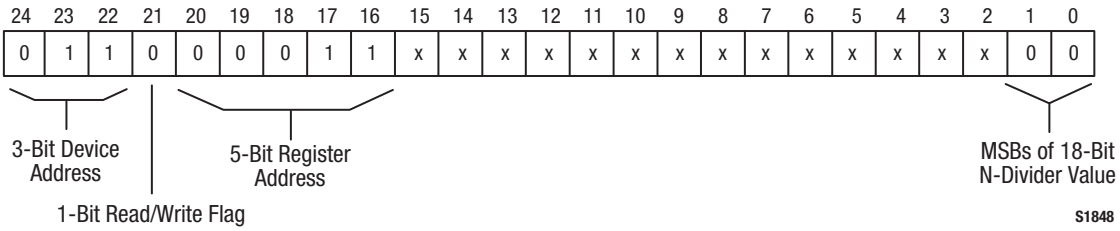


Figure 6. N_DIV1 Register Showing an N-Divider Value of 20000 (LSBs)



Note: Value of bits [15:2] can vary. Refer to *SKY73134-11 Frequency Synthesizer Programming Guide*, document number ***** TBD *****

Figure 7. N_DIV2 Register Showing an N-Divider Value of 20000 (MSBs)

Table 3. SKY73134-11 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage (VCC_VCO, VCC_OBUF, VCC_DIV, VCC_PLL, VCC_CP, VCC_DIG, and VCC_REF pins)	V_{CC}			3.6	V
Supply current	I_{CC}			150	mA
Operating case temperature	T_C	–40		+85	°C
Junction temperature	T_J			+150	°C
Storage case temperature	T_{STG}	–40		+125	°C

Notes: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

CAUTION: *Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 4. SKY73134-11 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage (VCC_VCO, VCC_OBUF, VCC_DIV, VCC_PLL, VCC_CP, VCC_DIG, and VCC_REF pins)	V_{CC}	3.0	3.3	3.6	V
Supply current	I_{CC}		120	130	mA
Operating case temperature	T_C	–40		+85	°C

Table 5. Electrical Specifications: Reference Input and Charge Pump (Note 1)
(T_C = 25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reference input frequency	F_{REF}		10		200	MHz
Reference input sensitivity			200	900		mVp-p
Comparison frequency	F_{COMP}		$F_{RF} \times 10^3 \times D/2^{18}$ (Note 2)		$F_{RF} \times 10^3 \times D/2^{10}$ (Note 2)	kHz
Frequency step	F_{STEP}		$F_{RF} \times 10^3/2^{18}$		$F_{RF} \times 10^3/2^{10}$	kHz
Charge pump current	I_{CP}	Step size = 0.6 mA	0.9	2.7	5.4	mA
Output voltage compliance range			0.4		V_{DD} – 0.4	V
Comparison spurs				–70	–65	dBc
Locking time		20 kHz bandwidth, 1 ppm frequency error			1	ms

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Note 2: D is the VCO divider (1, 2, 3, 4, or 8). F_{RF} is the RF frequency in MHz.

Table 6. SKY73134-11 Electrical Specifications: VCO and RF Output Characteristics (Note 1)
(T_C = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF output frequency	F_{RF}		350		6000	MHz
VCO 1 frequency			2.8		3.4	GHz
VCO 2 frequency			3.3		4.2	GHz
VCO 3 frequency			3.8		4.8	GHz
VCO 4 frequency			4.7		6.0	GHz
VCO sensitivity	K_{VCO}		12	20	38	MHz/V
VCO pushing				5	10	MHz/V
VCO control voltage	V_{CTRL}		0.4		V_{DD} – 0.4	V
RF power			–2	+2	+4	dBm

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Table 7. SKY73134-11 Electrical Specifications: Phase Noise Performance (1 of 2) (Note 1)
(T_C = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
In-Band Phase Noise, Closed Loop						
Normalized in-band phase noise floor with internal VCO		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–211		dBc/Hz
Normalized in-band phase noise floor with external VCO		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–216		dBc/Hz
In-band phase noise floor divide-by-1		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–211 + 20 × logN + 10log(F_{COMP})		dBc/Hz
In-band phase noise floor divide-by-2		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–217 + 20 ×logN + 10log(F_{COMP})		dBc/Hz
In-band phase noise floor divide-by-3		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–220 + 20 ×logN + 10log(F_{COMP})		dBc/Hz
In-band phase noise floor divide-by-4		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–223 + 20 ×logN + 10log(F_{COMP})		dBc/Hz
In-band phase noise floor divide-by-8		I_{CP} = 3.6 mA, PLL bandwidth = 30 kHz		–229 + 20 ×logN + 10log(F_{COMP})		dBc/Hz
PLL Integrated Phase Noise						
Integrated phase noise (1 kHz to 10 MHz)		PLL bandwidth = 30 kHz, RF output = 1 GHz, F_{STEP} = 200 kHz		–43		dBc
VCO 1 Open Loop						
Phase noise: @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz @ 3 MHz @ 10 MHz				 –48 –79 –109 –133 –143 –152		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
VCO 2 Open Loop						
Phase noise: @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz @ 3 MHz @ 10 MHz				 –46 –77 –106 –128 –138 –147		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz
VCO 3 Open Loop						
Phase noise: @ 1 kHz @ 10 kHz @ 100 kHz @ 1 MHz @ 3 MHz @ 10 MHz				 –44 –76 –105 –128 –138 –148		 dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz

Table 7. SKY73134-11 Electrical Specifications: Phase Noise Performance (3 of 3) (Note 1)
(T_C = +25 °C, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
VCO 4 Open Loop						
Phase noise:						
@ 1 kHz				–43		dBc/Hz
@ 10 kHz				–74		dBc/Hz
@ 100 kHz				–104		dBc/Hz
@ 1 MHz				–128		dBc/Hz
@ 3 MHz				–137		dBc/Hz
@ 10 MHz				–148		dBc/Hz
VCO Divided by 2						
Phase noise:						
@ 1 kHz				VCO – 6		dBc/Hz
@ 10 kHz				VCO – 6		dBc/Hz
@ 100 kHz				VCO – 6		dBc/Hz
@ 1 MHz				VCO – 6		dBc/Hz
VCO Divided by 3						
Phase noise:						
@ 1 kHz				VCO – 9.5		dBc/Hz
@ 10 kHz				VCO – 9.5		dBc/Hz
@ 100 kHz				VCO – 9.5		dBc/Hz
@ 1 MHz				VCO – 9.5		dBc/Hz
VCO Divided by 4						
Phase noise:						
@ 1 kHz				VCO – 12		dBc/Hz
@ 10 kHz				VCO – 12		dBc/Hz
@ 100 kHz				VCO – 12		dBc/Hz
@ 1 MHz				VCO – 12		dBc/Hz
VCO Divided by 8						
Phase noise:						
@ 1 kHz				VCO – 18		dBc/Hz
@ 10 kHz				VCO – 18		dBc/Hz
@ 100 kHz				VCO – 18		dBc/Hz

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Evaluation Board Description

The SKY73134-11 Evaluation Board is used to test the performance of the SKY73134-11 frequency synthesizer. An assembly drawing for the Evaluation Board is shown in Figure 8 and the layer detail is provided in Figure 9. A schematic diagram of the SKY73134-11 Evaluation Board is shown in Figure 10.

Circuit Design Configurations

The following design considerations are general in nature and must be followed regardless of final use or configuration:

1. Paths to ground should be made as short as possible.
2. The ground pad of the SKY73134-11 has special electrical and thermal grounding requirements. This pad is the main thermal conduit for heat dissipation. Since the circuit board acts as the heat sink, it must shunt as much heat as possible from the device. Therefore, design the connection to the ground pad to dissipate the maximum wattage produced by the circuit board.
3. Skyworks recommends including external bypass capacitors on the VCC voltage inputs of the device.

***** add'l info TBD *****

Package Dimensions

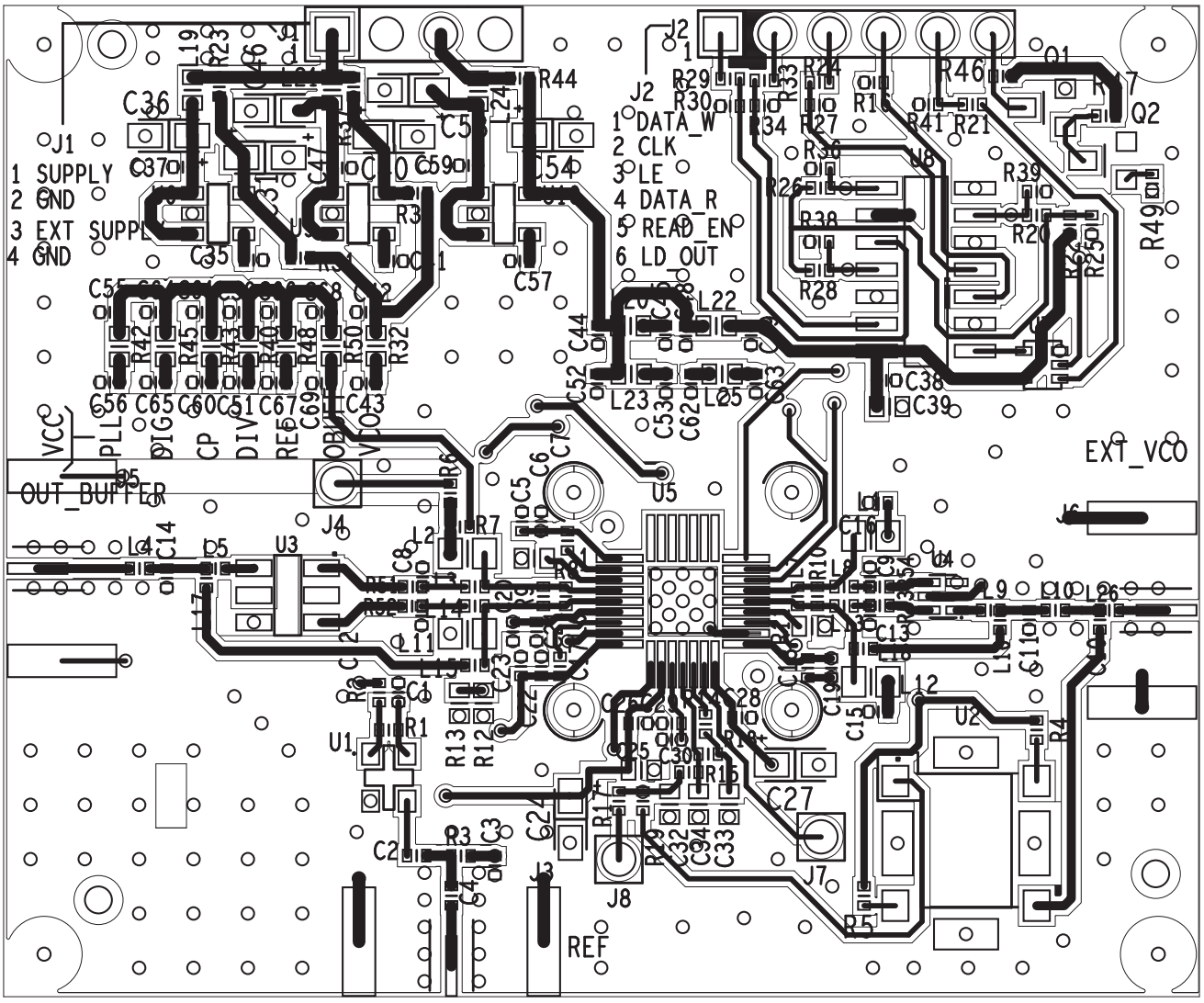
The PCB layout footprint for the SKY73134-11 is provided in Figure 11. Figure 12 shows the package dimensions for the 25-pin LGA and Figure 13 provides the tape and reel dimensions.

Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

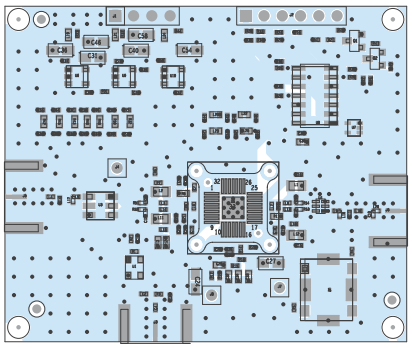
THE SKY73134-11 is rated to Moisture Sensitivity Level 3 (MSL3) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *PCB Design & SMT Assembly/Rework Guidelines for RFLGA Packages*, document number 103147.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

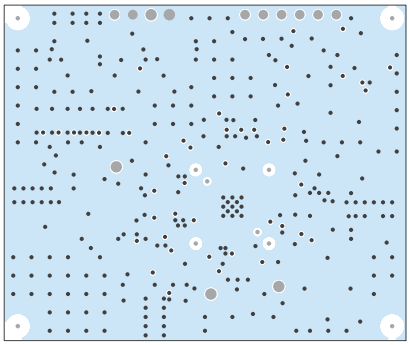


S1851

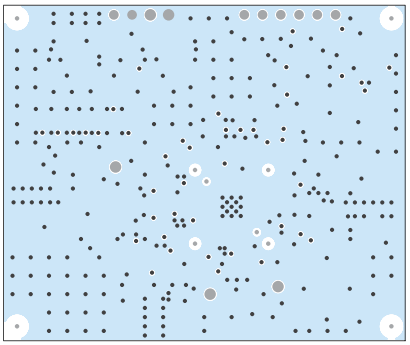
Figure 8. SKY73134-11 Evaluation Board Assembly Diagram



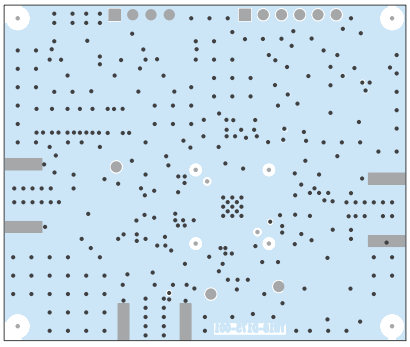
Layer 1: Top – Metal



Layer 2: Ground



Layer 3: Power Plane



Layer 4: Solid Ground Plane

S1852

Figure 9. SKY73134-11 Evaluation Board Layer Detail

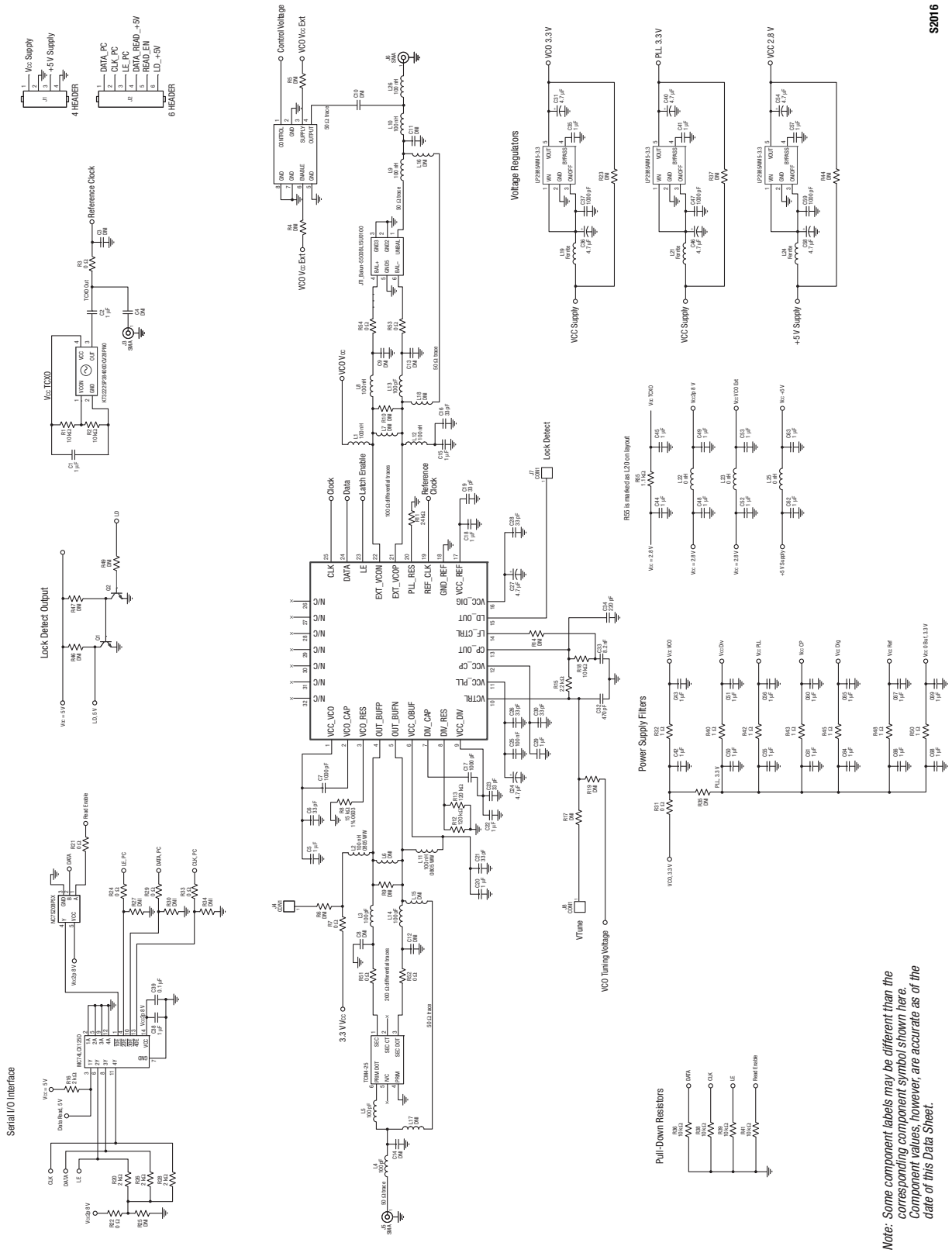


Figure 10. SKY73134-11 Evaluation Board Schematic

*** TBD ***

Figure 11. PCB Layout Footprint for the SKY73134-11 5 x 5 mm RFLGA

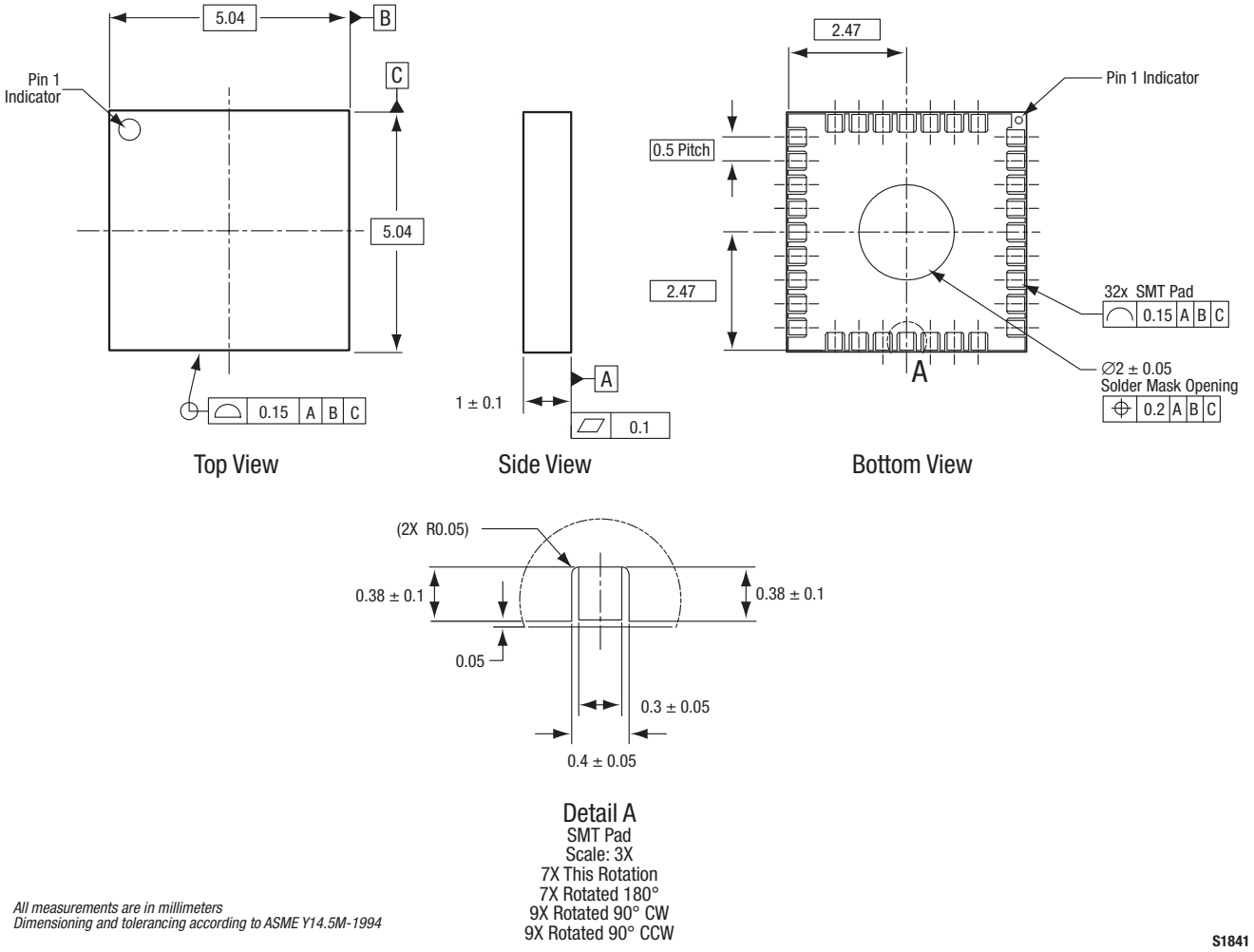


Figure 12. SKY73134-11 32-Pin RFLGA Package Dimensions

*** TBD ***

Figure 13. SKY73134-11 Tape and Reel Dimensions

Ordering Information

Model Name	Manufacturing Part Number	Evaluation Kit Part Number
SKY73134-11 Frequency Synthesizer	SKY73134-11	TW18-D170