

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4752V**

## **LSI**

## **A.C. motor control circuit**

Product specification  
File under Integrated Circuits, IC04

January 1995

# A.C. motor control circuit

# HEF4752V LSI

### DESCRIPTION

The HEF4752V is a circuit for a.c. motor speed control utilizing LOC MOS technology. The circuit synthesizes three 120° out of phase signals, of which the average voltage varies sinusoidally with time in the frequency range 0 to 200 Hz. The method employed is based upon the pulse width modulation principle, in order to achieve a sufficient accuracy of the output voltages over the whole frequency range. A pure digital waveform generation is used.

All outputs are of the push-pull type. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

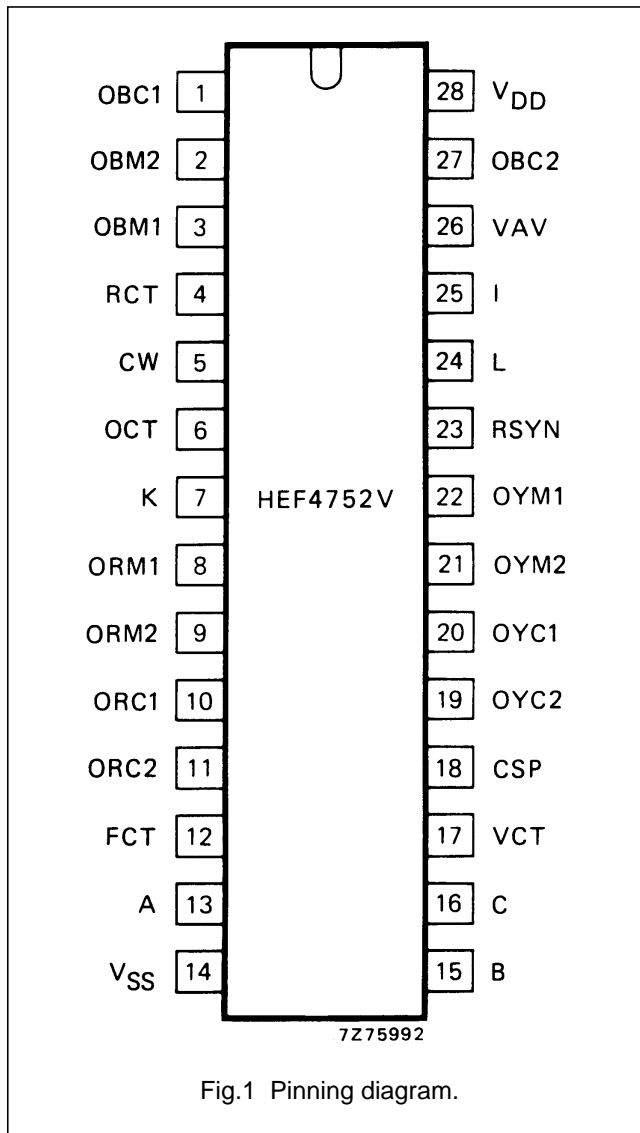


Fig.1 Pinning diagram.

### PINNING

#### Inputs; group I

24 = L	data
25 = I	data
7 = K	data
5 = CW	data
13 = A	data
15 = B	data
16 = C	data

#### Inputs; group II

12 = FCT	frequency clock
17 = VCT	voltage clock
4 = RCT	reference clock
6 = OCT	output delay clock

#### Outputs; group I

23 = RSYN	R-phase synchronization
26 = VAV	average voltage
18 = CSP	current sampling pulses

#### Outputs; group II

8 = ORM1	R-phase main
9 = ORM2	R-phase main
10 = ORC1	R-phase commutation
11 = ORC2	R-phase commutation
22 = OYM1	Y-phase main
21 = OYM2	Y-phase main
20 = OYC1	Y-phase commutation
19 = OYC2	Y-phase commutation
3 = OBM1	B-phase main
2 = OBM2	B-phase main
1 = OBC1	B-phase commutation
27 = OBC2	B-phase commutation

### SUPPLY VOLTAGE

	RATING	RECOMMENDED OPERATING
HEF4752V	-0,5 to 18	4,5 to 12,5 V

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HEF4752VP(N): 28-lead DIL; plastic (SOT117-2)

HEF4752VD(F): 28-lead DIL; ceramic (cerdip) (SOT135)

( ): Package Designator North America

**FAMILY DATA**

See Family Specifications

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## DC CHARACTERISTICS

 $V_{SS} = 0\text{ V}$ 

PARAMETER	$V_{DD}$ V	SYMBOL	$T_{amb}$ (°C)						UNIT	CONDITIONS	
			-40		+ 25		+ 85				
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Quiescent device current	5	$I_{DD}$	-	50	-	50	-	375	$\mu\text{A}$	all valid input combinations; $V_I = V_{SS}$ or $V_{DD}$	
	10		-	100	-	100	-	750	$\mu\text{A}$		
Input leakage current	10	$\pm I_{IN}$	-	-	-	0,3	-	1	$\mu\text{A}$	$V_I = 0$ or $10\text{ V}$	
Input voltage HIGH	5	$V_{IH}$	3,5	-	3,5	-	3,5	-	V	inputs: group I	
	10		7,0	-	7,0	-	7,0	-	V		
Input voltage LOW	5	$V_{IL}$	-	1,5	-	1,5	-	1,5	V	inputs: group I	
	10		-	3,0	-	3,0	-	3,0	V		
Output voltage HIGH	5	$V_{OH}$	4,95	-	4,95	-	4,95	-	V	$V_I = V_{SS}$ or $V_{DD}$ ; $ I_O  < 1\ \mu\text{A}$	
	10		9,95	-	9,95	-	9,95	-	V		
Output voltage LOW	5	$V_{OL}$	-	0,05	-	0,05	-	0,05	V	$V_I = V_{SS}$ or $V_{DD}$ ; $ I_O  < 1\ \mu\text{A}$	
	10		-	0,05	-	0,05	-	0,05	V		
Input tripping level; input voltage increasing	5	$V_{ti}$	1,5	4,0	1,5	4,0	1,5	4,0	V	inputs: group II	
	10		3,0	8,0	3,0	8,0	3,0	8,0	V		
Input tripping level; input voltage decreasing	5	$V_{td}$	1,0	3,5	1,0	3,5	1,0	3,5	V	inputs: group II	
	10		2,0	7,0	2,0	7,0	2,0	7,0	V		
Output current LOW	5	$I_{OL}$	0,45	-	0,38	-	0,3	-	mA	$V_{OL} = 0,4\text{ V}$	outputs: groups I and II
	10		1,4	-	1,17	-	0,9	-	mA	$V_{OL} = 0,5\text{ V}$	
Output current HIGH	5	$-I_{OH}$	0,3	-	0,25	-	0,2	-	mA	$V_{OH} = 4,6\text{ V}$	outputs: group I
	10		0,9	-	0,75	-	0,6	-	mA	$V_{OH} = 9,5\text{ V}$	
Output current HIGH	5	$-I_{OH}$	0,9	-	0,75	-	0,6	-	mA	$V_{OH} = 2,5\text{ V}$	outputs: group I
Output current HIGH	5	$-I_{OH}$	0,6	-	0,5	-	0,4	-	mA	$V_{OH} = 4,6\text{ V}$	outputs: groups II
	10		1,8	-	1,5	-	1,2	-	mA	$V_{OH} = 9,5\text{ V}$	
Output current HIGH	5	$-I_{OH}$	1,8	-	1,5	-	1,2	-	mA	$V_{OH} = 2,5\text{ V}$	outputs: group II
Total supply current	10	$I_{tot}$	-	-	typ. 2	-	-	-	mA	$I_{OL} = I_{OH} = 0$ ; frequency applied to inputs; FCT = 700 kHz; VCT = 400 kHz; RCT = 400 kHz	

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### APPLICATION INFORMATION

Figure 2 shows the functional block diagram of a 3-phase a.c. motor speed control system using a thyristorized inverter with variable frequency output. The inverter control signals are generated by the HEF4752V (PWM-IC). A special feature of the PWM (Pulse-Width Modulation) - IC is here, that the motor is supplied by sinusoidally modulated pulses, hence the resulting motor current will approach a sine-wave with a minimum on higher harmonics. In this way, an optimum speed drive with high performance is obtained.

Furthermore, the HEF4752V contains all logic circuitry required for this special waveform generation, so that the amount of control circuit components is reduced considerable. The speed drive system in Fig.2 is controlled by the analogue control section.

The FCT and VCT clock pulse oscillators are driven in such a way, that a fast response speed control of the a.c. motor is obtained, depending on: the reference values for speed; motor voltage; motor current (Limited by the measured motor current via DCCT - d.c. current transformer -); the increasing value of  $V_{Cb}$  during braking action.

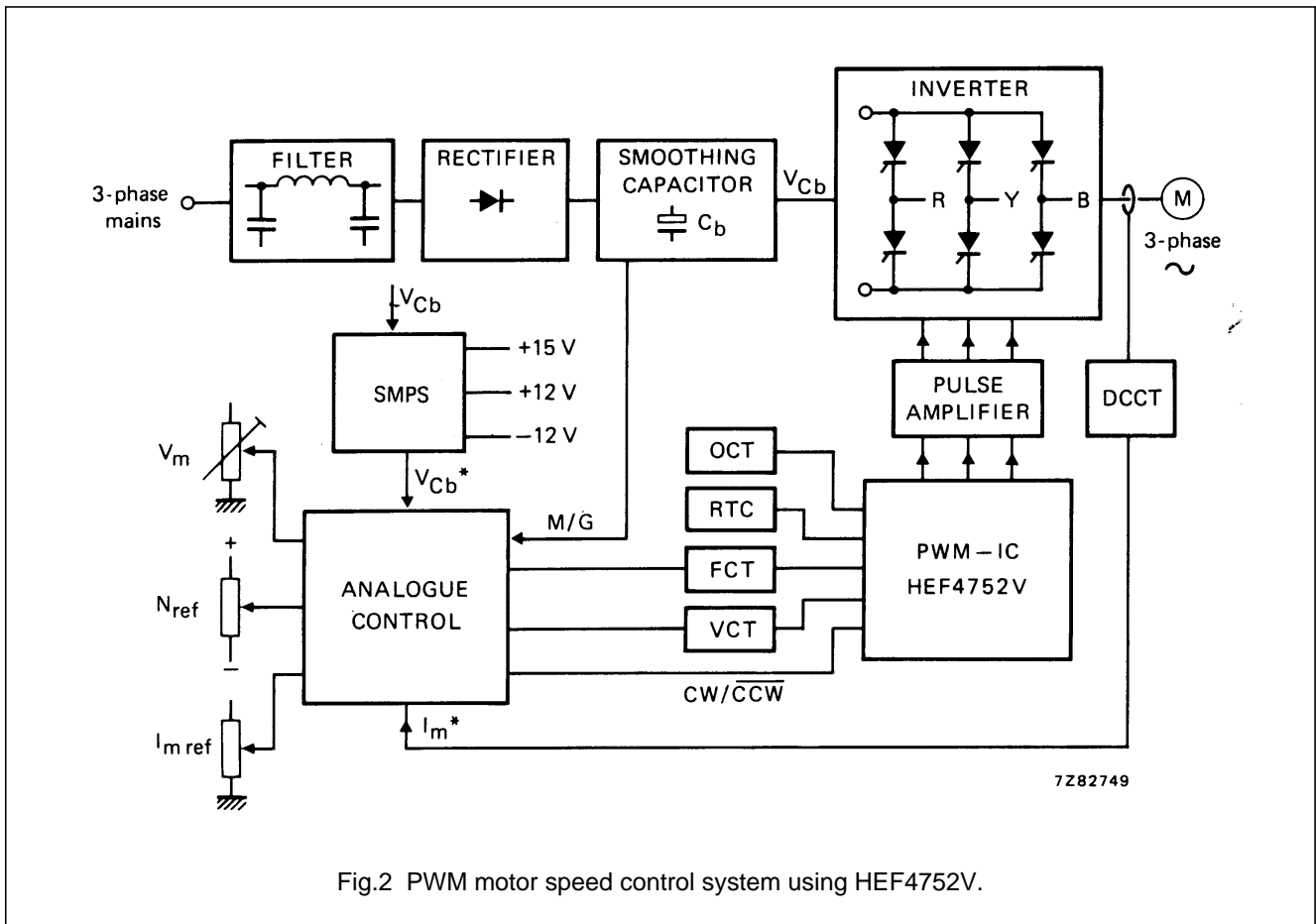


Fig.2 PWM motor speed control system using HEF4752V.

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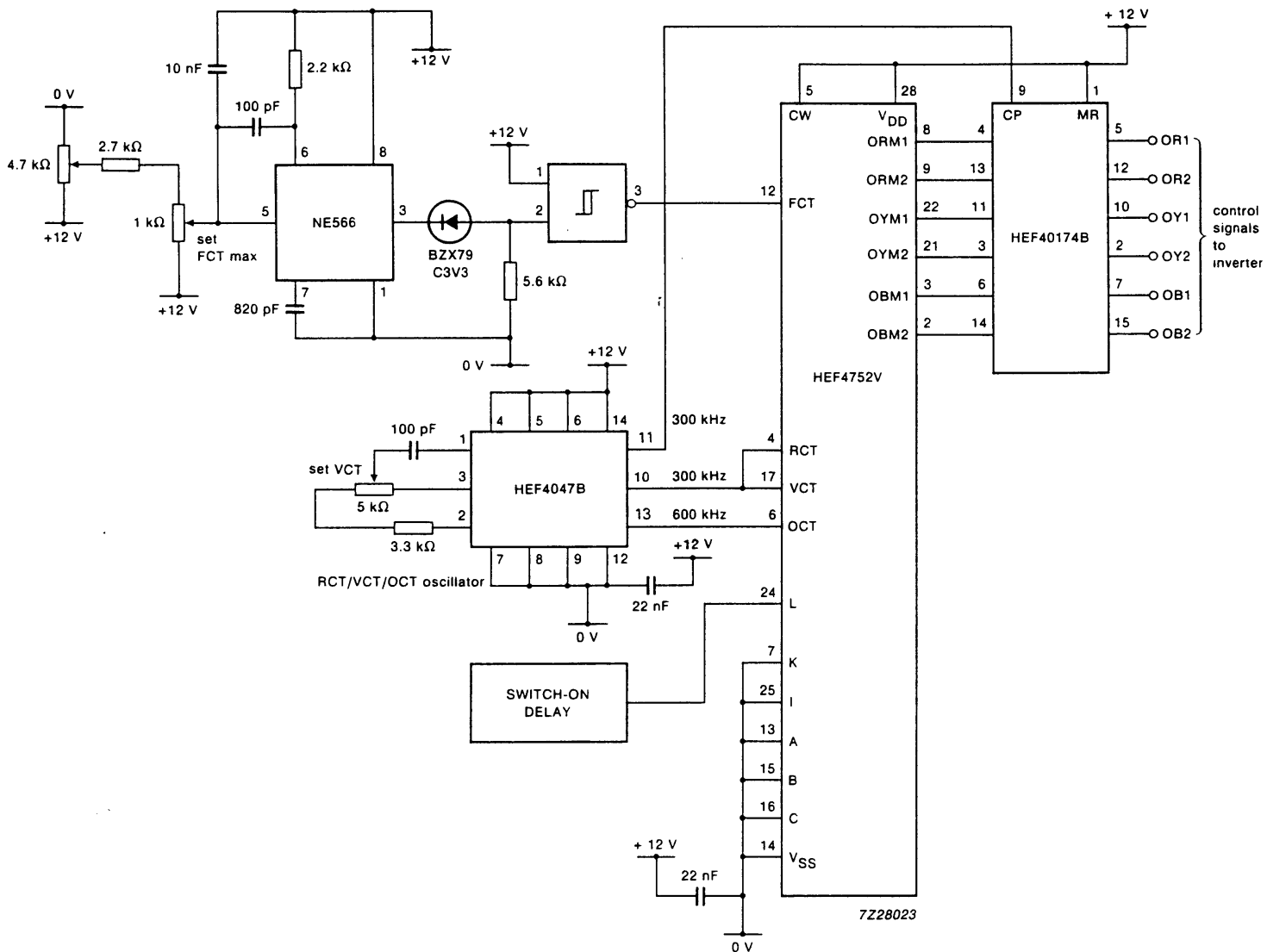


Fig.3 Application of HEF4752V in a basic circuit configuration for AC motor control.