

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4557B**

### **LSI**

**1-to-64 bit variable length shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

# 1-to-64 bit variable length shift register

## HEF4557B LSI

### DESCRIPTION

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs ( $L_1, L_2, L_4, L_8, L_{16}$  and  $L_{32}$ ) plus one. Serial data may be selected from the  $D_A$  or  $D_B$  data inputs with the  $A/\bar{B}$  select input. This feature is useful for recirculation

purposes. Information on  $D_A$  or  $D_B$  is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of  $CP_0$  while  $\overline{CP_1}$  is LOW or on the HIGH to LOW transition of  $\overline{CP_1}$  while  $CP_0$  is HIGH. A HIGH on master reset ( $MR$ ) resets the register and forces  $O$  to LOW and  $\bar{O}$  to HIGH, independent of the other inputs.

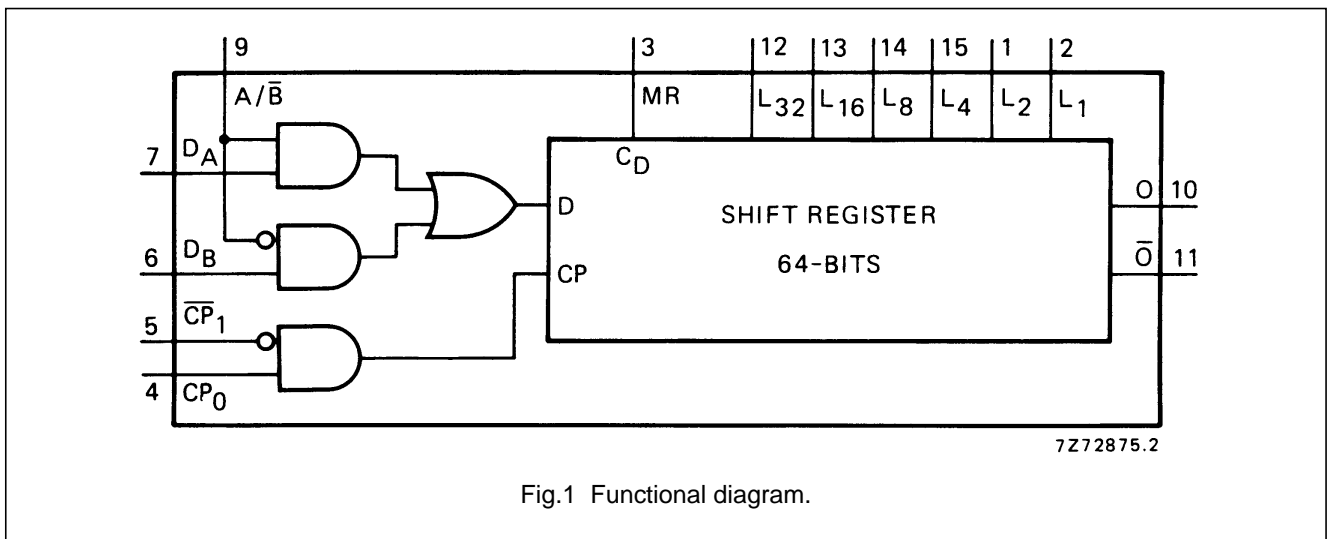


Fig.1 Functional diagram.

### PINNING

- $D_A, D_B$  data inputs
- $A/\bar{B}$  select data input
- $CP_0$  clock input
- $\overline{CP_1}$  clock enable input
- $MR$  asynchronous master reset
- $L_1$  to  $L_{32}$  bit-length control inputs
- $O, \bar{O}$  buffered outputs

- HEF4557BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4557BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4557BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

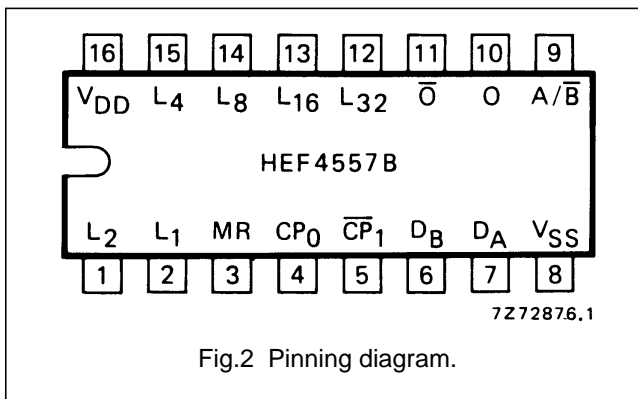


Fig.2 Pinning diagram.

### FAMILY DATA, $I_{DD}$ LIMITS category LSI

See Family Specifications

# 1-to-64 bit variable length shift register

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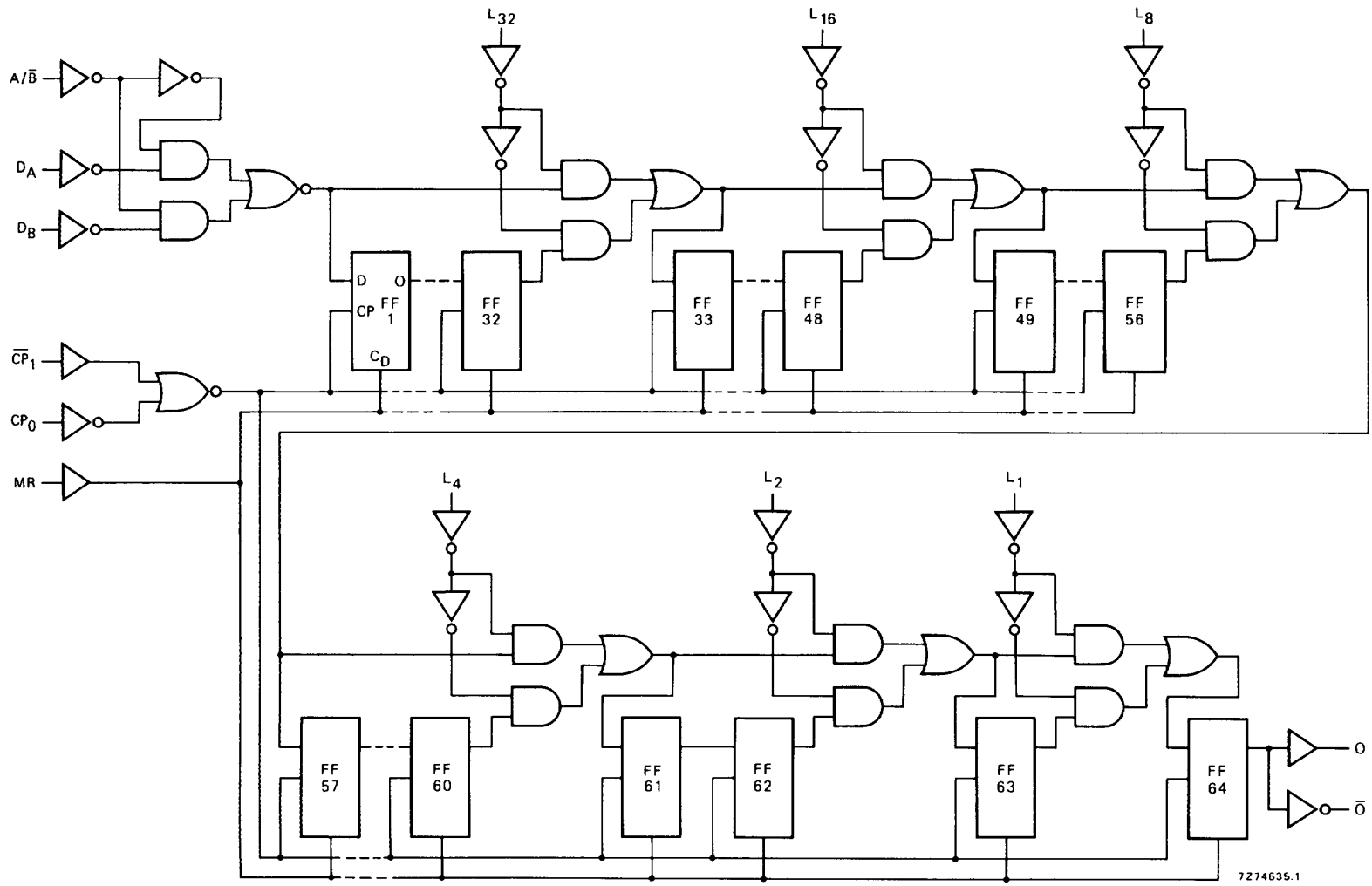


Fig.3 Logic diagram.

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### FUNCTION TABLE

INPUTS						OUTPUT
MR	A/B	D <sub>A</sub>	D <sub>B</sub>	CP <sub>O</sub>	CP <sub>1</sub>	O <sup>(1)</sup>
L	L	D <sub>1</sub>	D <sub>2</sub>	↗	L	D <sub>2</sub>
L	H	D <sub>1</sub>	D <sub>2</sub>	↗	L	D <sub>1</sub>
L	L	D <sub>1</sub>	D <sub>2</sub>	H	↘	D <sub>2</sub>
L	H	D <sub>1</sub>	D <sub>2</sub>	H	↘	D <sub>1</sub>
H	X	X	X	X	X	L

### Notes

1. The moment D<sub>n</sub> appears at O depends on the bit-length shown in the table below.
2. H = HIGH state (the more positive voltage)
3. L = LOW state (the less positive voltage)
4. X = state is immaterial
5. ↗ = positive-going transition
6. ↘ = negative-going transition
7. D<sub>n</sub> = either HIGH or LOW

### BIT-LENGTH SELECT FUNCTION TABLE

L <sub>32</sub>	L <sub>16</sub>	L <sub>8</sub>	L <sub>4</sub>	L <sub>2</sub>	L <sub>1</sub>	REGISTER LENGTH
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

### AC CHARACTERISTICS

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; input transition times ≤ 20 ns

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	3 500 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 15 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 37 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)

## 1-to-64 bit variable length shift register

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LSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP_0, \overline{CP}_1 \rightarrow O, \overline{O}$ HIGH to LOW	5	$t_{PHL}$	240	480	ns	$213\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	240	480	ns	$213\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		90	180	ns	$79\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		65	130	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$
	$MR \rightarrow O$ HIGH to LOW	5	$t_{PHL}$	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$
	$MR \rightarrow \overline{O}$ LOW to HIGH	5	$t_{PLH}$	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	$t_{THL}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$	
	15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{TLH}$	60	120	ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$
		10		30	60	ns	$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
		15		20	40	ns	$6\text{ ns} + (0,28\text{ ns/pF}) C_L$

Interpolation table (see note next page)

LENGTH CONTROL INPUTS						MINIMUM NUMBER OF BITS SELECTED	SET-UP, HOLD, RECOVERY TIMES
$L_1$	$L_2$	$L_4$	$L_8$	$L_{16}$	$L_{32}$		
L	L	L	L	L	L	1	specified
H	L	L	L	L	L	2	
X	H	L	L	L	L	3	
X	X	H	L	L	L	5	six equal steps
X	X	X	H	L	L	9	
X	X	X	X	H	L	17	
X	X	X	X	X	H	33	specified

**Notes**

- H = HIGH state (the more positive voltage)
- L = LOW state (the less positive voltage)
- X = state is immaterial

## 1-to-64 bit variable length shift register

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LSI**AC CHARACTERISTICS** $V_{SS} = 0$  V;  $T_{amb} = 25$  °C;  $C_L = 50$  pF; input transition times  $\leq 20$  ns; see also waveforms Fig.4

	$V_{DD}$ V	SYMBOL	MIN.	TYP.		
Minimum clock pulse width; LOW for $CP_0$ or HIGH for $\overline{CP}_1$	5	$t_{WCPL}$	180	90 ns	see note	
	10	or	60	30 ns		
	15	$t_{WCPH}$	40	20 ns		
Minimum reset pulse width; HIGH	5	$t_{WMRH}$	150	75 ns		
	10		70	35 ns		
	15		50	25 ns		
Set-up times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ $\overline{CP}_1$ $L_1$ to $L_{32} = \text{LOW}$	5	$t_{su}$	360	180 ns		
	10		140	70 ns		
	15		90	45 ns		
	$L_{32} = \text{HIGH}$	5	$t_{su}$	40		-20 ns
		10		35		-10 ns
		15		30		-5 ns
Hold times $D_A, D_B, A/\overline{B} \rightarrow CP_0,$ $\overline{CP}_1$ $L_1$ to $L_{32} = \text{LOW}$	5	$t_{hold}$	-40	-110 ns		
	10		-10	-45 ns		
	15		0	-30 ns		
	$L_{32} = \text{HIGH}$	5	$t_{hold}$	90	30 ns	
		10		60	20 ns	
		15		50	15 ns	
Recovery times for MR $L_1$ to $L_{32} = \text{LOW}$	5	$t_{RMR}$	500	250 ns		
	10		250	125 ns		
	15		150	75 ns		
	$L_{32} = \text{HIGH}$	5	$t_{RMR}$	110	50 ns	
		10		70	30 ns	
		15		60	25 ns	
Minimum clock pulse frequency	5	$f_{max}$	2,5	5 MHz		
	10		7	14 MHz		
	15		10	20 MHz		

**Note**

1. The set-up, hold and recovery times vary with the minimum number of bits selected. For other values as specified one may interpolate as shown in the table (see previous page).

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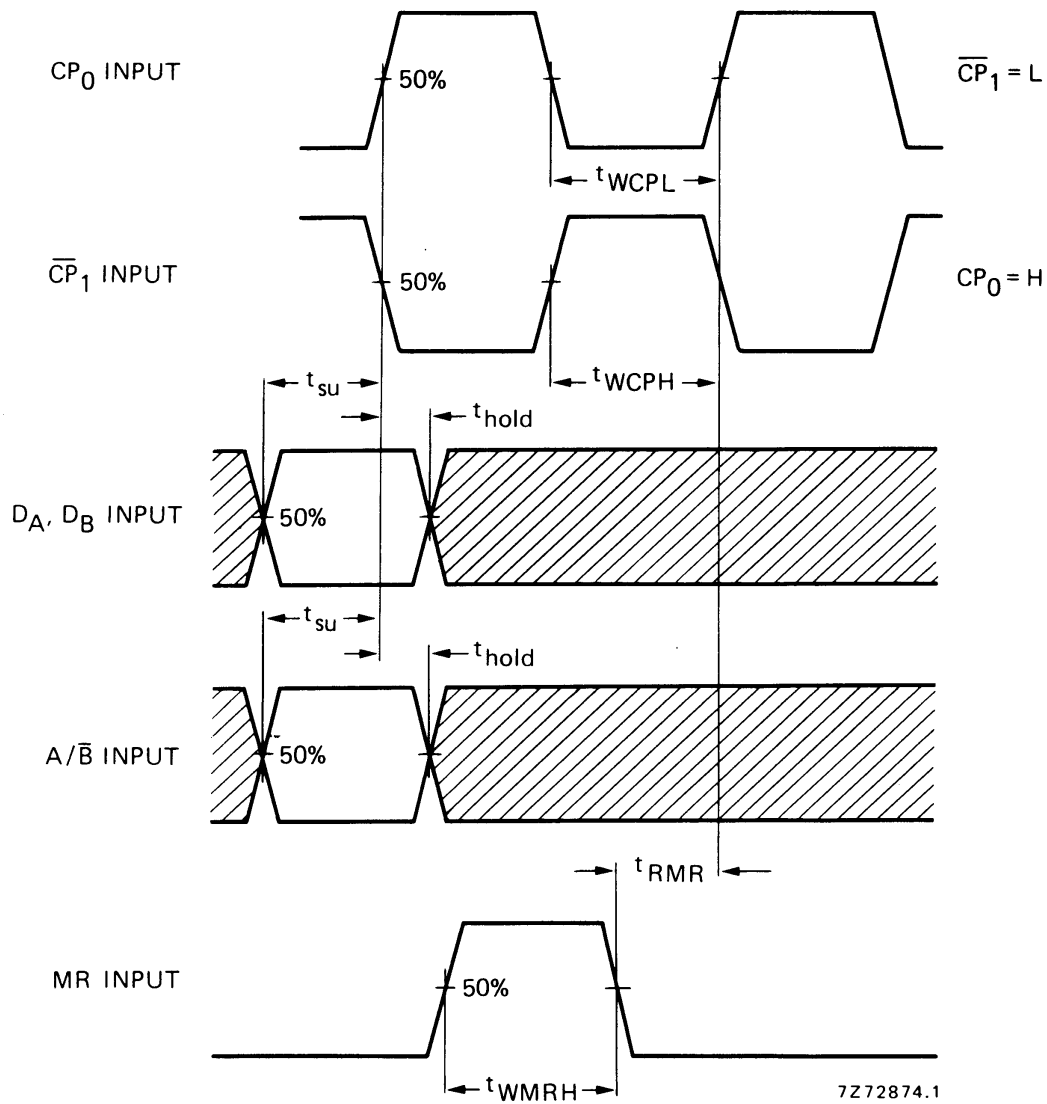


Fig.4 Waveforms showing recovery time for MR and minimum CP<sub>0</sub>,  $\overline{CP}_1$  and MR pulse widths, set-up and hold times for D<sub>A</sub>, D<sub>B</sub> and A/ $\overline{B}$  to CP<sub>0</sub> and  $\overline{CP}_1$ . Set-up and hold times are shown as positive values but may be specified as negative values.