

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4035B**

## **MSI**

## **4-bit universal shift register**

Product specification  
File under Integrated Circuits, IC04

January 1995

4-bit universal shift register

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DESCRIPTION

The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P<sub>0</sub> to P<sub>3</sub>), two synchronous serial data inputs (J,  $\bar{K}$ ), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O<sub>0</sub> to O<sub>3</sub>), a true/complement input (T/ $\bar{C}$ ) and an overriding asynchronous master reset input (MR). Each register is of a D-type master-slave flip-flop.

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P<sub>0</sub> to P<sub>3</sub> on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and  $\bar{K}$  and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and  $\bar{K}$ . When J = HIGH and  $\bar{K}$  = LOW the first stage is in the toggle mode. When J = LOW and  $\bar{K}$  = HIGH the first stage is in the hold mode.

The outputs (O<sub>0</sub> to O<sub>3</sub>) are either inverting or non-inverting, depending on T/ $\bar{C}$  state. With T/ $\bar{C}$  HIGH, O<sub>0</sub> to O<sub>3</sub> are non-inverting (active HIGH) and when T/ $\bar{C}$  is LOW, O<sub>0</sub> to O<sub>3</sub> are inverting (active LOW).

A HIGH on MR resets all four bit positions (O<sub>0</sub> to O<sub>3</sub> = LOW if T/ $\bar{C}$  = HIGH, O<sub>0</sub> to O<sub>3</sub> = HIGH if T/ $\bar{C}$  = LOW) independent of all other input conditions.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

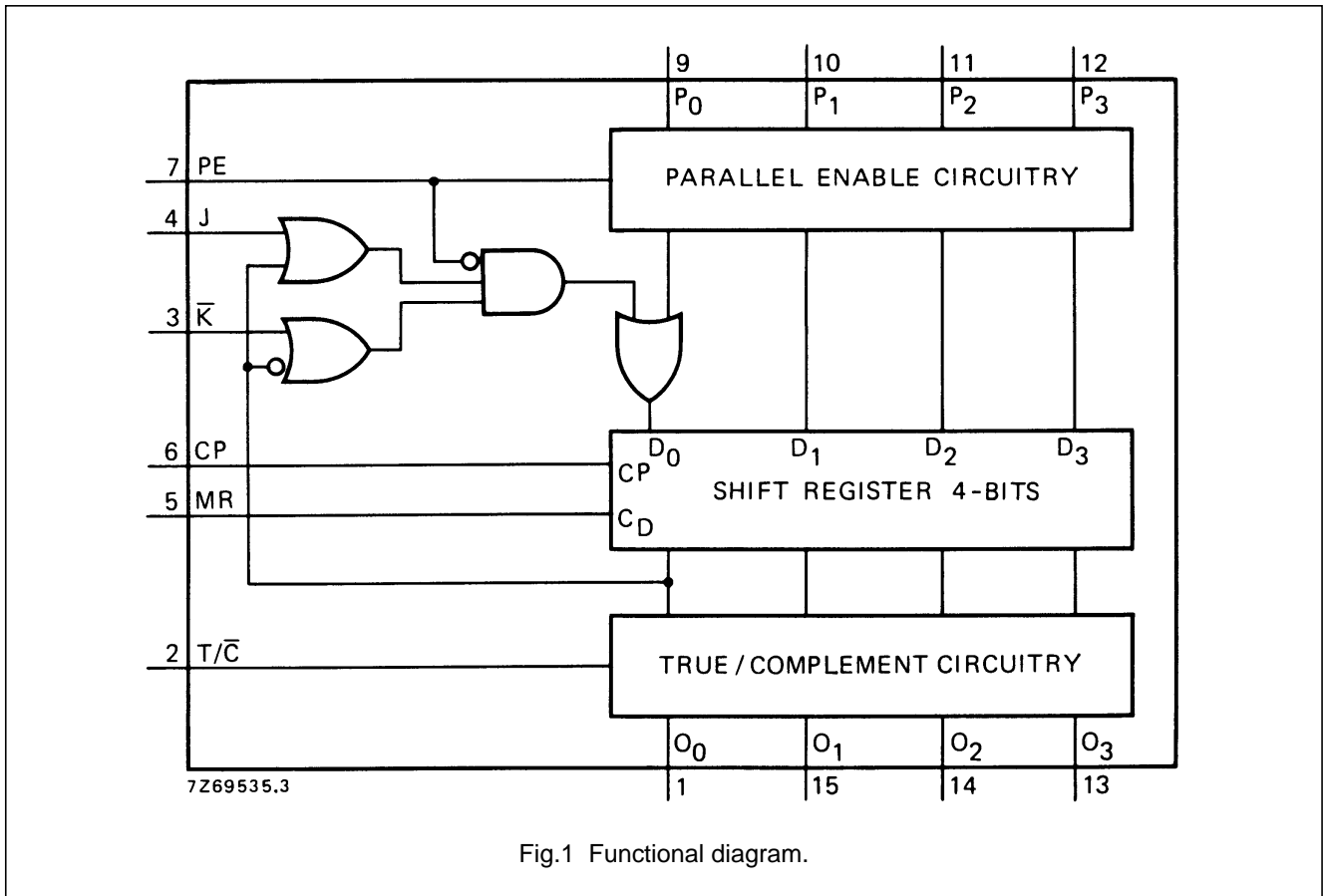


Fig.1 Functional diagram.

FAMILY DATA, I<sub>DD</sub> LIMITS category MSI

See Family Specifications

### 4-bit universal shift register

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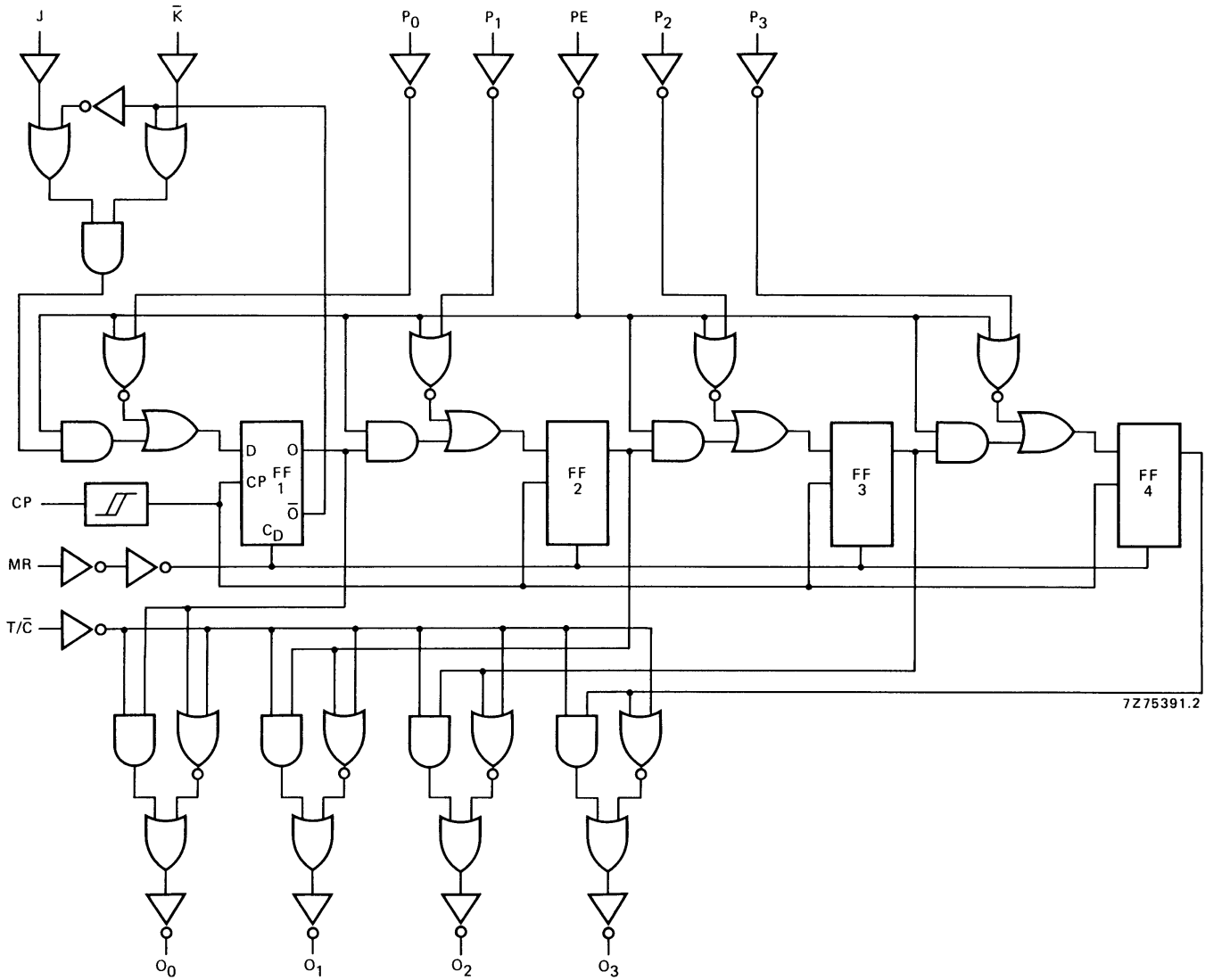


Fig.2 Logic diagram.

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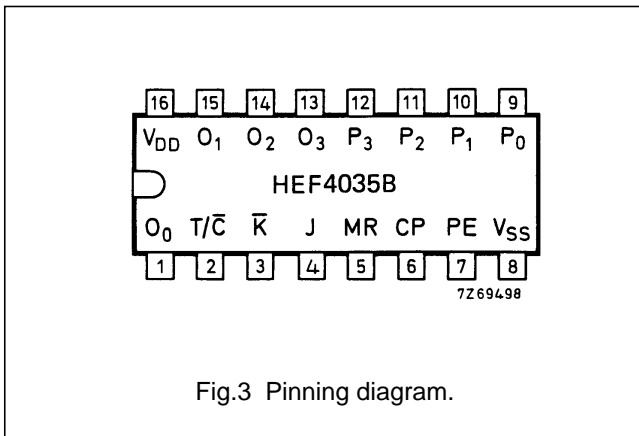


Fig.3 Pinning diagram.

- HEF4035BP(N): 16-lead DIL; plastic (SOT38-1)
  - HEF4035BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
  - HEF4035BT(D): 16-lead SO; plastic (SOT109-1)
- ( ): Package Designator North America

**PINNING**

- PE parallel enable input
- P<sub>0</sub> to P<sub>3</sub> parallel data inputs
- J first stage J-input (active HIGH)
- $\bar{K}$  first stage K-input (active LOW)
- CP clock input (LOW to HIGH edge-triggered)
- $T/\bar{C}$  true/complement input
- MR master reset input
- O<sub>0</sub> to O<sub>3</sub> buffered parallel outputs

**FUNCTION TABLES**

**Serial operation first stage**

INPUTS				OUTPUT	MODE OF OPERATION
CP	J	$\bar{K}$	MR	O <sub>0+1</sub>	
↗	H	H	L	H	D flip-flop
↗	L	L	L	L	D flip-flop
↗	H	L	L	$\bar{O}_0$	toggle
↗	L	H	L	O <sub>0</sub>	no change
X	X	X	H	L	reset

**Note**

1.  $T/\bar{C}$  = HIGH; PE = LOW

**Parallel operation**

CP	INPUTS				OUTPUTS			
	P <sub>0</sub>	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	O <sub>0</sub>	O <sub>1</sub>	O <sub>2</sub>	O <sub>3</sub>
↗	H	H	H	H	H	H	H	H
↗	L	L	L	L	L	L	L	L

**Notes**

1.  $T/\bar{C}$  = HIGH; PE = HIGH; MR = LOW  
 ↗ = positive-going transition  
 H = HIGH state (the more positive voltage)  
 L = LOW state (the less positive voltage)  
 X = state is immaterial

## 4-bit universal shift register

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays CP $\rightarrow$ $O_n$ HIGH to LOW	5		170	340	ns	143 ns + (0,55 ns/pF) $C_L$
	10	$t_{PHL}$	70	140	ns	59 ns + (0,23 ns/pF) $C_L$
	15		50	100	ns	42 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5		150	300	ns	123 ns + (0,55 ns/pF) $C_L$
	10	$t_{PLH}$	65	130	ns	54 ns + (0,23 ns/pF) $C_L$
	15		50	100	ns	42 ns + (0,16 ns/pF) $C_L$
MR $\rightarrow$ $O_n$ HIGH to LOW	5		115	230	ns	88 ns + (0,55 ns/pF) $C_L$
	10	$t_{PHL}$	50	100	ns	39 ns + (0,23 ns/pF) $C_L$
	15		40	80	ns	32 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5		115	230	ns	88 ns + (0,55 ns/pF) $C_L$
	10	$t_{PLH}$	50	100	ns	39 ns + (0,23 ns/pF) $C_L$
	15		40	80	ns	32 ns + (0,16 ns/pF) $C_L$
$T/\bar{C} \rightarrow O_n$ HIGH to LOW	5		105	210	ns	78 ns + (0,55 ns/pF) $C_L$
	10	$t_{PHL}$	50	100	ns	39 ns + (0,23 ns/pF) $C_L$
	15		35	70	ns	27 ns + (0,16 ns/pF) $C_L$
LOW to HIGH	5		85	170	ns	58 ns + (0,55 ns/pF) $C_L$
	10	$t_{PLH}$	45	90	ns	34 ns + (0,23 ns/pF) $C_L$
	15		35	70	ns	27 ns + (0,16 ns/pF) $C_L$
Output transition times HIGH to LOW	5		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10	$t_{THL}$	30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$
LOW to HIGH	5		60	120	ns	10 ns + (1,0 ns/pF) $C_L$
	10	$t_{TLH}$	30	60	ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40	ns	6 ns + (0,28 ns/pF) $C_L$

4-bit universal shift register

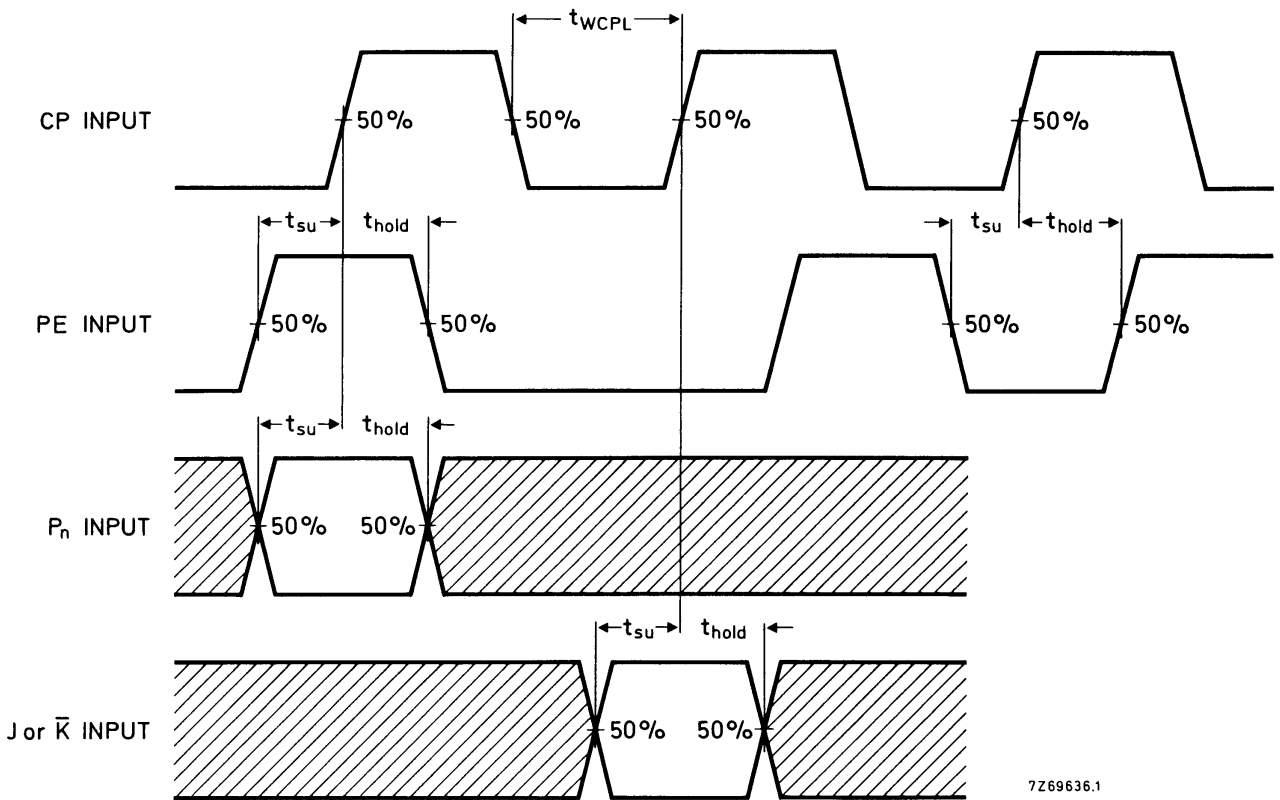
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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum clock pulse width; LOW	5	t <sub>WCPL</sub>	80	40	ns	see also waveforms Figs 4 and 5
	10		40	20	ns	
	15		30	15	ns	
Minimum MR pulse width; HIGH	5	t <sub>WMRH</sub>	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t <sub>RMR</sub>	50	20	ns	
	10		40	15	ns	
	15		25	10	ns	
Set-up times P <sub>n</sub> → CP	5	t <sub>su</sub>	40	5	ns	
	10		25	0	ns	
	15		15	0	ns	
PE → CP	5	t <sub>su</sub>	50	25	ns	
	10		35	15	ns	
	15		30	10	ns	
J, $\bar{K}$ → CP	5	t <sub>su</sub>	55	40	ns	
	10		35	15	ns	
	15		25	10	ns	
Hold times P <sub>n</sub> → CP	5	t <sub>hold</sub>	25	10	ns	
	10		20	10	ns	
	15		20	10	ns	
PE → CP	5	t <sub>hold</sub>	15	-5	ns	
	10		10	-5	ns	
	15		5	-5	ns	
J, $\bar{K}$ → CP	5	t <sub>hold</sub>	10	-5	ns	
	10		10	0	ns	
	15		10	0	ns	
Maximum clock pulse frequency	5	f <sub>max</sub>	5	10	MHz	
	10		12	25	MHz	
	15		15	30	MHz	

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load cap. (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)
	10	6 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	
	15	20 000 f <sub>i</sub> + ∑ (f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	

4-bit universal shift register

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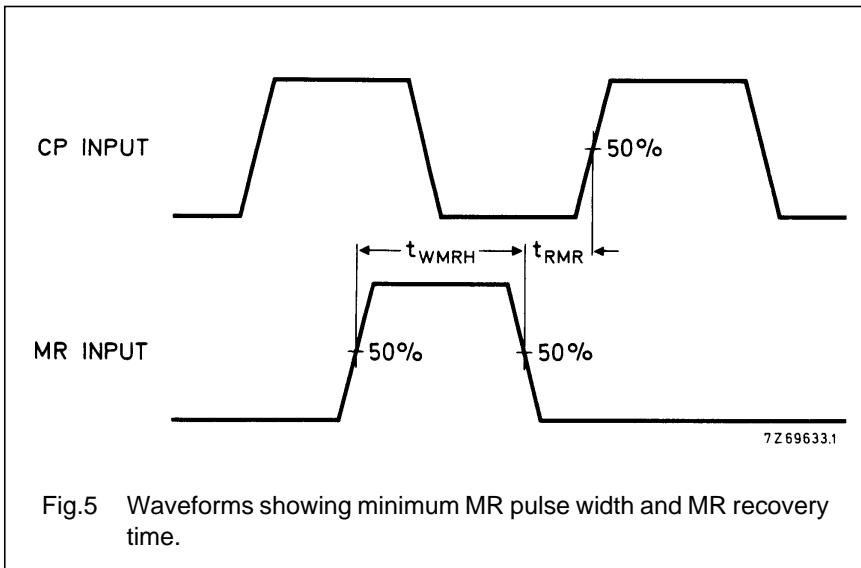


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Fig.4 Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

4-bit universal shift register

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APPLICATION INFORMATION

Some examples of applications for the HEF4035B are:

- Counters, registers, arithmetic-unit registers, shift-left/shift-right registers.
- Serial-to-parallel/parallel-to-serial conversions.
- Sequence generation.
- Control circuits.
- Code conversion.

