

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4071B

gates

Quadruple 2-input OR gate

Product specification
File under Integrated Circuits, IC04

January 1995

Quadruple 2-input OR gate

HEF4071B
gates

DESCRIPTION

The HEF4071B is a positive logic quadruple 2-input OR gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

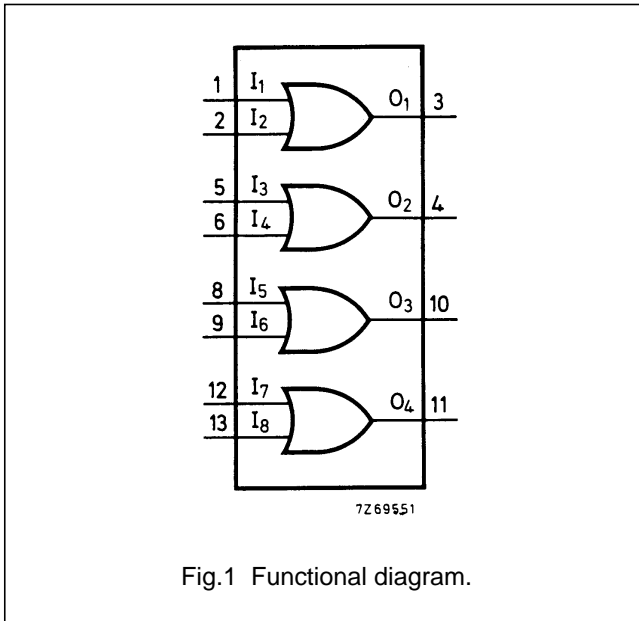


Fig.1 Functional diagram.

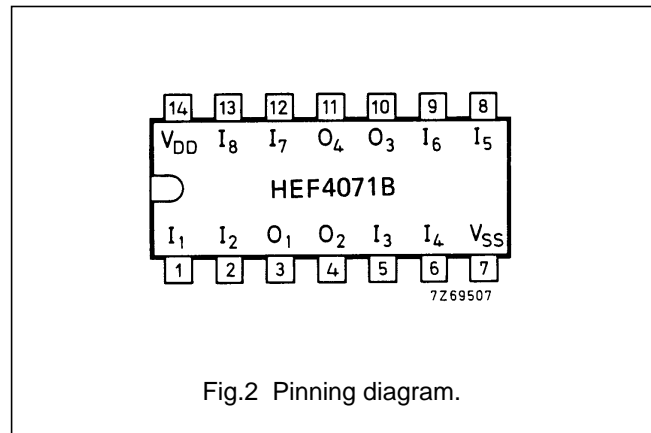


Fig.2 Pinning diagram.

- HEF4071BP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4071BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4071BT(D): 14-lead SO; plastic (SOT108-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category GATES

See Family Specifications

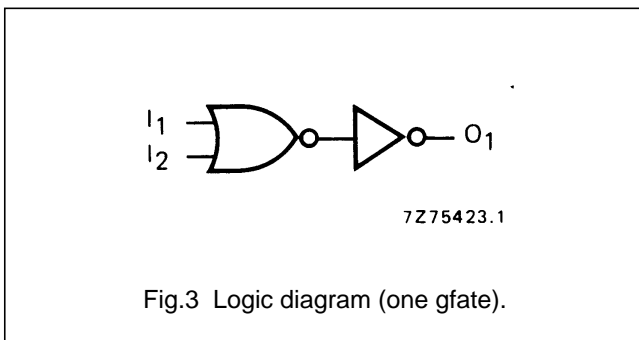


Fig.3 Logic diagram (one gate).

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AC CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$	5	t_{PHL}	55	115	ns	28 ns + (0,55 ns/pF) C_L
			25	50	ns	15 ns + (0,23 ns/pF) C_L
			20	35	ns	12 ns + (0,16 ns/pF) C_L
	10	t_{PLH}	45	90	ns	18 ns + (0,55 ns/pF) C_L
			20	45	ns	9 ns + (0,23 ns/pF) C_L
			15	30	ns	7 ns + (0,16 ns/pF) C_L
Output transition times	5	t_{THL}	60	120	ns	10 ns + (1,0 ns/pF) C_L
			30	60	ns	9 ns + (0,42 ns/pF) C_L
			20	40	ns	6 ns + (0,28 ns/pF) C_L
	10	t_{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C_L
			30	60	ns	9 ns + (0,42 ns/pF) C_L
			20	40	ns	6 ns + (0,28 ns/pF) C_L

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1150 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4800 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$19\,700 f_i + \sum (f_o C_L) \times V_{DD}^2$	