

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF40192B**

### **MSI**

## 4-bit up/down decade counter

Product specification  
File under Integrated Circuits, IC04

January 1995

## 4-bit up/down decade counter

HEF40192B  
MSI

## DESCRIPTION

The HEF40192B is a 4-bit synchronous up/down decade counter. The counter has a count-up clock input ( $CP_U$ ), a count-down clock input ( $CP_D$ ), an asynchronous parallel load input ( $\overline{PL}$ ), four parallel data inputs ( $P_0$  to  $P_3$ ), an asynchronous master reset input ( $MR$ ), four counter outputs ( $O_0$  to  $O_3$ ), an active LOW terminal count-up (carry) output ( $\overline{TC}_U$ ) and an active LOW terminal count-down (borrow) output ( $\overline{TC}_D$ ).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct

counting, both clock inputs cannot be LOW simultaneously. The outputs  $\overline{TC}_U$  and  $\overline{TC}_D$  are normally HIGH. When the circuit has reached the maximum count state of '9', the next HIGH to LOW transition of  $CP_U$  will cause  $\overline{TC}_U$  to go LOW.  $\overline{TC}_U$  will stay LOW until  $CP_U$  goes HIGH again. Likewise, output  $\overline{TC}_D$  will go LOW when the circuit is in the zero state and  $CP_D$  goes LOW. When  $\overline{PL}$  is LOW, the information on  $P_0$  to  $P_3$  is asynchronously loaded into the counter. A HIGH on  $MR$  resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

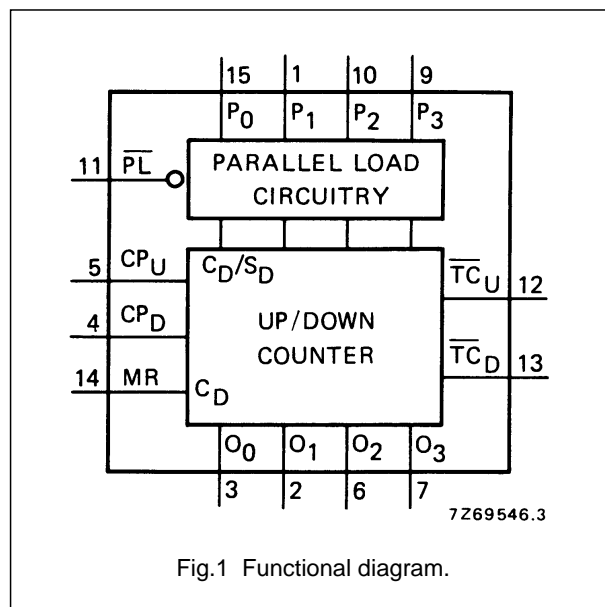


Fig.1 Functional diagram.

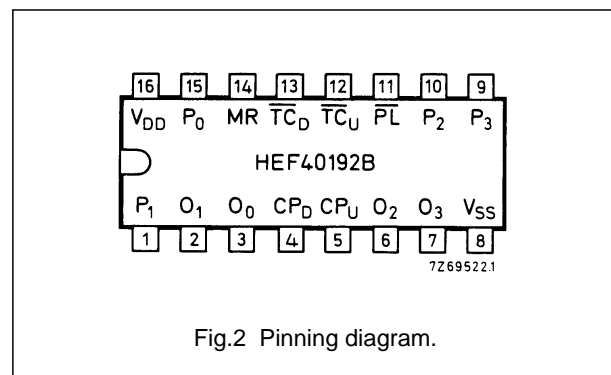


Fig.2 Pinning diagram.

## PINNING

$\overline{PL}$	parallel load input (active LOW)
$P_0$ to $P_3$	parallel data inputs
$CP_U$	count-up clock pulse input (LOW to HIGH, edge-triggered)
$CP_D$	count-down clock pulse input (LOW to HIGH, edge-triggered)
$MR$	master reset input (asynchronous)
$\overline{TC}_U$	buffered terminal count-up (carry) output (active LOW)
$\overline{TC}_D$	buffered terminal count-down (borrow) output (active LOW)
$O_0$ to $O_3$	buffered counter outputs

HEF40192BP(N):	16-lead DIL; plastic (SOT38-1)
HEF40192BD(F):	16-lead DIL; ceramic (cerdip) (SOT74)
HEF40192BT(D):	16-lead SO; plastic (SOT109-1)
( ):	Package Designator North America

FAMILY DATA,  $I_{DD}$  LIMITS category MSI

See Family Specifications

4-bit up/down decade counter

HEF40192B  
MSI

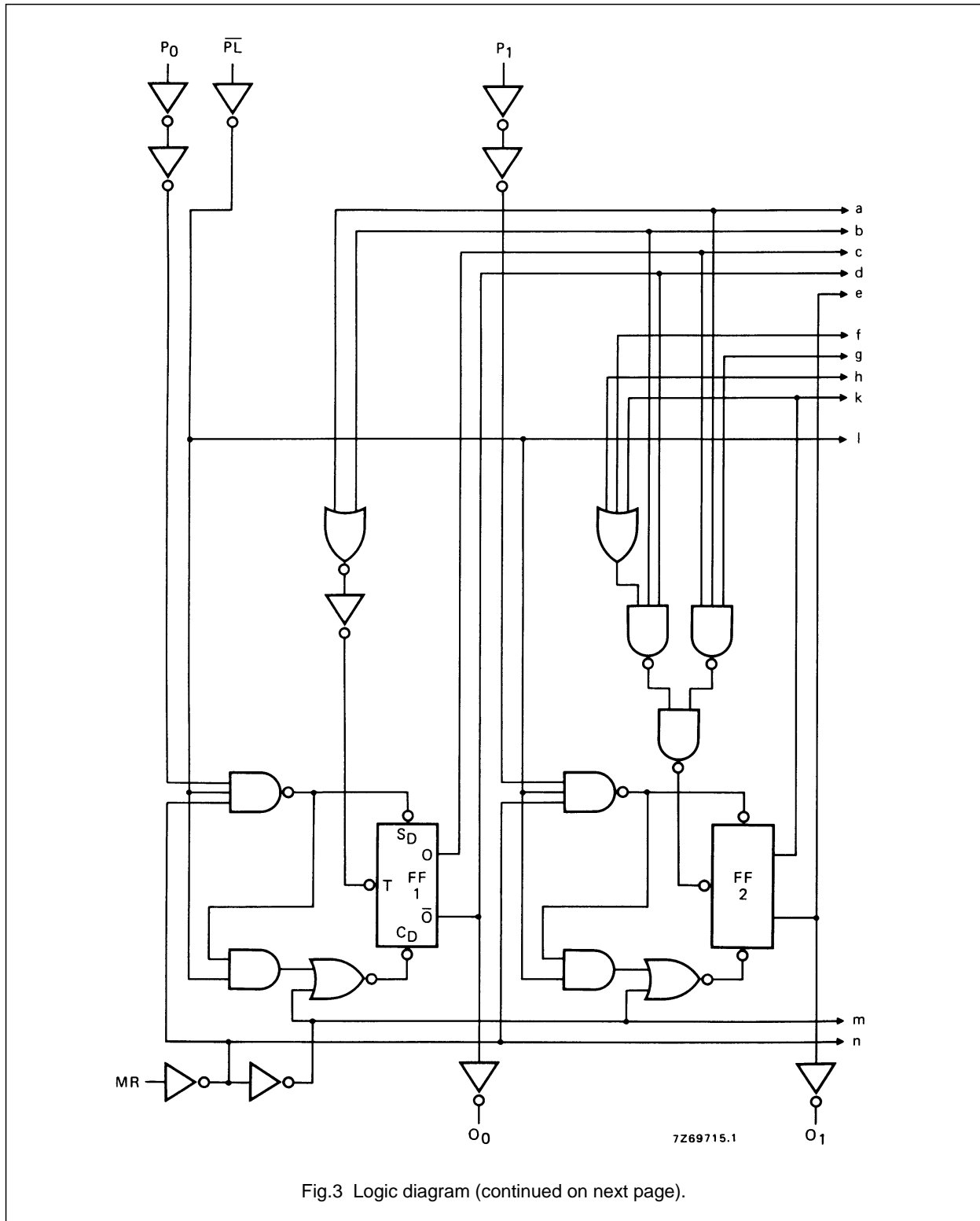


Fig.3 Logic diagram (continued on next page).

4-bit up/down decade counter

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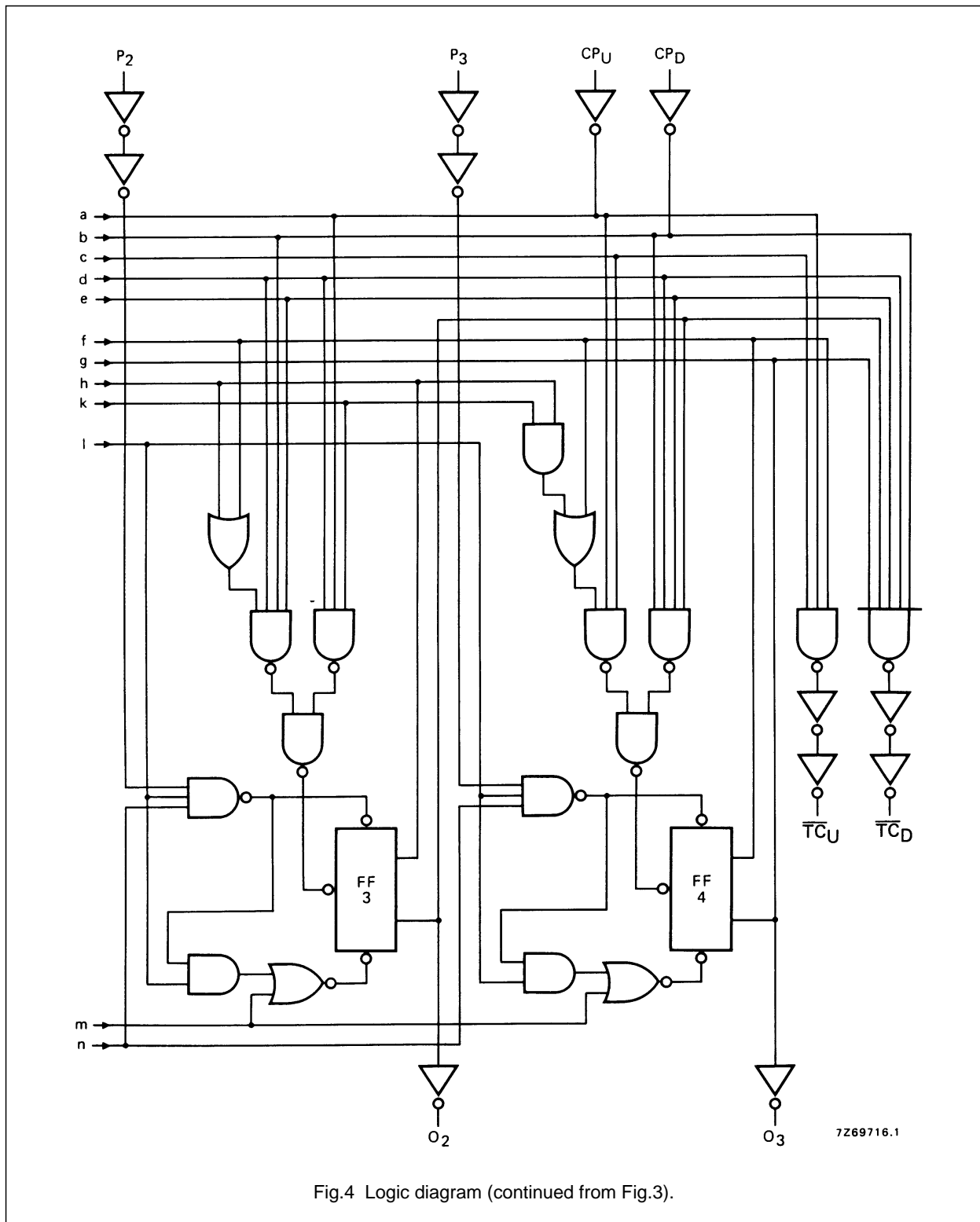




Fig.4 Logic diagram (continued from Fig.3).


# 4-bit up/down decade counter

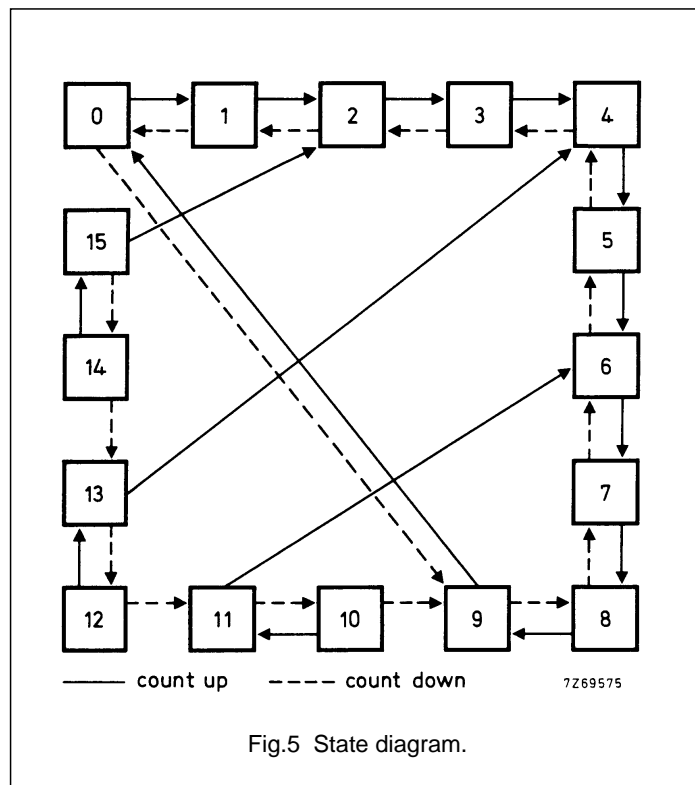
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**FUNCTION TABLE**

MR	$\overline{PL}$	CP <sub>U</sub>	CP <sub>D</sub>	MODE
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H		H	count-up
L	H	H		count-down

**Notes**

- H = HIGH state (the more positive voltage)  
L = LOW state (the less positive voltage)  
X = state is immaterial  
 = positive-going transition



Logic equations for terminal count:

$$\overline{TC}_D = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot CP_D}$$

$$\overline{TC}_U = O_0 \cdot O_3 \cdot \overline{CP_U}$$

**AC CHARACTERISTICS**

V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; input transition times ≤ 20 ns

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	550 f <sub>i</sub> + ∑(f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 2400 f <sub>i</sub> + ∑(f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup> 6500 f <sub>i</sub> + ∑(f <sub>o</sub> C <sub>L</sub> ) × V <sub>DD</sub> <sup>2</sup>	where f <sub>i</sub> = input freq. (MHz) f <sub>o</sub> = output freq. (MHz) C <sub>L</sub> = load capacitance (pF) ∑ (f <sub>o</sub> C <sub>L</sub> ) = sum of outputs V <sub>DD</sub> = supply voltage (V)

## 4-bit up/down decade counter

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$ 

	$V_{DD}$ V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP_U \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	210	415	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		85	165	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	210	420	ns	$183\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		85	170	ns	$74\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		65	125	ns	$57\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	170	340	ns	$143\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		70	140	ns	$59\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		50	100	ns	$42\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_U \rightarrow \overline{TC}_U$ HIGH to LOW	5	$t_{PHL}$	125	250	ns	$98\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		50	100	ns	$39\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		35	70	ns	$27\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	95	185	ns	$68\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	80	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	60	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$CP_D \rightarrow \overline{TC}_D$ HIGH to LOW	5	$t_{PHL}$	140	280	ns	$113\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		55	110	ns	$44\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		40	80	ns	$32\text{ ns} + (0,16\text{ ns/pF}) C_L$	
	LOW to HIGH	5	$t_{PLH}$	100	195	ns	$73\text{ ns} + (0,55\text{ ns/pF}) C_L$
		10		40	85	ns	$29\text{ ns} + (0,23\text{ ns/pF}) C_L$
		15		30	65	ns	$22\text{ ns} + (0,16\text{ ns/pF}) C_L$
$MR \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	195	390	ns	$168\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		80	160	ns	$69\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		60	120	ns	$52\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$MR \rightarrow \overline{TC}_U$ LOW to HIGH	5	$t_{PLH}$	145	285	ns	$118\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		60	115	ns	$49\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		45	90	ns	$37\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$MR \rightarrow \overline{TC}_D$ HIGH to LOW	5	$t_{PHL}$	365	730	ns	$338\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		130	265	ns	$119\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		100	205	ns	$92\text{ ns} + (0,16\text{ ns/pF}) C_L$	
$\overline{PL} \rightarrow O_n$ HIGH to LOW	5	$t_{PHL}$	185	360	ns	$158\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10		75	150	ns	$64\text{ ns} + (0,23\text{ ns/pF}) C_L$	
	15		55	110	ns	$47\text{ ns} + (0,16\text{ ns/pF}) C_L$	

## 4-bit up/down decade counter

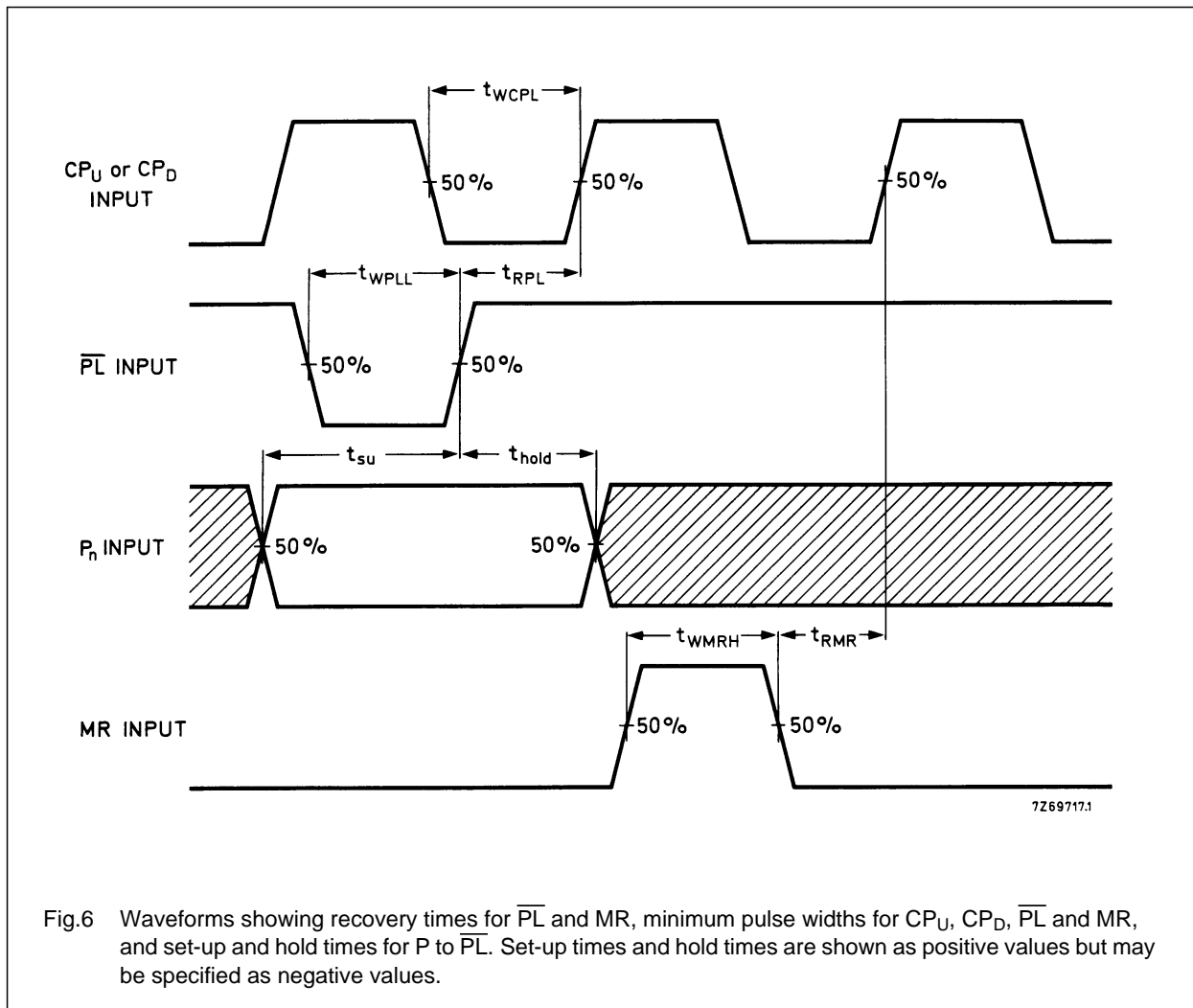
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	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
LOW to HIGH	5	t <sub>PLH</sub>		145	290	ns	118 ns + (0,55 ns/pF) C <sub>L</sub>
	10			60	120	ns	49 ns + (0,23 ns/pF) C <sub>L</sub>
	15			45	90	ns	37 ns + (0,16 ns/pF) C <sub>L</sub>

**AC CHARACTERISTICS**V<sub>SS</sub> = 0 V; T<sub>amb</sub> = 25 °C; C<sub>L</sub> = 50 pF; input transition times ≤ 20 ns

	V <sub>DD</sub> V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Output transition times HIGH to LOW	5	t <sub>THL</sub>		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
	10			30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15			20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
LOW to HIGH	5	t <sub>TLH</sub>		60	120	ns	10 ns + (1,0 ns/pF) C <sub>L</sub>
	10			30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15			20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
Set-up time P <sub>n</sub> → $\overline{PL}$	5	t <sub>su</sub>	160	80		ns	see also waveforms Fig.6
	10		60	30		ns	
	15		50	25		ns	
Hold time P <sub>n</sub> → $\overline{PL}$	5	t <sub>hold</sub>	10	-70		ns	
	10		5	-25		ns	
	15		5	-20		ns	
Minimum CP <sub>U</sub> or CP <sub>D</sub> pulse width; LOW	5	t <sub>WCPL</sub>	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Minimum MR pulse width; HIGH	5	t <sub>WMRH</sub>	180	90		ns	
	10		70	35		ns	
	15		60	30		ns	
Minimum $\overline{PL}$ pulse width; LOW	5	t <sub>WPLL</sub>	120	60		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for MR	5	t <sub>RMR</sub>	125	65		ns	
	10		70	35		ns	
	15		50	25		ns	
Recovery time for $\overline{PL}$	5	t <sub>RPL</sub>	90	45		ns	
	10		35	15		ns	
	15		25	10		ns	
Maximum clock pulse frequency	5	f <sub>max</sub>	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	

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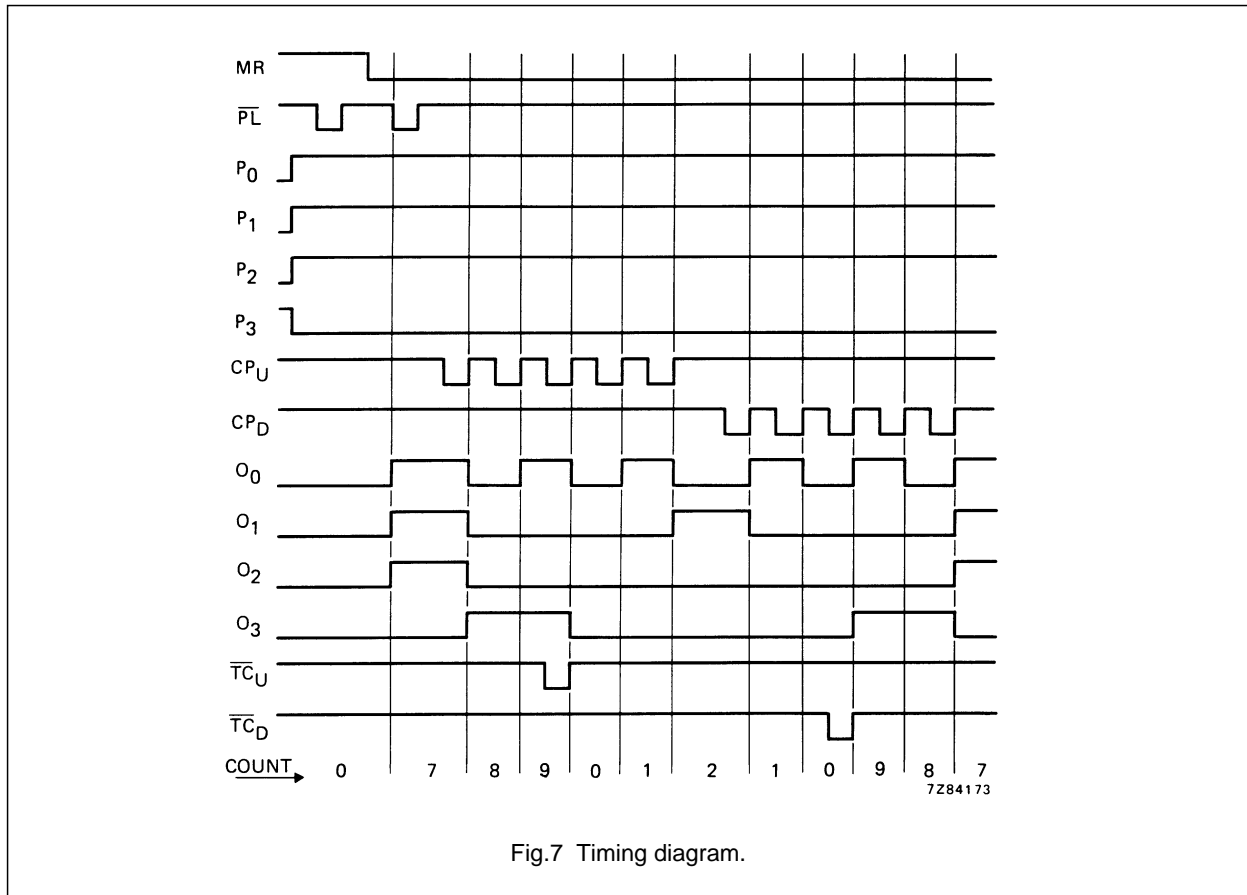


Fig.7 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF40192B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting.

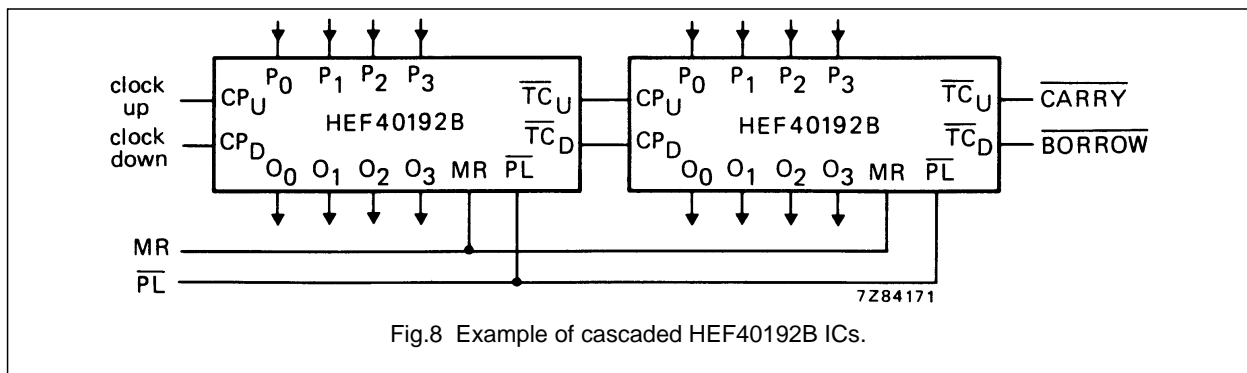


Fig.8 Example of cascaded HEF40192B ICs.