

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4538

Dual retriggerable precision
monostable multivibrator

Product specification
File under Integrated Circuits, IC06

September 1993

Dual retriggerable precision monostable multivibrator

74HC/HCT4538

FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I_{CC} category: MSI
- Power-on reset on-chip

GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ($\overline{nA_0}$), an active HIGH

trigger/retrigger input (nA_1), an overriding active LOW direct reset input ($\overline{nR_D}$), an output (nQ) and its complement (\overline{nQ}), and two pins (nC_{TC} and nRC_{TC}) for connecting the external timing components C_t and R_t . Typical pulse width variation over temperature range is $\pm 0.2\%$.

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components C_t and R_t . The output pulse width (T) is equal to $0.7 \times R_t \times C_t$. The linear design techniques guarantee precise control of the output pulse width.

A LOW level at $\overline{nR_D}$ terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay $\overline{nA_0}$, nA_1 to nQ , \overline{nQ} | C _L = 15 pF; V _{CC} = 5 V | 27 | 30 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per multivibrator | notes 1 and 2 | 136 | 138 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC} \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

D = duty factor in %

C_{EXT} = timing capacitance in pF

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

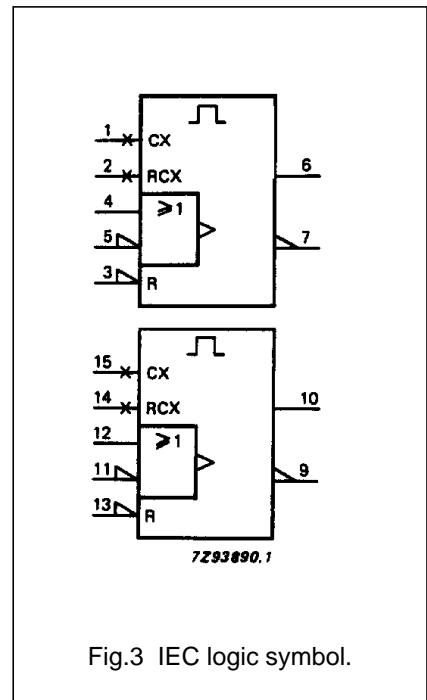
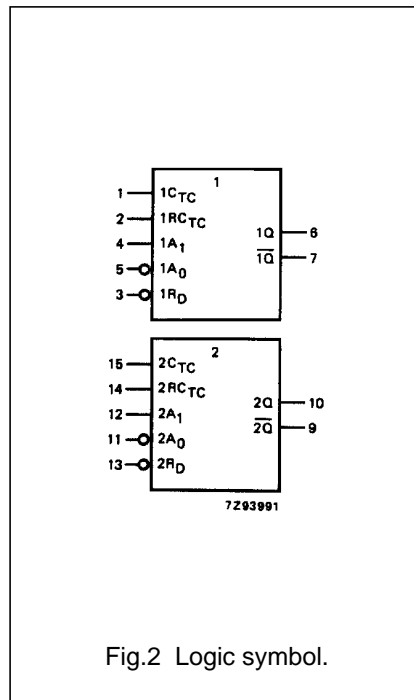
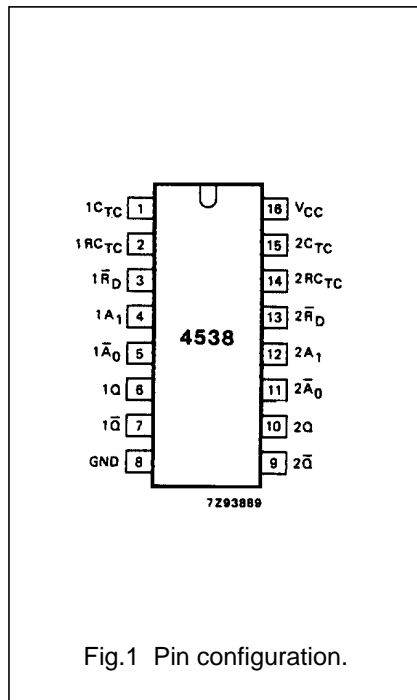
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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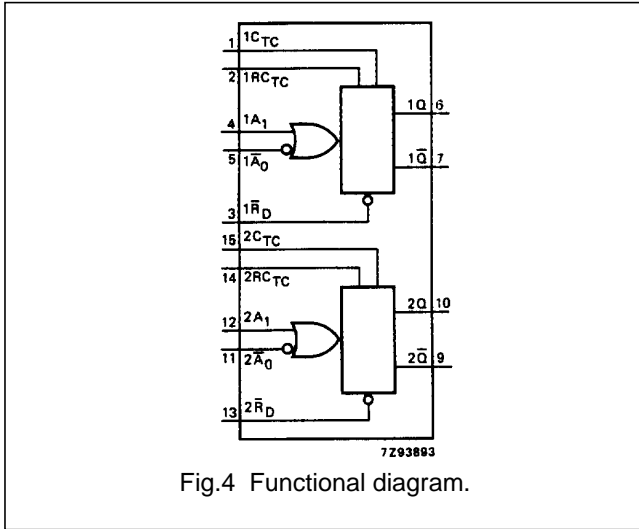
PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|---------|--------------------------|--|
| 1, 15 | $1C_{TC}, 2C_{TC}$ | external capacitor connections |
| 2, 14 | $1RC_{TC}, 2RC_{TC}$ | external resistor/capacitor connections |
| 3, 13 | $1\bar{R}_D, 2\bar{R}_D$ | direct reset inputs (active LOW) |
| 4, 12 | $1A_1, 2A_1$ | trigger inputs (LOW-to-HIGH, edge-triggered) |
| 5, 11 | $1\bar{A}_0, 2\bar{A}_0$ | trigger inputs (HIGH-to-LOW, edge-triggered) |
| 6, 10 | $1Q, 2Q$ | pulse outputs |
| 7, 9 | $1\bar{Q}, 2\bar{Q}$ | complementary pulse outputs |
| 8 | GND | ground (0 V) |
| 16 | V_{CC} | positive supply voltage |



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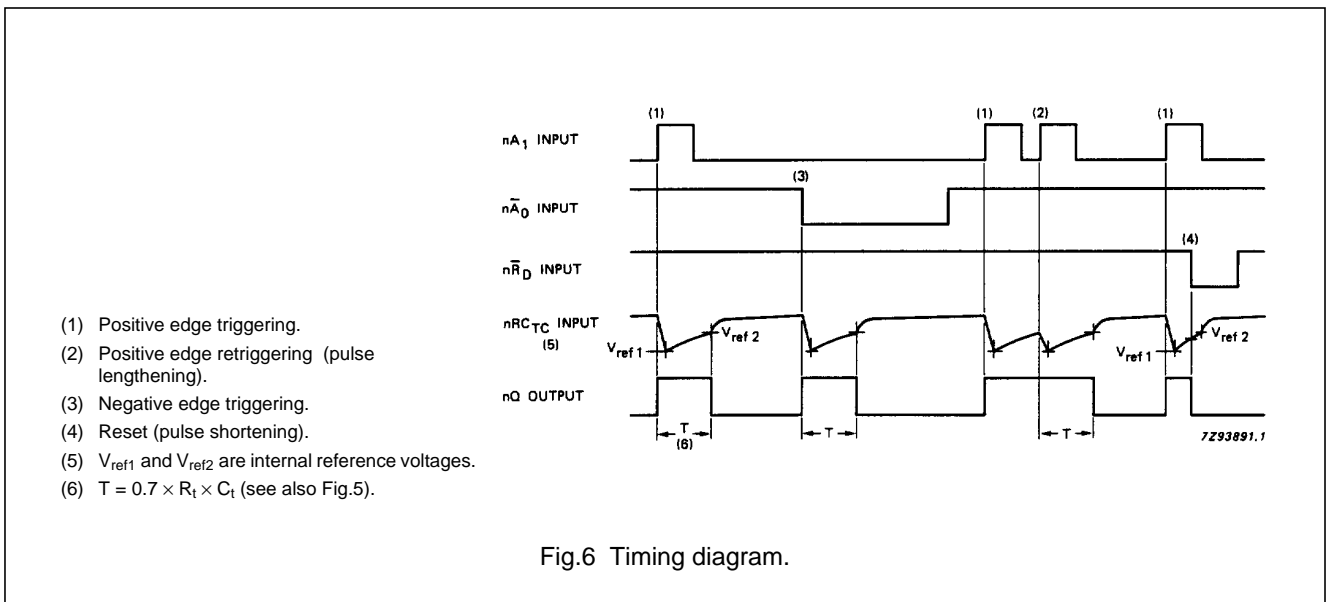
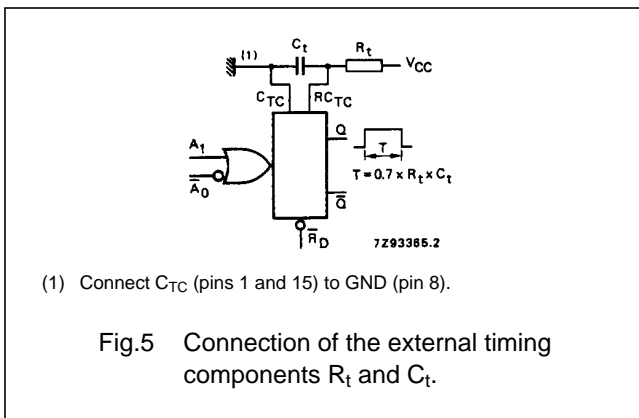


FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|--------------|--------|--------------|---------|------------|
| $n\bar{A}_0$ | nA_1 | $n\bar{R}_D$ | nQ | $n\bar{Q}$ |
| ↓ | L | H | | |
| H | ↑ | H | | |
| X | X | L | L | H |

Notes

- H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
 = one HIGH level output pulse
 = one LOW level output pulse



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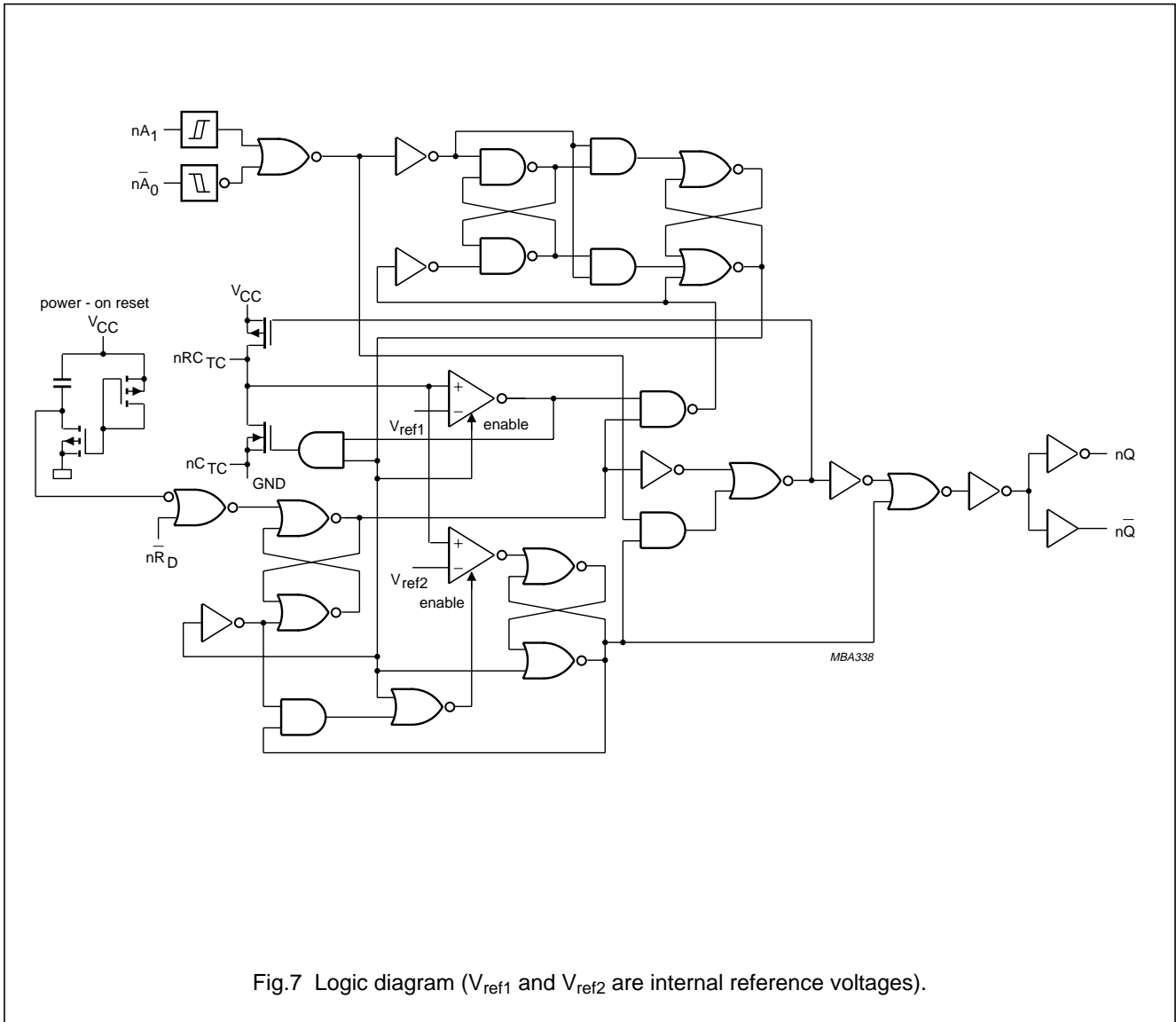


Fig.7 Logic diagram (V_{ref1} and V_{ref2} are internal reference voltages).

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DC CHARACTERISTICS FOR 74HCFor the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

 I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------|---|----------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|-------------------|--|
| | | 74HC | | | | | | | | V_{CC} (V) | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t_{PLH} | propagation delay nA_0, nA_1 to nQ | | 85 31 25 | 265 53 45 | | 330 66 56 | | 400 80 68 | ns | 2.0 4.5 6.0 | Fig.8 |
| t_{PHL} | propagation delay nA_0, nA_1 to $n\bar{Q}$ | | 83 30 24 | 265 53 45 | | 330 66 56 | | 400 80 68 | ns | 2.0 4.5 6.0 | Fig.8 |
| t_{PHL} | propagation delay $n\bar{R}_D$ to nQ | | 80 29 23 | 265 53 45 | | 330 66 56 | | 400 80 68 | ns | 2.0 4.5 6.0 | Fig.8 |
| t_{PLH} | propagation delay $n\bar{R}_D$ to $n\bar{Q}$ | | 83 30 24 | 265 53 45 | | 340 68 58 | | 400 80 68 | ns | 2.0 4.5 6.0 | Fig.8 |
| t_{THL}/t_{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.8 |
| t_W | $n\bar{A}_0$ pulse width LOW | 80 16 14 | 17 6 5 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t_W | nA_1 pulse width HIGH | 80 16 14 | 17 6 5 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t_W | $n\bar{R}_D$ pulse width LOW | 80 16 14 | 19 7 6 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t_W | $nQ, n\bar{Q}$ pulse width HIGH or LOW | 0.63 | 0.70 | 0.77 | 0.602 | 0.798 | 0.595 | 0.805 | ms | 5.0 | Fig.8; $R_t = 10$ k Ω ; $C_t = 0.1$ μ F |
| t_{rem} | removal time \bar{R}_D to $n\bar{A}_0, nA_1$ | 35 7 6 | 6 2 2 | | 45 9 8 | | 55 11 9 | | ns | 2.0 4.5 6.0 | Fig.8 |

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| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|------------------|---|-----------------------|-------|--------------|------------|------|-------------|------|------|------------------------|---|
| | | 74HC | | | | | | | | V _{CC} (V) | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{rt} | retrigger time nĀ ₀ , nA ₁ | – | 455+X | | – | | – | | ns | 2.0 4.5 6.0 | Fig.8 X = C _{EXT} / (4.5 × V _{CC}) |
| R _{EXT} | external timing resistor | 10 2 | | 1000 1000 | | | | | kΩ | 2.0 5.0 | |
| C _{EXT} | external timing capacitor | no limits | | | | | | | pF | 5.0 | |

NON-STANDARD DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | | |
|-----------------|---|-----------------------|------|------|------------|------|-------------|------|------|------------------------|-----------------------|-----------------------------------|
| | | 74HC | | | | | | | | V _{CC} (V) | V _I (V) | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| ±I _I | input leakage current nRC _{EXT} | | | 0.5 | | 5.0 | | 10.0 | μA | 6.0 | 2.0 or GND | V _{CC} or GND; note 1 |

Note

1. This measurement can only be carried out after a trigger pulse is applied.

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------------------|-----------------------|
| $\overline{nA_0}$, nA_1 | 0.50 |
| nR_D | 0.65 |

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|--|-----------------------|------|------|------------|-------|-------------|-------|------|------|---|-------|------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | OTHER | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | min. | | | | max. |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | | |
| t _{PLH} | propagation delay $\overline{nA_0}$, nA_1 to nQ | | 35 | 60 | | 75 | | 90 | ns | 4.5 | Fig.8 | | |
| t _{PHL} | propagation delay $\overline{nA_0}$, nA_1 to \overline{nQ} | | 35 | 60 | | 75 | | 90 | ns | 4.5 | Fig.8 | | |
| t _{PHL} | propagation delay nR_D to nQ | | 35 | 60 | | 75 | | 90 | ns | 4.5 | Fig.8 | | |
| t _{PLH} | propagation delay nR_D to \overline{nQ} | | 35 | 60 | | 75 | | 90 | ns | 4.5 | Fig.8 | | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 21 | ns | 4.5 | Fig.8 | | |
| t _W | $\overline{nA_0}$ pulse width LOW | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig.8 | | |
| t _W | nA_1 pulse width HIGH | 16 | 5 | | 20 | | 24 | | ns | 4.5 | Fig.8 | | |
| t _W | $\overline{nR_D}$ pulse width LOW | 20 | 11 | | 25 | | 30 | | ns | 4.5 | Fig.8 | | |
| t _W | nQ, \overline{nQ} pulse width HIGH or LOW | 0.63 | 0.70 | 0.77 | 0.602 | 0.798 | 0.595 | 0.805 | ms | 5.0 | Fig.8; R _t = 10 kΩ; C _t = 0.1 μF | | |
| t _{rem} | removal time $\overline{R_D}$ to $\overline{nA_0}$, nA_1 | 7 | 2 | | 9 | | 11 | | ns | 4.5 | Fig.8 | | |
| t _{rt} | retrigger time $\overline{nA_0}$, nA_1 | – | 80+X | | – | | – | | ns | 4.5 | Fig.8 X = C _{EXT} / (4.5 × V _{CC}) | | |
| R _{EXT} | external timing resistor | 2 | | 1000 | | | | | kΩ | 5.0 | | | |
| C _{EXT} | external timing capacitor | no limits | | | | | | | pF | 5.0 | | | |

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NON-STANDARD DC CHARACTERISTICS FOR 74HCT

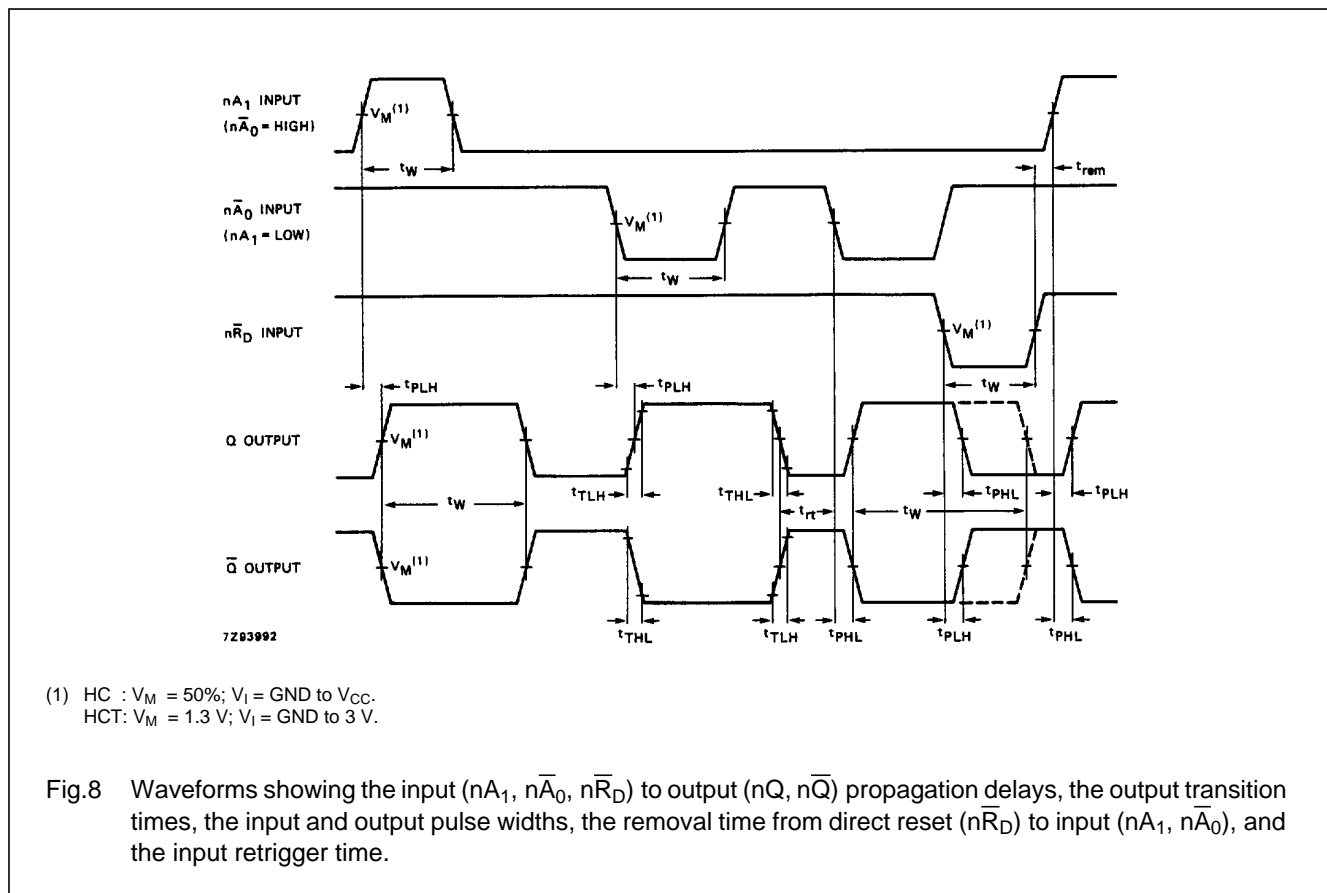
Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | | |
|-----------------|---|-----------------------|-----|------|------------|------|-------------|------|----|------|------------------------|-----------------------------------|-------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | V _I (V) | OTHER |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | | |
| | | min. | typ | max. | min. | max. | min. | max. | | | | | |
| ±I _I | input leakage current nRC _{EXT} | | | 0.5 | | 5.0 | | 10.0 | µA | 5.5 | 2.0 or GND | V _{CC} or GND; note 1 | |

Note

1. This measurement can only be carried out after a trigger pulse is applied.

AC WAVEFORMS



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APPLICATION INFORMATION

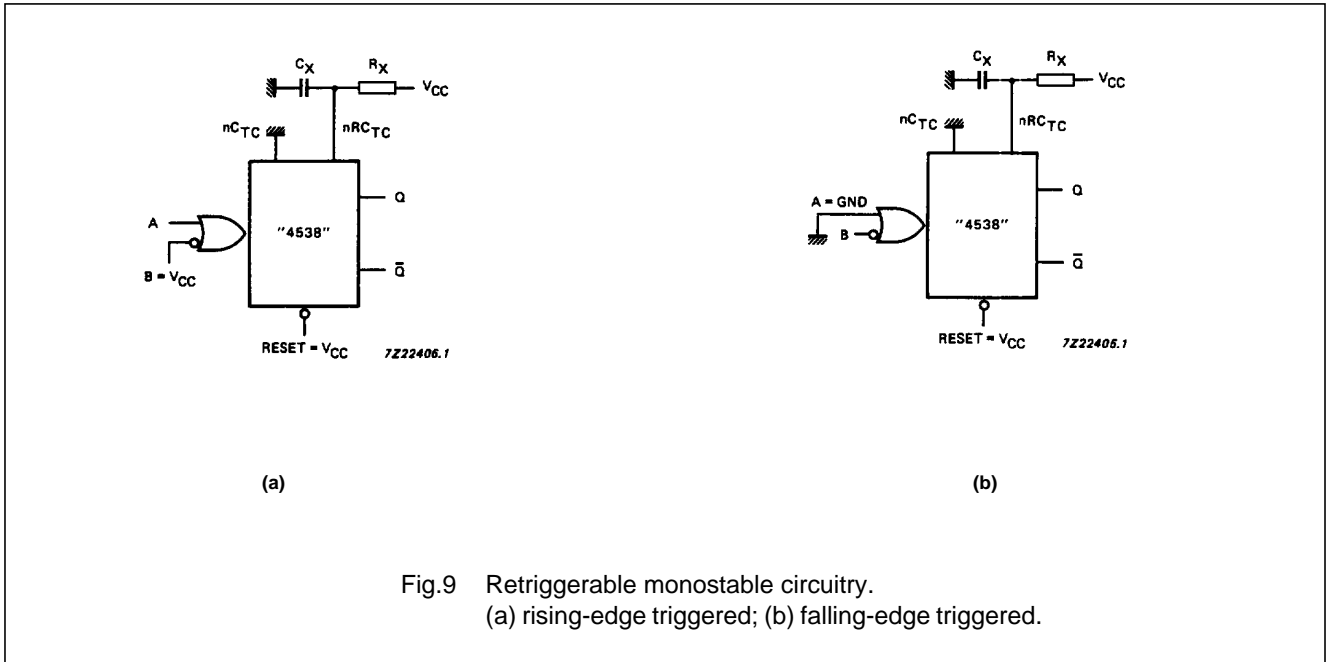


Fig.9 Retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.

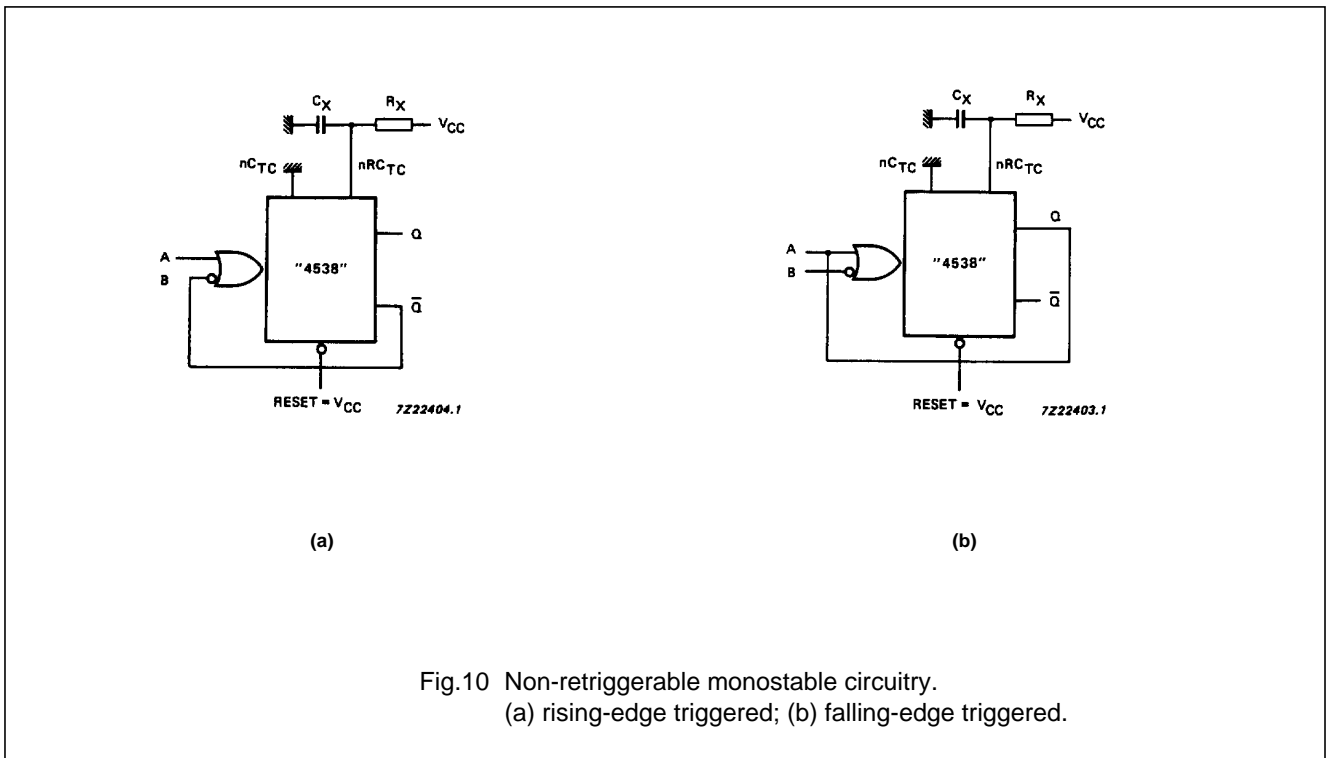


Fig.10 Non-retriggerable monostable circuitry.
(a) rising-edge triggered; (b) falling-edge triggered.

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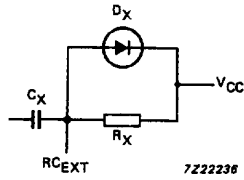


Fig.11 Power-down protection circuit.

Power-down considerations

A large capacitor (C_X) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of V_{CC} to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode (D_X) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig.11.

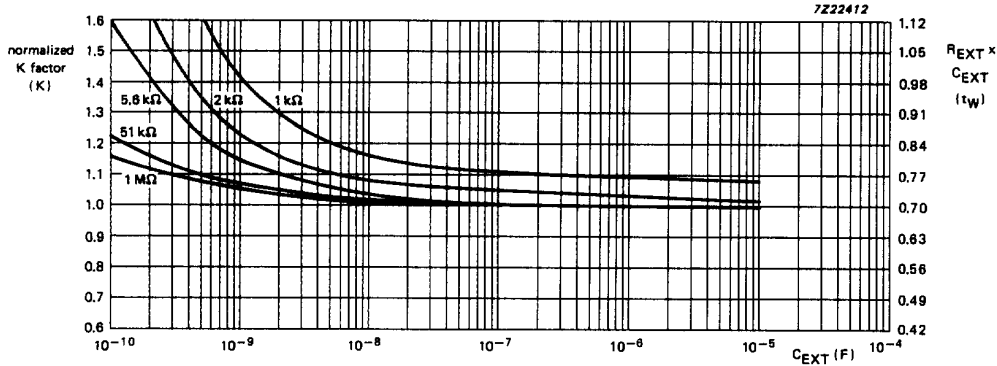


Fig.12 Typical pulse width accuracy versus external capacitance; $V_{CC} = 4.5 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

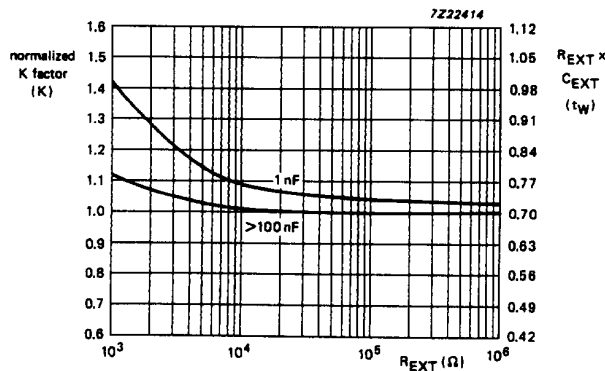
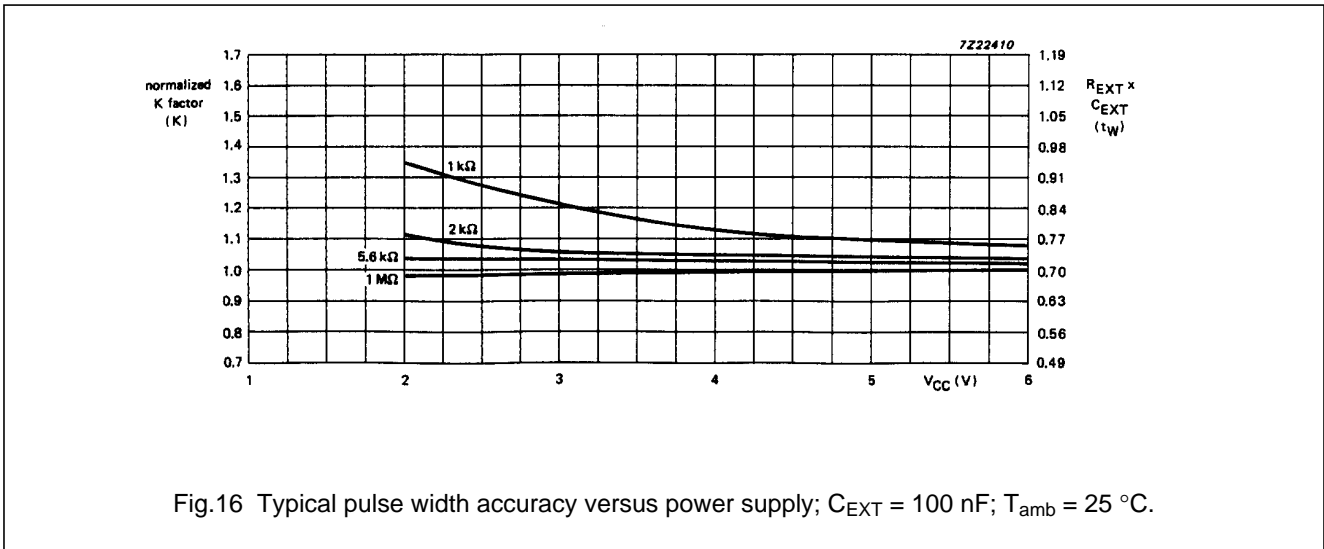
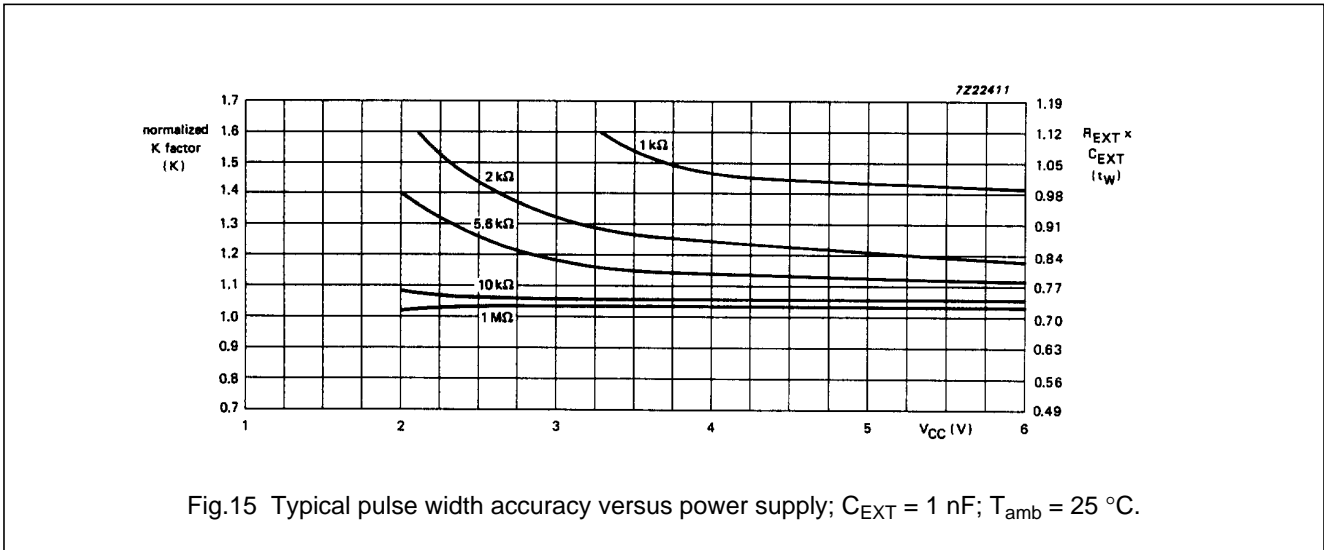
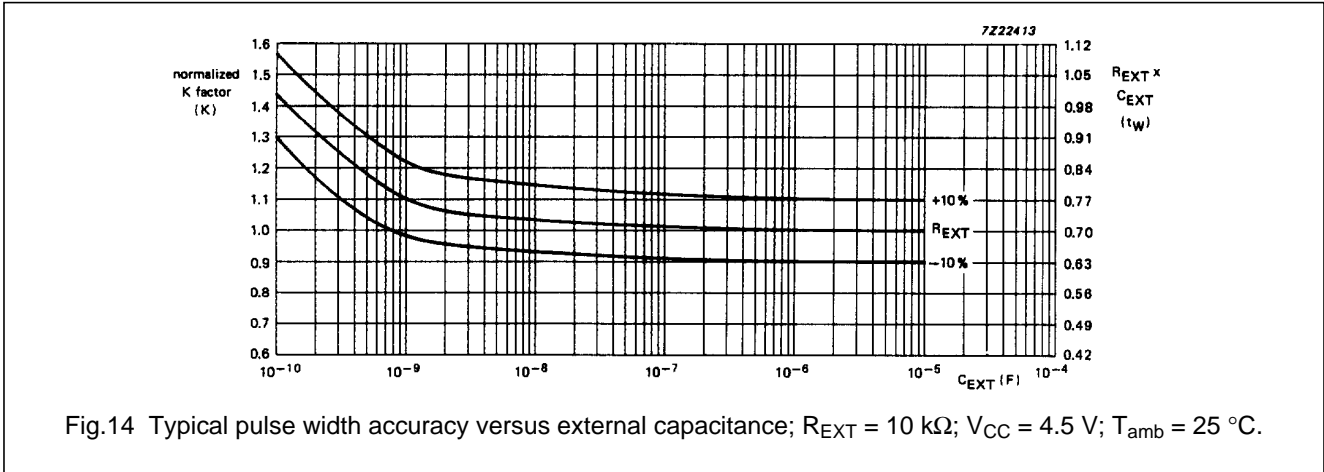


Fig.13 Typical pulse width accuracy versus external resistance; $V_{CC} = 4.5 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$.

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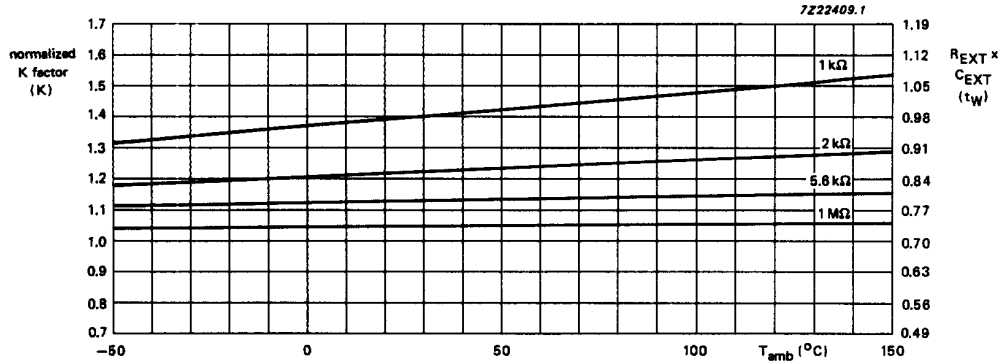


Fig.17 Typical pulse width accuracy versus temperature; $C_{EXT} = 1 \text{ nF}$; $V_{CC} = 4.5 \text{ V}$.

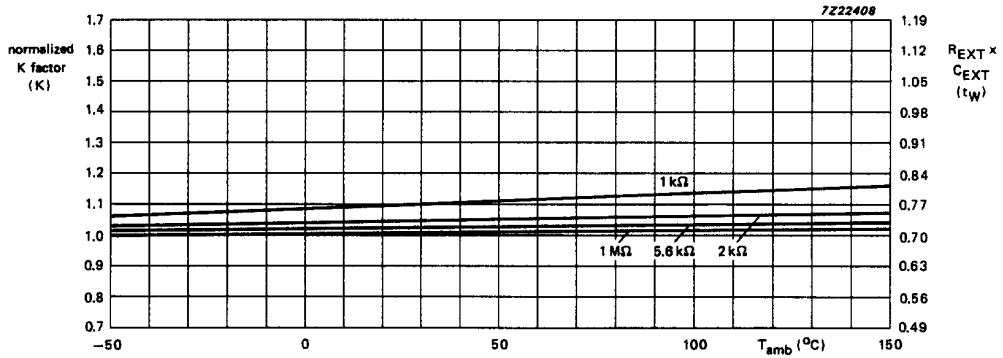


Fig.18 Typical pulse width accuracy versus temperature; $C_{EXT} = 1 \text{ } \mu\text{F}$; $V_{CC} = 4.5 \text{ V}$.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".