DATA SHEET

74HC4066; 74HCT4066
Quad bilateral switches

Product specification
Supersedes data of 2003 Jun 17

2004 Nov 11

Philips
Semiconductors

FEATURES

- Very low ON-resistance:
  - 50 Ω (typical) at V_{CC} = 4.5 V
  - 45 Ω (typical) at V_{CC} = 6.0 V
  - 35 Ω (typical) at V_{CC} = 9.0 V.
- Complies with JEDEC standard no. 7A
- ESD protection:
  HBM EIA/JESD22-A114-B exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

GENERAL DESCRIPTION

The 74HC4066 and 74HCT4066 are high-speed Si-gate CMOS devices and are pin compatible with the HEF4066B. They are specified in compliance with JEDEC standard no. 7A.

The 74HC4066 and 74HCT4066 have four independent analog switches. Each switch has two input/output pins (pins nY or nZ) and an active HIGH enable input pin (pin nE). When pin nE = LOW the belonging analog switch is turned off.

The 74HC4066 and 74HCT4066 are pin compatible with the 74HC4016 and 74HCT4016 but exhibit a much lower on-resistance. In addition, the on-resistance is relatively constant over the full input signal range.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC4066	74HCT4066	
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	11	12	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	13	16	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per switch	notes 1 and 2	11	12	pF
C_S	maximum switch capacitance		8	8	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   C_S = maximum switch capacitance in pF;
   V_{CC} = supply voltage in V;
   N = number of inputs switching;
   $\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ = sum of the outputs.
2. For 74HC4066 the condition is V_I = GND to V_{CC}.
   For 74HCT4066 the condition is V_I = GND to V_{CC} – 1.5 V.

FUNCTION TABLE

See note 1.

INPUT nE	SWITCH
L	off
H	on

Note

1. H = HIGH voltage level.
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC4066N	–40 °C to 125 °C	14	DIP14	plastic	SOT27-1
74HCT4066N	–40 °C to 125 °C	14	DIP14	plastic	SOT27-1
74HC4066D	–40 °C to 125 °C	14	SO14	plastic	SOT108-1
74HCT4066D	–40 °C to 125 °C	14	SO14	plastic	SOT108-1
74HC4066DB	–40 °C to 125 °C	14	SSOP14	plastic	SOT337-1
74HCT4066DB	–40 °C to 125 °C	14	SSOP14	plastic	SOT337-1
74HC4066PW	–40 °C to 125 °C	14	TSSOP14	plastic	SOT402-1
74HCT4066PW	–40 °C to 125 °C	14	TSSOP14	plastic	SOT402-1
74HC4066BQ	–40 °C to 125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT4066BQ	–40 °C to 125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1Y	independent input/output
2	1Z	independent input/output
3	2Z	independent input/output
4	2Y	independent input/output
5	2E	enable input (active HIGH)
6	3E	enable input (active HIGH)
7	GND	ground (0 V)
8	3Y	independent input/output
9	3Z	independent input/output
10	4Z	independent input/output
11	4Y	independent input/output
12	4E	enable input (active HIGH)
13	1E	enable input (active HIGH)
14	V_{CC}	supply voltage

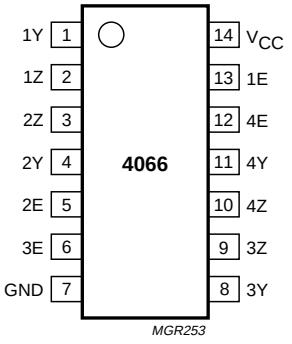
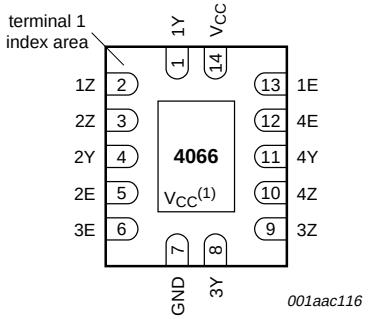


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

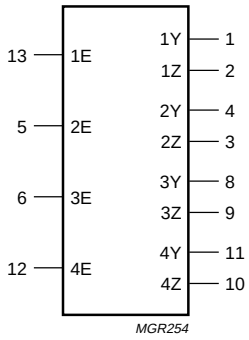


Fig.3 Logic symbol.

Fig.4 IEEEC logic symbol.

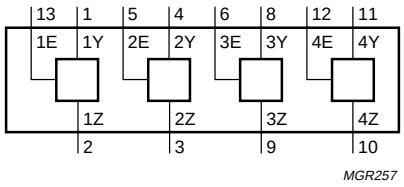


Fig.5 Functional diagram.

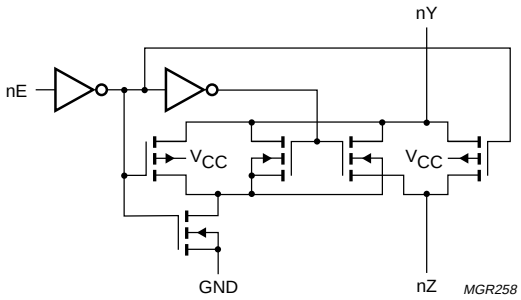


Fig.6 Schematic diagram (one switch).

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC4066			74HCT4066			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	10.0	4.5	5.0	5.5	V
V_I	input voltage		GND	–	V_{CC}	GND	–	V_{CC}	V
V_S	switch voltage		GND	–	V_{CC}	GND	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+85	–40	+25	+85	°C
			–40	–	+125	–40	–	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	6.0	1000	–	6.0	500	ns
		V_{CC} = 4.5 V	–	–	500	–	–	–	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns
		V_{CC} = 10.0 V	–	–	250	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+11.0	V
I_{IK}	input diode current	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V	–	±20	mA
I_{SK}	switch diode current	$V_S < –0.5$ V or $V_S > V_{CC} + 0.5$ V	–	±20	mA
I_S	switch current	$–0.5 \text{ V} < V_O < V_{CC} + 0.5$ V; note 1	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C; note 2	–	500	mW
P_S	power dissipation per switch		–	100	mW

Notes

1. To avoid drawing V_{CC} current out of pin nZ, when switch current flows in pin nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into pin nZ, no V_{CC} current will flow out of pin nY. In this case there is no limit for the voltage drop across the switch, but the voltages at pins nY and nZ may not exceed V_{CC} or GND.
2. For DIP14 packages: above 70 °C derate linearly with 12 mW/K.

   For SO14 packages: above 70 °C derate linearly with 8 mW/K.

   For SSOP14 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

   For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

DC CHARACTERISTICS

Family 74HC4066

Voltages are referenced to GND (ground = 0 V); V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nY or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
			9.0	6.3	4.7	–	V
V_{IL}	LOW-level input voltage		2.0	–	0.8	0.50	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.80	V
			9.0	–	4.3	2.70	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	µA
			10.0	–	–	±2.0	µA
$I_{S(OFF)}$	analog switch current OFF-state	per channel; V_I = V_{IH} or V_{IL}; V_S = V_{CC} − GND; see Fig.7	10.0	–	–	±1.0	µA
$I_{S(ON)}$	analog switch current ON-state	V_I = V_{IH} or V_{IL}; V_S = V_{CC} − GND; see Fig.8	10.0	–	–	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND	6.0	–	–	20.0	µA
			10.0	–	–	40.0	µA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
			9.0	6.3	–	–	V
V_{IL}	LOW-level input voltage		2.0	–	–	0.50	V
			4.5	–	–	1.35	V
			6.0	–	–	1.80	V
			9.0	–	–	2.70	V
I_{LI}	input leakage current	V_I = V_{CC} or GND	6.0	–	–	±1.0	µA
			10.0	–	–	±2.0	µA
$I_{S(OFF)}$	analog switch current OFF-state	per channel; V_I = V_{IH} or V_{IL}; V_S = V_{CC} – GND; see Fig.7	10.0	–	–	±1.0	µA
$I_{S(ON)}$	analog switch current ON-state	V_I = V_{IH} or V_{IL}; V_S = V_{CC} – GND; see Fig.8	10.0	–	–	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = GND or V_{CC}; V_{os} = V_{CC} or GND	6.0	–	–	40.0	µA
			10.0	–	–	80.0	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Family 74HCT4066

Voltages are referenced to GND (ground = 0 V); V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nY or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	±1.0	μA
$I_{S(OFF)}$	analog switch current OFF-state	per channel; $V_I = V_{IH}$ or V_{IL}; $V_S = V_{CC} - GND$; see Fig.7	5.5	–	–	±1.0	μA
$I_{S(ON)}$	analog switch current ON-state	$V_I = V_{IH}$ or V_{IL}; $V_S = V_{CC} - GND$; see Fig.8	5.5	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND	4.5 to 5.5	–	–	20.0	μA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND	4.5 to 5.5	–	100	450	μA
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V_{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND	5.5	–	–	±1.0	μA
$I_{S(OFF)}$	analog switch current OFF-state	per channel; $V_I = V_{IH}$ or V_{IL}; $V_S = V_{CC} - GND$; see Fig.7	10.0	–	–	±1.0	μA
$I_{S(ON)}$	analog switch current ON-state	$V_I = V_{IH}$ or V_{IL}; $V_S = V_{CC} - GND$; see Fig.8	10.0	–	–	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; V_{is} = GND or V_{CC}; $V_{os} = V_{CC}$ or GND	4.5 to 5.5	–	–	40.0	μA
ΔI_{CC}	additional quiescent supply current per input	$V_I = V_{CC} - 2.1$ V; other inputs at V_{CC} or GND	4.5 to 5.5	–	–	490	μA

Note

1. All typical values are measured at T_{amb} = 25 °C.

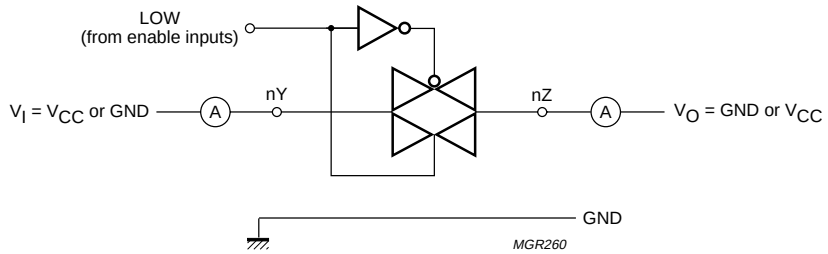


Fig.7 Test circuit for measuring OFF-state current.

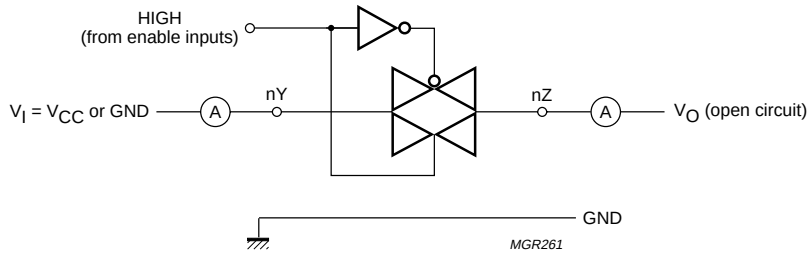


Fig.8 Test circuit for measuring ON-state current.

Resistance R_{ON} for 74HC4066 and 74HCT4066

For 74HC4066: V_{CC} = 2.0, 4.5, 6.0 and 9.0 V; for 74HCT4066: V_{CC} = 4.5 V; note 1; V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; see Fig.9.

SYMBOL	PARAMETER	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
		OTHER	I_S (μA)	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 2								
$R_{ON(peak)}$	ON-resistance (peak)	$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$ to GND	100	2.0	–	–	–	Ω
			1000	4.5	–	54	118	Ω
				6.0	–	42	105	Ω
				9.0	–	32	88	Ω
$R_{ON(rail)}$	ON-resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND	100	2.0	–	80	–	Ω
			1000	4.5	–	35	95	Ω
				6.0	–	27	82	Ω
				9.0	–	20	70	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$	100	2.0	–	100	–	Ω
			1000	4.5	–	42	106	Ω
				6.0	–	35	94	Ω
				9.0	–	27	78	Ω
ΔR_{ON}	maximum variation of ON-resistance between any two channels	$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$ to GND	–	2.0	–	–	–	Ω
				4.5	–	5	–	Ω
				6.0	–	4	–	Ω
				9.0	–	3	–	Ω
T_{amb} = −40 °C to +125 °C								
$R_{ON(peak)}$	ON-resistance (peak)	$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$ to GND	100	2.0	–	–	–	Ω
			1000	4.5	–	–	142	Ω
				6.0	–	–	126	Ω
				9.0	–	–	105	Ω
$R_{ON(rail)}$	ON-resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND	100	2.0	–	–	–	Ω
			1000	4.5	–	–	115	Ω
				6.0	–	–	100	Ω
				9.0	–	–	85	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$	100	2.0	–	–	–	Ω
			1000	4.5	–	–	128	Ω
				6.0	–	–	113	Ω
				9.0	–	–	95	Ω

Notes

1. At supply voltages approaching 2 V, the analog ON-resistance switch becomes extremely non-linear. Therefore, it is recommended that these devices are being used to transmit digital signals only, when using these supply voltages.
2. All typical values are measured at T_{amb} = 25 °C.

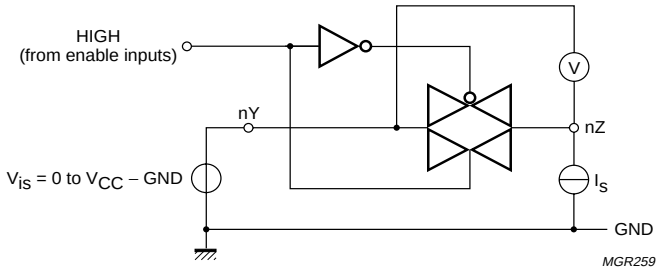
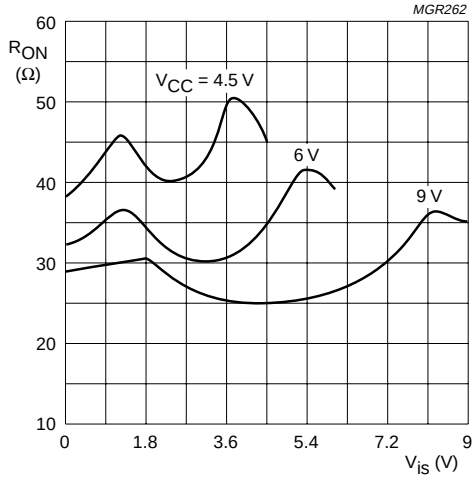


Fig.9 Test circuit for measuring ON-resistance (R_{ON}).



V_{is} = 0 V to V_{CC}.

Fig.10 Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}).

AC CHARACTERISTICS

Type 74HC4066

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nY or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	2.0	–	8	75	ns
			4.5	–	3	15	ns
			6.0	–	2	13	ns
			9.0	–	2	10	ns
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	2.0	–	36	125	ns
			4.5	–	13	25	ns
			6.0	–	10	21	ns
			9.0	–	8	16	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	2.0	–	44	190	ns
			4.5	–	16	38	ns
			6.0	–	13	33	ns
			9.0	–	16	26	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	2.0	–	–	90	ns
			4.5	–	–	18	ns
			6.0	–	–	15	ns
			9.0	–	–	12	ns
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	2.0	–	–	150	ns
			4.5	–	–	30	ns
			6.0	–	–	26	ns
			9.0	–	–	20	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	2.0	–	–	225	ns
			4.5	–	–	45	ns
			6.0	–	–	38	ns
			9.0	–	–	30	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT4066

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nY or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	4.5	–	3	15	ns
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	4.5	–	12	30	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	4.5	–	20	44	ns
T_{amb} = –40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞; see Fig.19	4.5	–	–	18	ns
t_{PZH}/t_{PZL}	turn-on time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	4.5	–	–	36	ns
t_{PHZ}/t_{PLZ}	turn-off time nE to V_{os}	R_L = 1 kΩ; see Figs 20 and 21	4.5	–	–	53	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

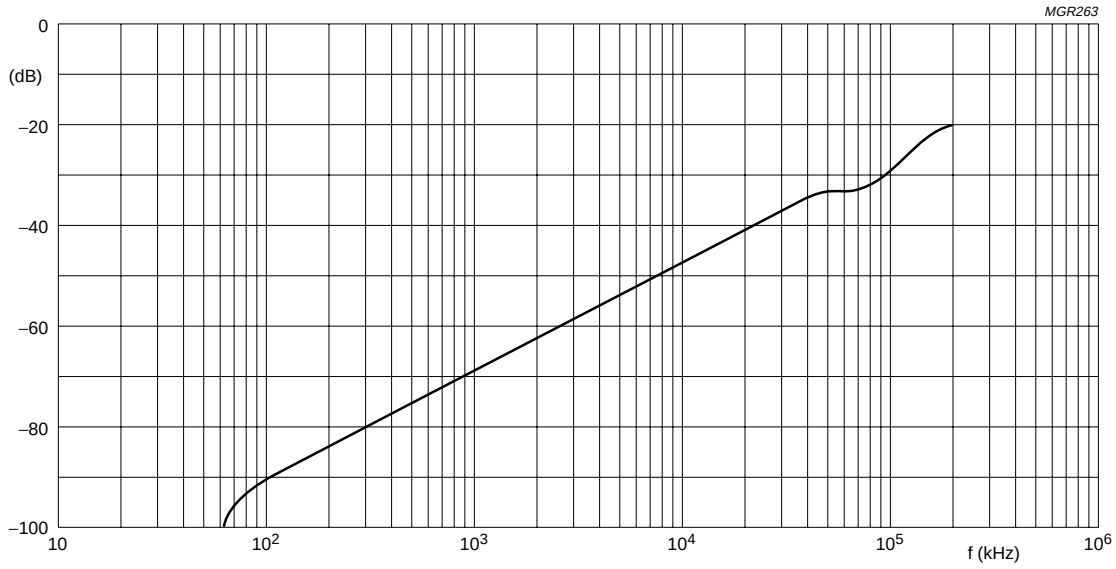
74HC4066 and 74HCT4066

At recommended conditions and typical values; GND = 0 V; $t_r = t_f$ = 6 ns; V_{is} is the input voltage at pins nY or nZ, whichever is assigned as an input; V_{os} is the output voltage at pins nY or nZ, whichever is assigned as an output.

SYMBOL	PARAMETER	CONDITIONS			TYP.	UNIT
		OTHER	$V_{is(p-p)}$ (V)	V_{CC} (V)		
d_{sin}	sine wave distortion	f = 1 kHz; R_L = 10 kΩ; C_L = 50 pF; see Fig.17	4.0	4.5	0.04	%
			8.0	9.0	0.02	%
		f = 10 kHz; R_L = 10 kΩ; C_L = 50 pF; see Fig.17	4.0	4.5	0.12	%
			8.0	9.0	0.06	%
$\alpha_{OFF(feedthr)}$	switch OFF signal feed-through	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz; see Figs 11 and 18	note 1	4.5	–50	dB
				9.0	–50	dB
$\alpha_{ct(s)}$	crosstalk between any two switches	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz; see Fig.13	note 1	4.5	–60	dB
				9.0	–60	dB
$V_{ct(p-p)}$	crosstalk voltage between any input to any switch (peak-to-peak value)	R_L = 600 Ω; C_L = 50 pF; f = 1 MHz; see Fig.15 (nE, square wave between V_{CC} and GND, $t_r = t_f$ = 6 ns)	–	4.5	110	mV
				9.0	220	mV
f_{max}	minimum frequency response (–3 dB)	R_L = 50 Ω; C_L = 10 pF; see Figs 12 and 16	note 2	4.5	180	MHz
				9.0	200	MHz
C_S	maximum switch capacitance		–	–	8	pF

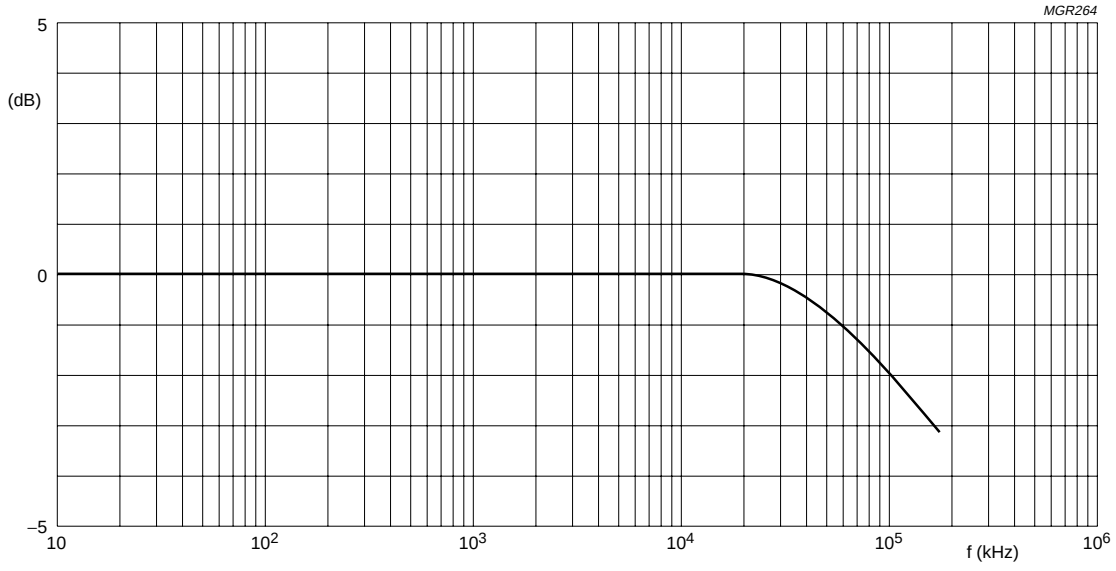
Notes

1. Adjust input voltage V_{is} is 0 dBM level (0 dBM = 1 mW into 600 Ω).
2. Adjust input voltage V_{is} is 0 dBM level at V_{os} for 1 MHz (0 dBM = 1 mW into 50 Ω).



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.11 Typical switch OFF signal feed-through as a function of frequency.



Test conditions: V_{CC} = 4.5 V; GND = 0 V; R_L = 50 Ω; R_{source} = 1 kΩ.

Fig.12 Typical frequency response.

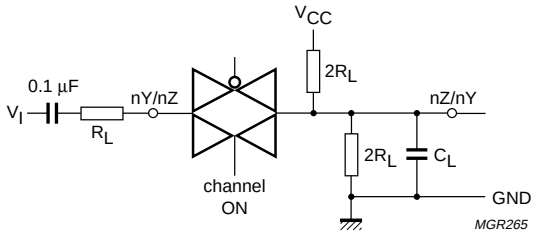


Fig.13 Test circuit for measuring crosstalk between any two switches; channels ON condition.

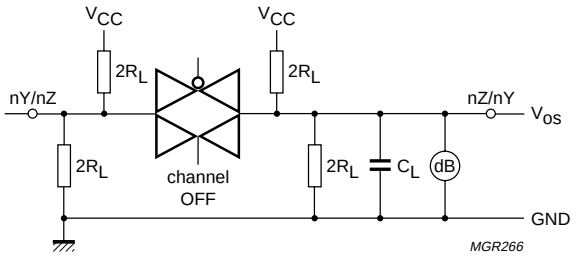


Fig.14 Test circuit for measuring crosstalk between any two switches; channels OFF condition.

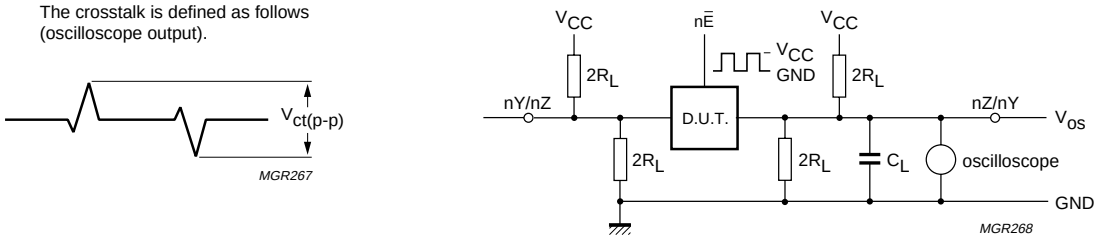
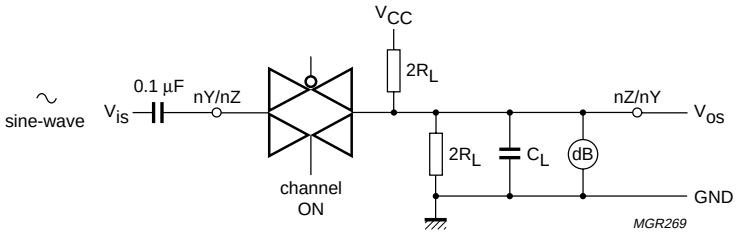


Fig.15 Test circuit for measuring crosstalk between control and any switch.



Adjust input voltage to obtain 0 dB at V_{os} when f_i = 1 MHz. After set-up, the frequency of f_i is increased to obtain a reading of -3 dB at V_{os}.

Fig.16 Test circuit for measuring minimum frequency response.

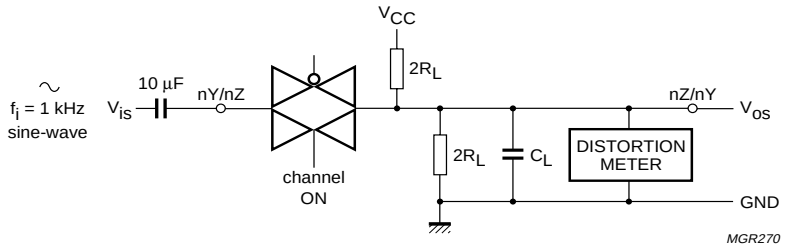


Fig.17 Test circuit for measuring sine wave distortion.

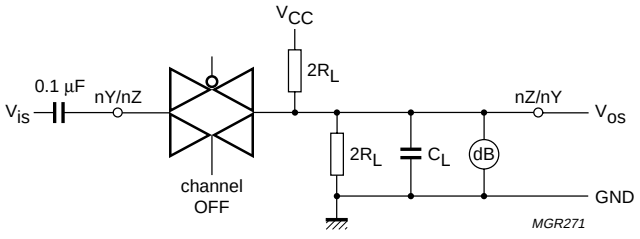


Fig.18 Test circuit for measuring switch OFF signal feed-through.

AC WAVEFORMS

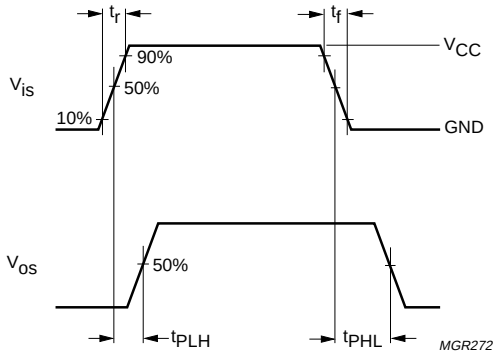
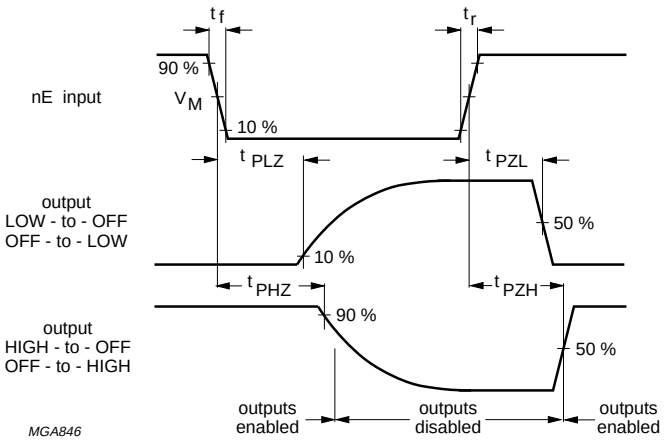


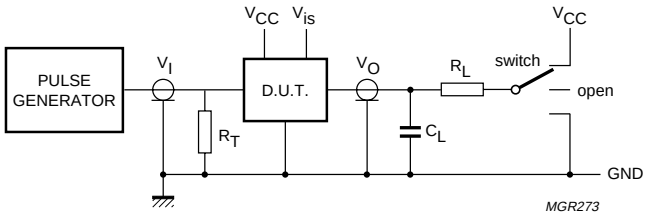
Fig.19 Waveforms showing the input (V_{is}) to output (V_{os}) propagation delays.



74HC4066: V_M = 50 %; V_I = GND to V_{CC}.
74HCT4066: V_M = 1.3 V; V_I = GND to 3 V.

Fig.20 Waveforms showing the turn-on and turn-off times.

TEST CIRCUIT AND WAVEFORMS



TEST	SWITCH	V_{is}
t_{PZH}	GND	V_{CC}
t_{PZL}	V_{CC}	GND
t_{PHZ}	GND	V_{CC}
t_{PLZ}	V_{CC}	GND
other	open	pulse

Definitions for test circuit:

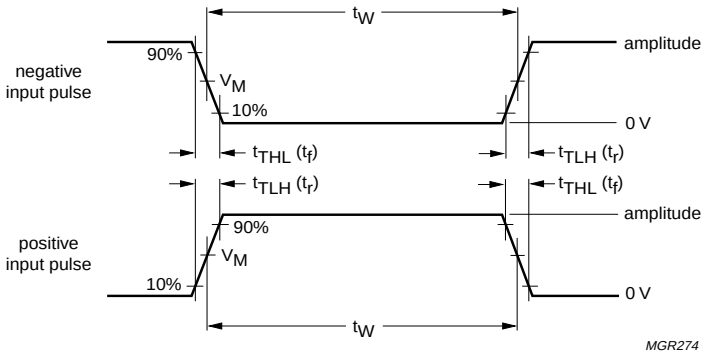
R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_f = 6 ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

Fig.21 Test circuit for measuring AC performance.

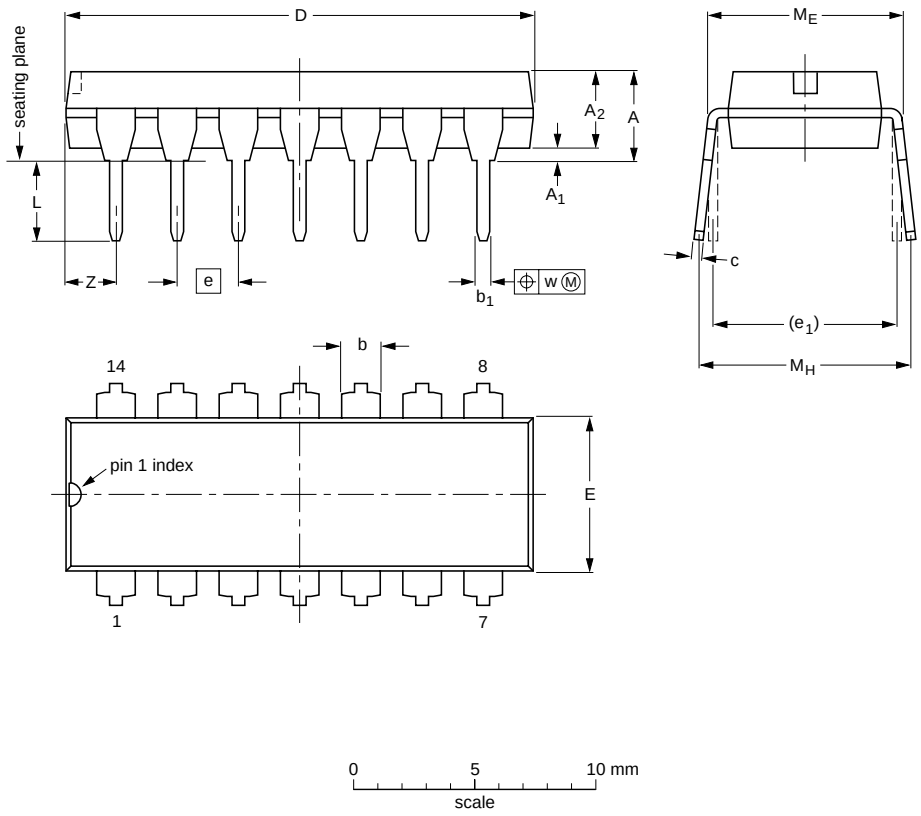


FAMILY	AMPLITUDE	V_M	t_r and t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC4066	V_{CC}	50 %	<2 ns	6 ns
74HCT4066	3.0 V	1.3 V	<2 ns	6 ns

Fig.22 Input pulse definitions.

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

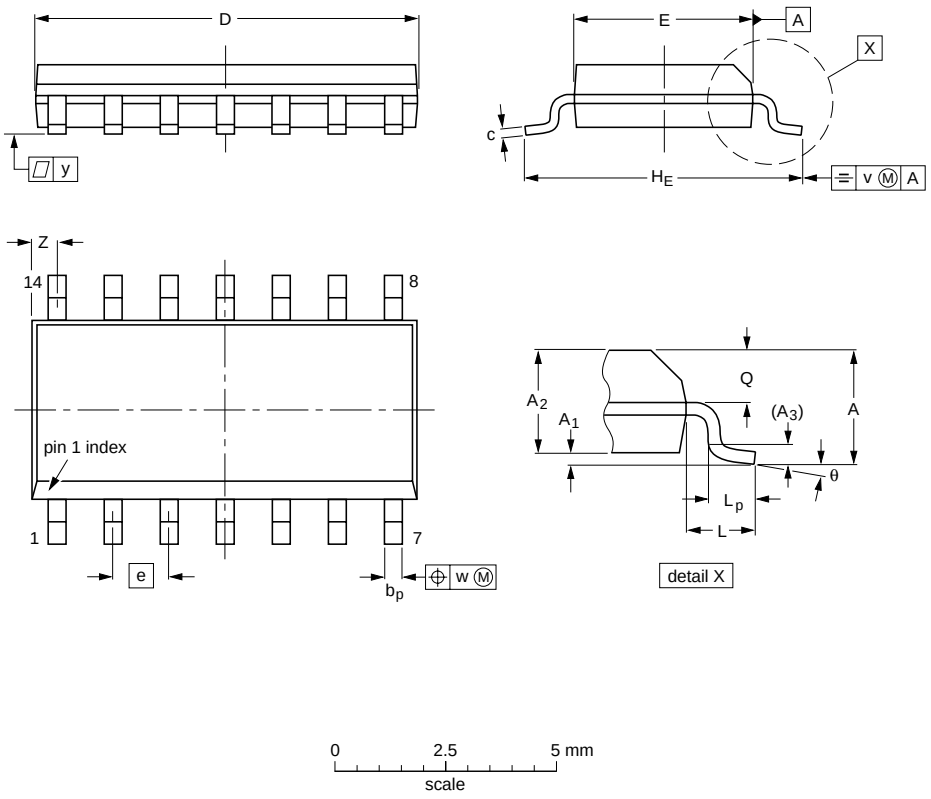
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

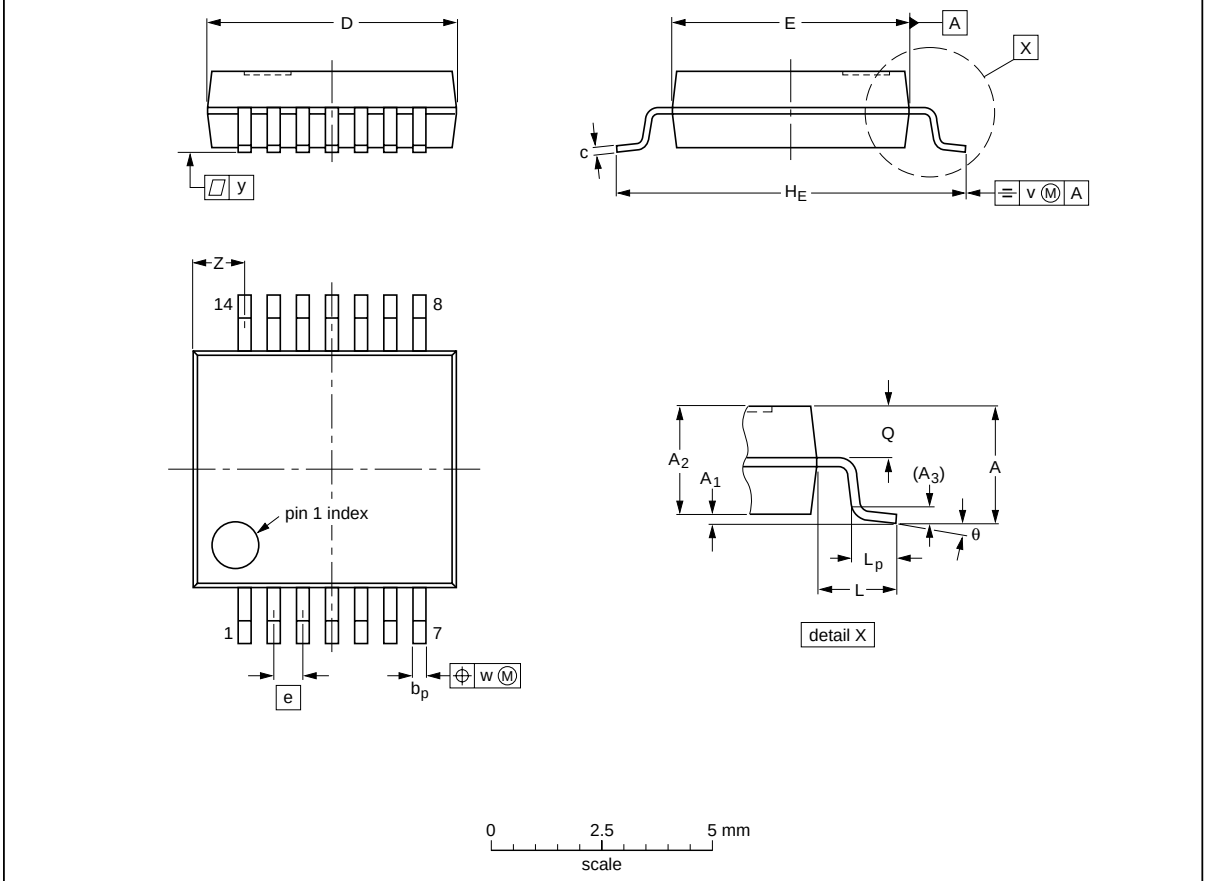
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

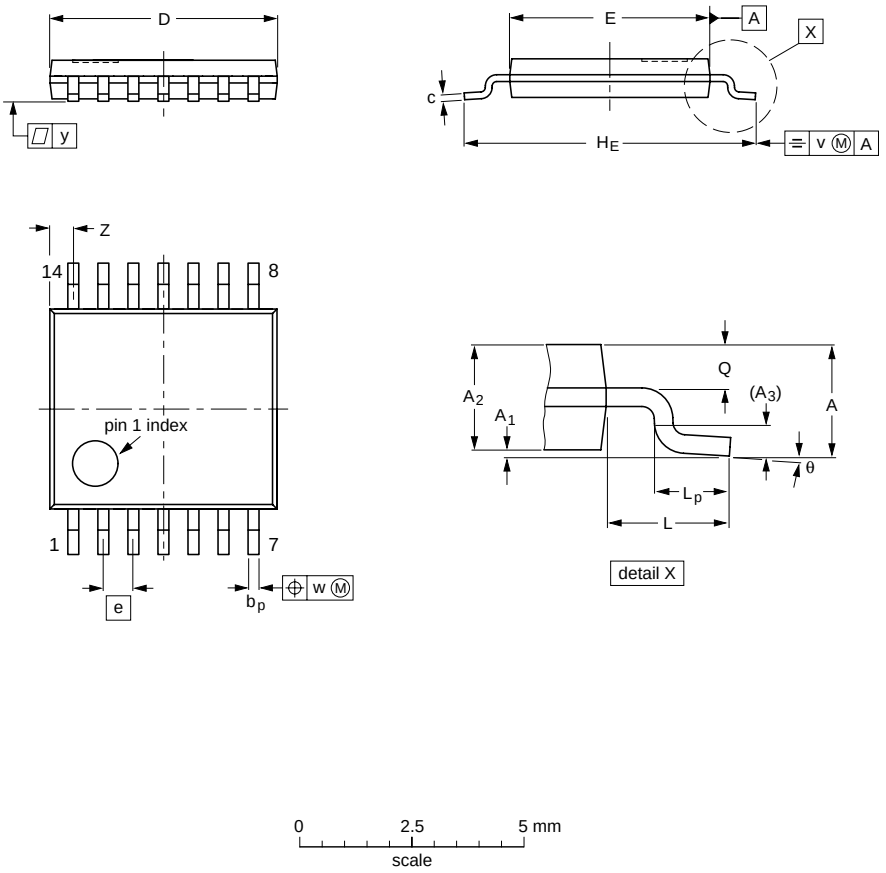
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

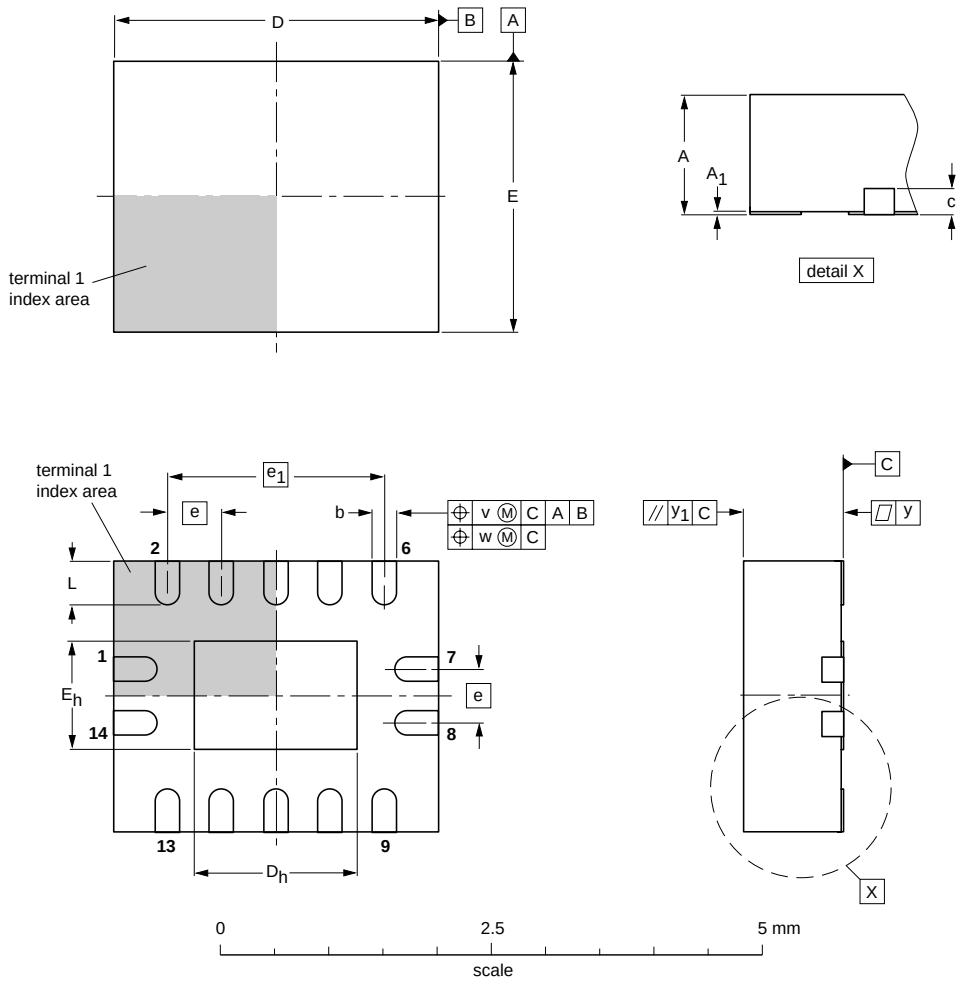
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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