FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C912
6-Digit BCD Display Controller/Driver

General Description

The MM74C912 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, ($\overline{CE}$), and WRITE ENABLE, ($\overline{WE}$), are LOW and is latched when either $\overline{CE}$ or $\overline{WE}$ return HIGH. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, ($\overline{OSE}$), which is tied LOW in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives an LED display through high drive (100 mA typ.) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, ($\overline{SOE}$), is LOW and go into 3-STATE when $\overline{SOE}$ is HIGH. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format.

All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

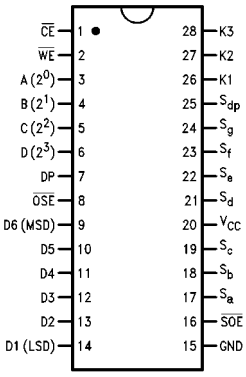
- Direct segment drive (100 mA typ.) 3-STATE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ.)
- Internal segment decoder
- TTL compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
MM74C912N	N28B	28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide

Connection Diagram

Dual-In-Line Package



Top View

Truth Tables

Input Control

$\overline{CE}$	Digit Address			$\overline{WE}$	Operation
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = Don't Care

Output Control

$\overline{SOE}$	$\overline{OSE}$	Operation
0	0	Refresh Display
0	1	Stop Oscillator (Note 1)
1	0	Disable Segment Outputs
1	1	Standby Mode

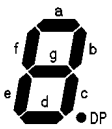
Note 1: Segment drive may exceed maximum display dissipation.

Functional Description

Character Font

MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	o	‾	-	_		.
Input A 2^0	X	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	1	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
OUTPUT ENABLE $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Segment Identification

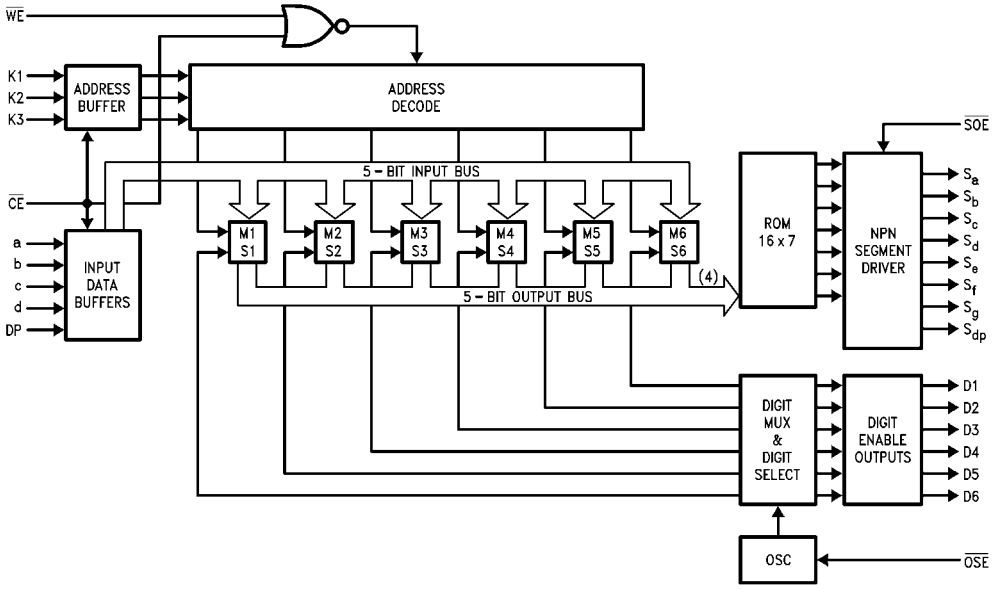


The MM74C912 display controller is manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an over-burdened microprocessor.

Block Diagram



Absolute Maximum Ratings (Note 2)

(Note 3)

Voltage at Any Pin Except Inputs	–0.3V to V_{CC} + 0.3V
Voltage at Any Input	–0.3V to +15V
Operating Temperature Range (T_A)	–40°C to +85°C
Storage Temperature Range (T_S)	–65°C to +150°C
Power Dissipation (P_D)	Refer to $P_{D\ MAX}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum (V_{CC})	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: All voltages reference to ground.

DC Electrical Characteristics

Min/Max limits apply at 40°C ≤ T_J ≤ 85°C, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	–1.0	–0.005		µA
I_{CC}	Supply Current	V_{CC} = 5V, Outputs Open		0.5	2	mA
I_{OUT}	3-STATE Output Current	V_{CC} = 5V, V_O = 5V		0.03	10	µA
		V_{CC} = 5V, V_O = 0V	–10	–0.03		µA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} – 2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	V_{CC} = 5V, V_O = 3.4V				
		T_J = 25°C	–60	–100		mA
		T_J = 100°C	–40	–60		mA
I_{DH}	High Level Digit Current	V_{CC} = 5V, V_O = 1V				
		T_J = 25°C	–10	–20		mA
		T_J = 100°C	–7	–15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	V_{CC} = 5V, I_O = –360µA	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Digit	V_{CC} = 5V, I_O = 360µA			0.4	V
θ_{JA}	Thermal Resistance	(Note 4)		100		°C/W

Note 4: θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics (Note 5)

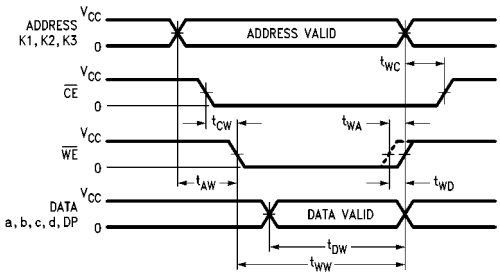
V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

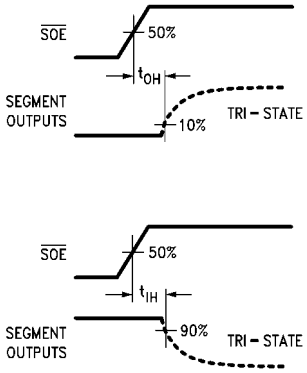
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CW}	Chip Enable to Write	T_J = 25°C	35	15		ns
	Enable Setup Time	T_J = 125°C	50	20		ns
t_{AW}	Address to Write	T_J = 25°C	35	15		ns
	Enable Setup Time	T_J = 125°C	50	20		ns
t_{WW}	Write Enable Width	T_J = 25°C	400	225		ns
		T_J = 125°C	450	250		ns
t_{DW}	Data to Write Enable	T_J = 25°C	390	225		ns
	Setup Time	T_J = 125°C	430	250		ns
t_{WD}	Write Enable to Data	T_J = 25°C	0	–10		ns
	Hold Time	T_J = 125°C	0	–15		ns
t_{WA}	Write Enable to Address	T_J = 25°C	0	–10		ns
	Hold Time	T_J = 125°C	0	–15		ns
t_{WC}	Write Enable to Chip Enable	T_J = 25°C	50	30		ns
	Hold Time	T_J = 125°C	75	40		ns
t_{1H}, t_{0H}	Logical “1”, Logical “0”	R_L = 10k, T_J = 25°C		275	500	ns
	Levels into 3-STATE	C_L = 10 pF, T_J = 125°C		325	600	ns
t_{H1}, t_{H0}	3-STATE to Logical “1” to	R_L = 10k, T_J = 25°C		325	600	ns
	Logical “0” Level	C_L = 50 pF, T_J = 125°C		375	700	ns
t_{IB}	Interdigit Blanking Time	T_J = 25°C	5	10		µs
		T_J = 125°C	10	20		µs
f_{MUX}	Multiplex Scan Frequency	T_J = 25°C		350		Hz
		T_J = 125°C		250		Hz
C_{IN}	Input Capacitance	(Note 6)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	(Note 6)		30	50	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

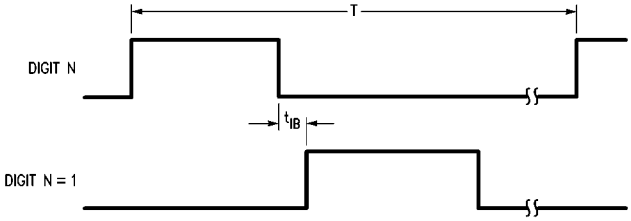
Note 6: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms





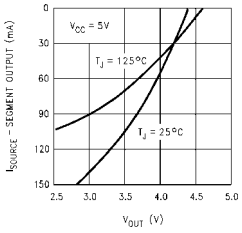
Multiplexing Output Waveforms



$T = 1/f_{MUX}$

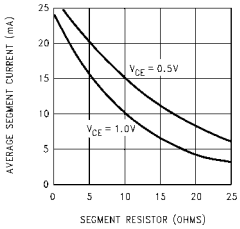
Typical Performance Characteristics

I_{SH} vs V_{OUT}



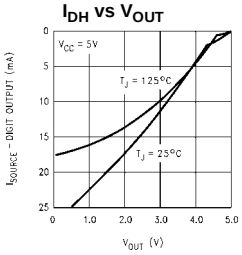
Segment outputs if shorted to ground will exceed maximum power dissipation of the device

I_{AVG} vs R_{LIM}

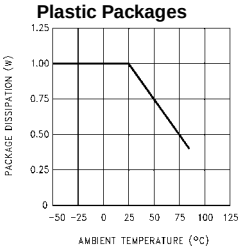


V_{CE} is the saturation voltage of the digit drive transistor.

I_{DH} vs V_{OUT}

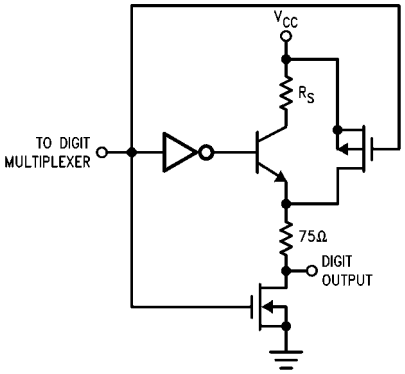


Power Dissipation vs. Temperature for Plastic Packages

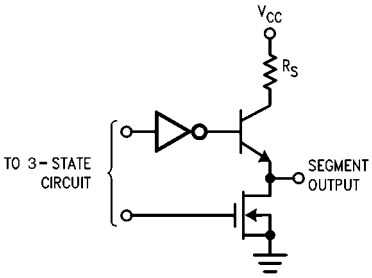


Typical Applications

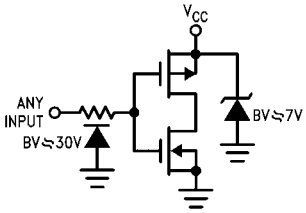
Digit Output Structure

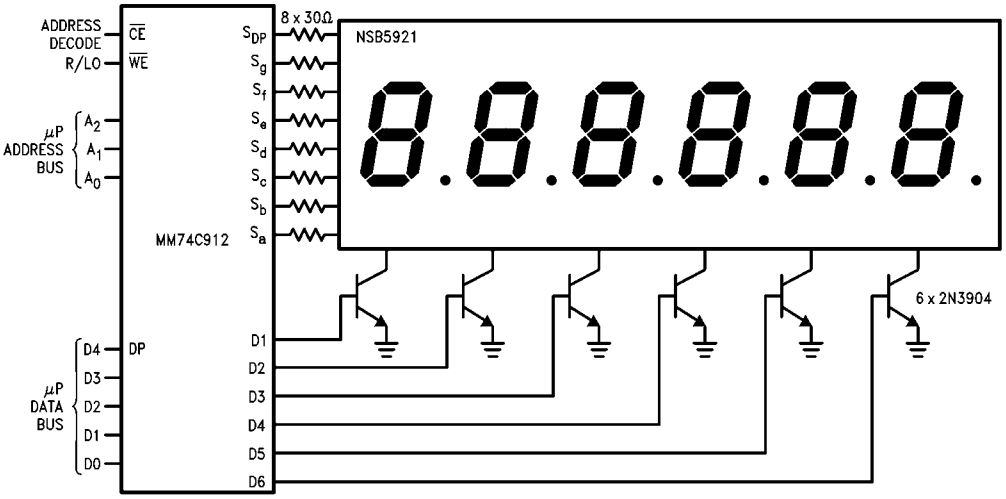


Segment Output Structure

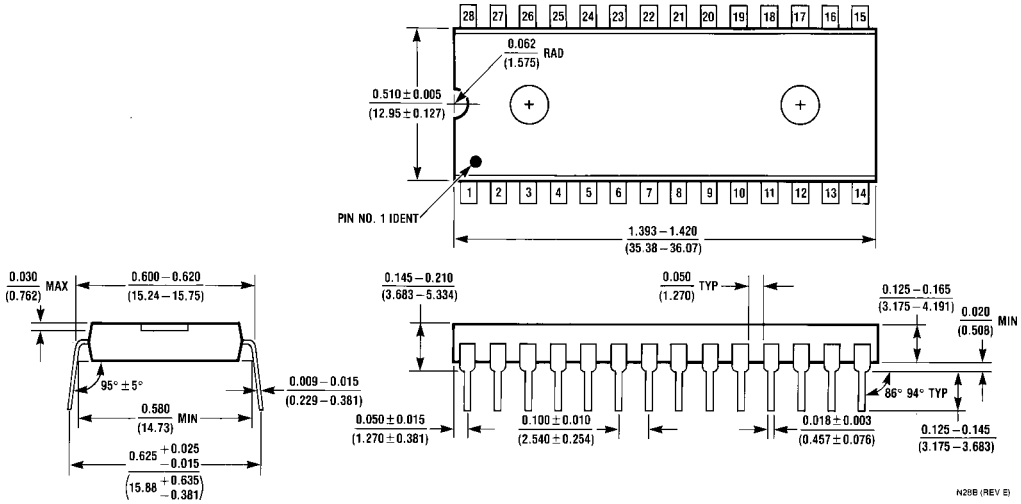


Input Protection





Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.600" Wide
Package Number N28B

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