FAIRCHILD SEMICONDUCTOR™

September 1983
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MM74HCT14
Hex Inverting Schmitt Trigger

General Description

The MM74HCT14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HCT logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 10 µA maximum
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V
- TTL, LS pin-out and input threshold compatible

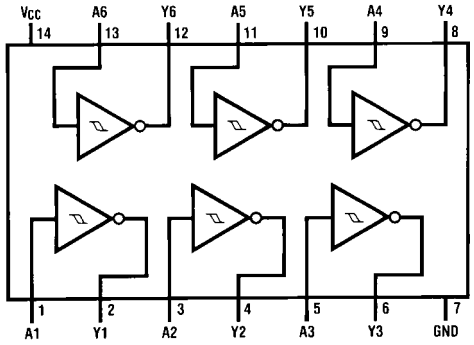
Ordering Codes:

Order Number	Package Number	Package Description
MM74HCT14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HCT14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

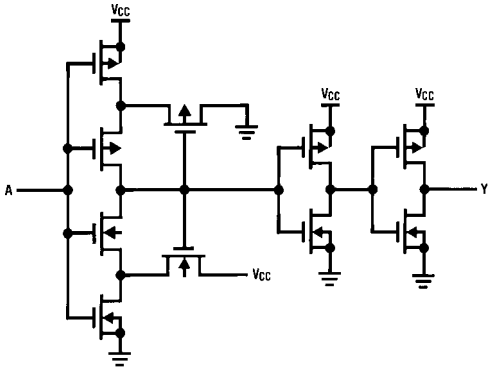
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Schematic Diagram



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Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C		Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going	Minimum	4.5V	1.5	1.2	1.2	V
	Threshold Voltage		5.5V	1.7	1.4	1.4	V
		Maximum	4.5V	1.5	1.9	1.9	V
			5.5V	1.7	2.1	2.1	V
V_{T-}	Negative Going	Minimum	4.5V	0.9	0.5	0.5	V
	Threshold Voltage		5.5V	1.0	0.6	0.6	V
		Maximum	4.5V	0.9	1.2	1.2	V
			5.5V	1.0	1.4	1.4	V
V_H	Hysteresis Voltage	Minimum	4.5V	0.6	0.4	0.4	V
			5.5V	0.7	0.4	0.4	V
		Maximum	4.5V	0.6	1.4	1.4	V
			5.5V	0.7	1.5	1.5	V
V_{OH}	Minimum HIGH Level	$V_{IN} = V_{IL}$					
	Output Voltage	$\|I_{OUT}\|$ = 20 μA		V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		4.2	3.98	3.84	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V		5.2	4.98	4.98	V
V_{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$					
	Voltage	$\|I_{OUT}\|$ = 20 μA		0	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.2	0.26	0.33	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V		0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND			±0.1	±1.0	μA
		V_{IH} or V_{IL}					
I_{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	5.5V		1.0	10	μA
	Supply Current	I_{OUT} = 0 μA					
		V_{IN}=2.4V or 0.5V (Note 3)	5.5V		2.4	2.4	mA

Note 3: For a power supply of 5V ± 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

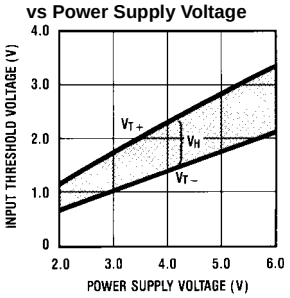
V_{CC}= 5V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°	T_A = −40 to 85°C		Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay			20	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	ns
C_{PD}	Power Dissipation Capacitance (Note 4)	(per gate)		25		pF
C_{IN}	Maximum Input Capacitance		5	10	10	pF

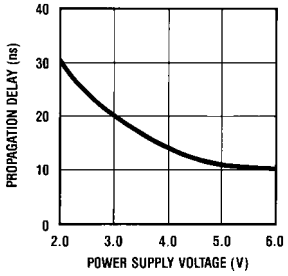
Note 4: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Performance Characteristics

Input Threshold, V_T+, V_T-, vs Power Supply Voltage

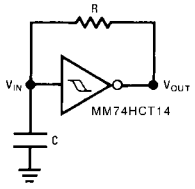


Propagation Delay vs Power Supply



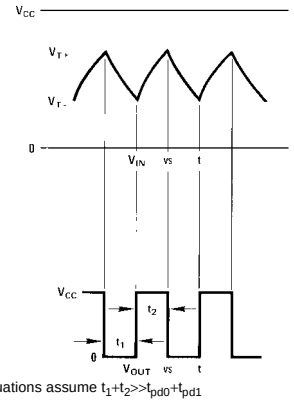
Typical Applications

Low Power Oscillator



$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$



Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$

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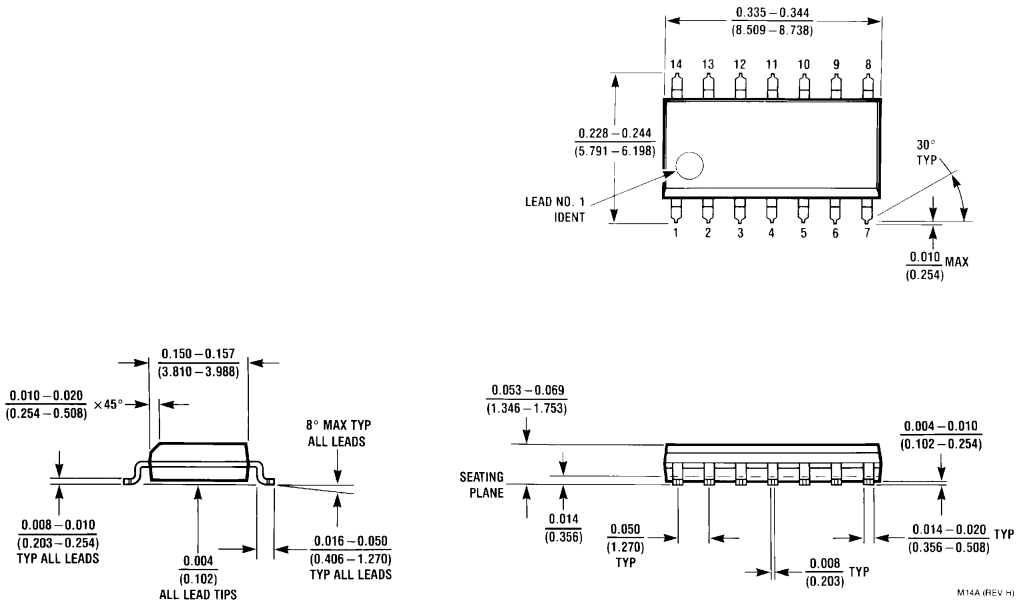
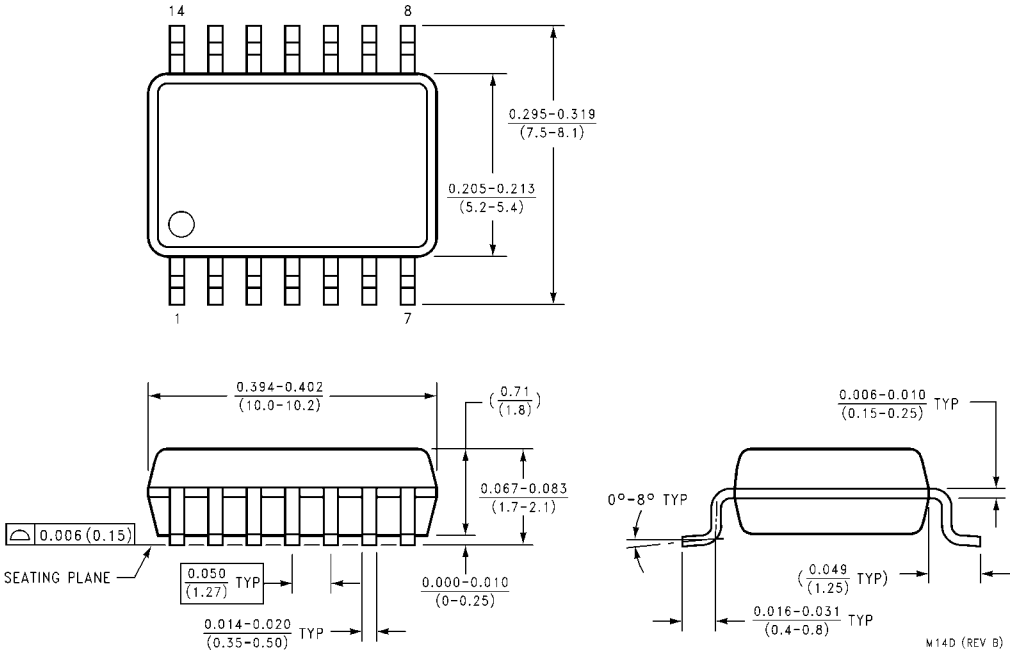
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

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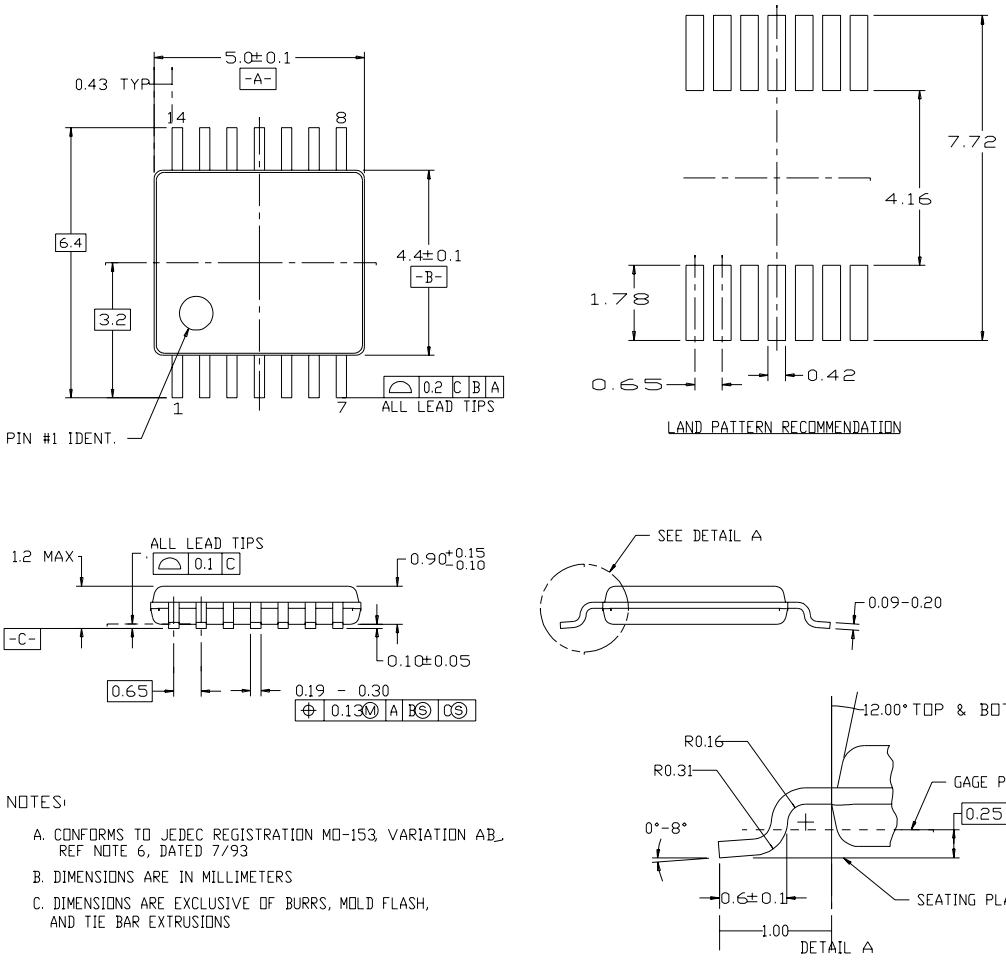
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

4LD, TSSOP, JEDEC MO-153, 4.4MM WIDE



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

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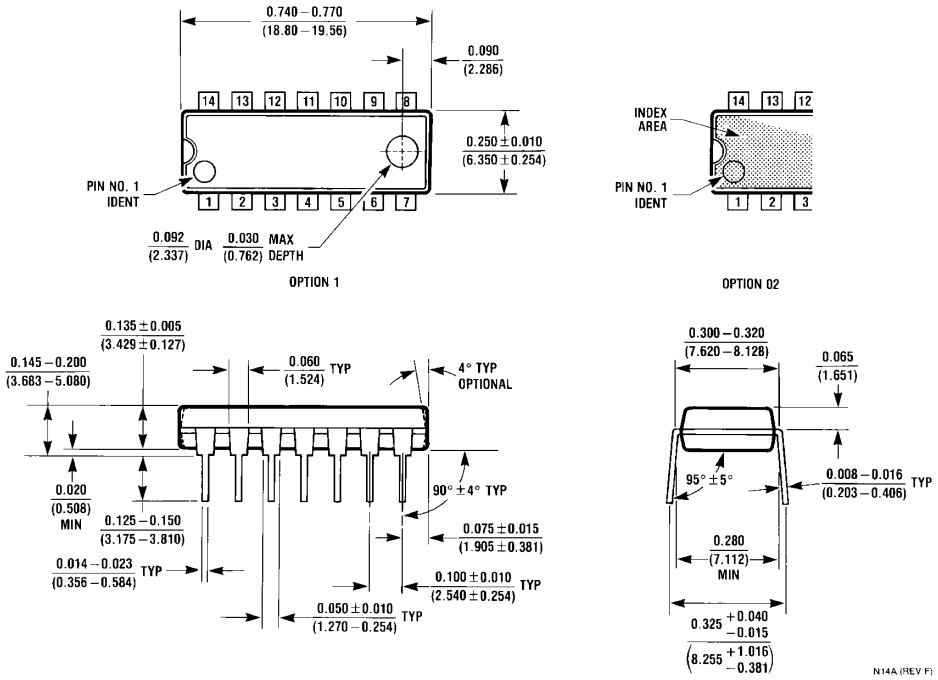
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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