PCK942P

Low voltage 1 : 18 clock distribution chip

Rev. 01 — 17 February 2006 Product data sheet

1. General description

The PCK942P is a 1 : 18 low voltage clock distribution chip with 2.5 V or 3.3 V LVCMOS output capabilities. The device is offered in two versions: the PCK942C has an LVCMOS input clock, while the PCK942P has a LVPECL input clock. The 18 outputs are 2.5 V or 3.3 V LVCMOS compatible and feature the drive strength to drive 50 Ω series-terminated transmission lines. With output-to-output skews of 200 ps, the PCK942P is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5 V output also makes the device ideal for supplying clocks for a higher performance Pentium II microprocessor-based design.

With a low output impedance of approximately 12 Ω, in both the HIGH and LOW logic states, the output buffers of the PCK942P are ideal for driving series-terminated transmission lines. With an output impedance of 12 Ω, the PCK942P can drive two series-terminated transmission lines from each output. This capability gives the PCK942P an effective fan-out of 1 : 36. The PCK942P provides enough copies of low skew clocks for most high performance synchronous systems.

The differential LVPECL inputs of the PCK942P allow the device to interface directly with a LVPECL fan-out buffer like the MC100EP111 to build very wide clock fan-out trees or to couple to a high frequency clock source. The OE pin will place the outputs to a high-impedance state. The OE pin has an internal pull-up resistor.

The PCK942P is a single supply device. The V_{CC} power pins require either 2.5 V or 3.3 V. The 32-lead LQFP package was chosen to optimize performance, board space, and cost of the device. The 32-lead LQFP package has a 7 mm × 7 mm body size with a conservative 0.8 mm pin spacing.

2. Features

- LVPECL clock input
- 2.5 V LVCMOS outputs for Pentium II microprocessor support
- 200 ps maximum targeted output-to-output skew
- Maximum output frequency of 250 MHz at 3.3 V V_{CC}
- 32-lead LQFP packaging
- Single 3.3 V or 2.5 V supply voltage

PHILIPS

3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCK942PBD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4. Functional diagram

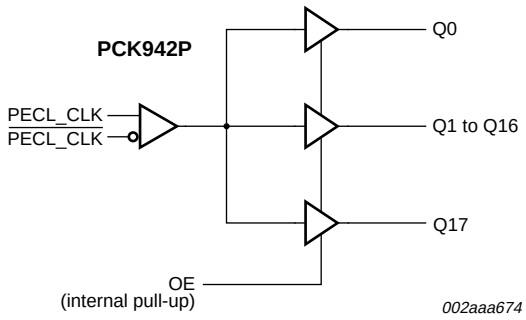


Fig 1. Functional diagram of PCK942P

5. Pinning information

5.1 Pinning

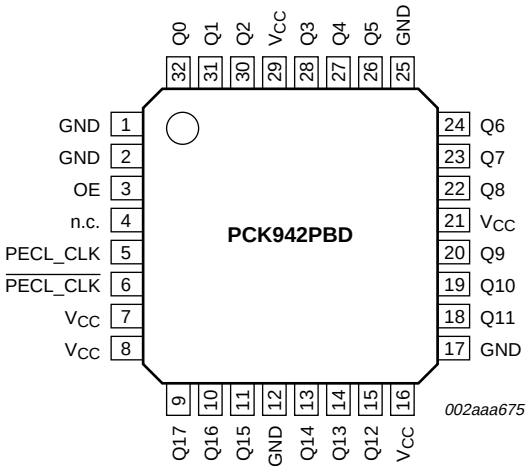


Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
GND	1, 2, 12, 17, 25	ground
OE	3	output enable
n.c.	4	not connected
PECL_CLK, $\overline{\text{PECL\_CLK}}$	5, 6	differential clock inputs
Q[0:17]	32, 31, 30, 28, 27, 26, 24, 23, 22, 20, 19, 18, 15, 14, 13, 11, 10, 9	outputs
V_{CC}	7, 8, 16, 21, 29	supply voltage

6. Functional description

6.1 Function table

Table 3: Function table

OE	Output
0	high-impedance
1	outputs enabled

7. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+3.6	V
V_I	input voltage		–0.3	V_{DD} + 0.3	V
I_I	input current	CMOS inputs	-	±20	mA
T_{stg}	storage temperature		–40	+125	°C

8. Static characteristics

Table 5: Static characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 2.5 V ± 5 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-state input voltage		2.0	-	V_{CC}	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK	0.6	-	1.0	V
V_{IX}	crosspoint voltage of differential inputs	PECL_CLK	V_{CC} – 1.0	-	V_{CC} – 0.6	V
V_{OH}	HIGH-state output voltage	I_{OH} = –16 mA	2.0	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 16 mA	-	-	0.5	V
I_I	input current		-	-	±200	µA
C_i	input capacitance		-	4.0	-	pF
C_{PD}	power dissipation capacitance	per output	-	14	-	pF
Z_o	output impedance		-	12	-	Ω
$I_{q(max)}$	maximum quiescent current		-	0.5	5.0	mA

Table 6: Static characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 3.3 V ± 5 %

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-state input voltage		2.4	-	V_{CC}	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
$V_{i(p-p)}$	peak-to-peak input voltage	PECL_CLK	0.6	-	1.0	V
V_{IX}	crosspoint voltage of differential inputs	PECL_CLK	V_{CC} – 1.0	-	V_{CC} – 0.6	V
V_{OH}	HIGH-state output voltage	I_{OH} = –20 mA	2.4	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 20 mA	-	-	0.6	V
I_I	input current		-	-	±200	µA
C_i	input capacitance		-	4.0	-	pF
C_{PD}	power dissipation capacitance	per output	-	14	-	pF
Z_o	output impedance		-	12	-	Ω
$I_{q(max)}$	maximum quiescent current		-	0.5	5.0	mA

9. Dynamic characteristics

Table 7: Dynamic characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 2.5 V ± 5 %

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{oper(max)}$	maximum operating frequency			-	-	200	MHz
t_{PLH}	LOW-to-HIGH propagation delay			1.8	-	4.0	ns
t_{PHL}	HIGH-to-LOW propagation delay			2.0	-	4.3	ns
$t_{sk(o)}$	output skew time	output-to-output		-	-	200	ps
$t_{sk(pr)}$	process skew time	part-to-part	[2]	-	-	2.2	ns
		part-to-part	[1]	-	-	1.3	ps
t_r	rise time	output		0.1	-	1.0	ns
t_f	fall time	output		0.1	-	1.0	ns

[1] For a specific temperature and voltage, includes output skew.

[2] Across temperature and voltage ranges, includes output skew.

Table 8: Static characteristics

T_{amb} = 0 °C to 70 °C; V_{CC} = 3.3 V ± 5 %

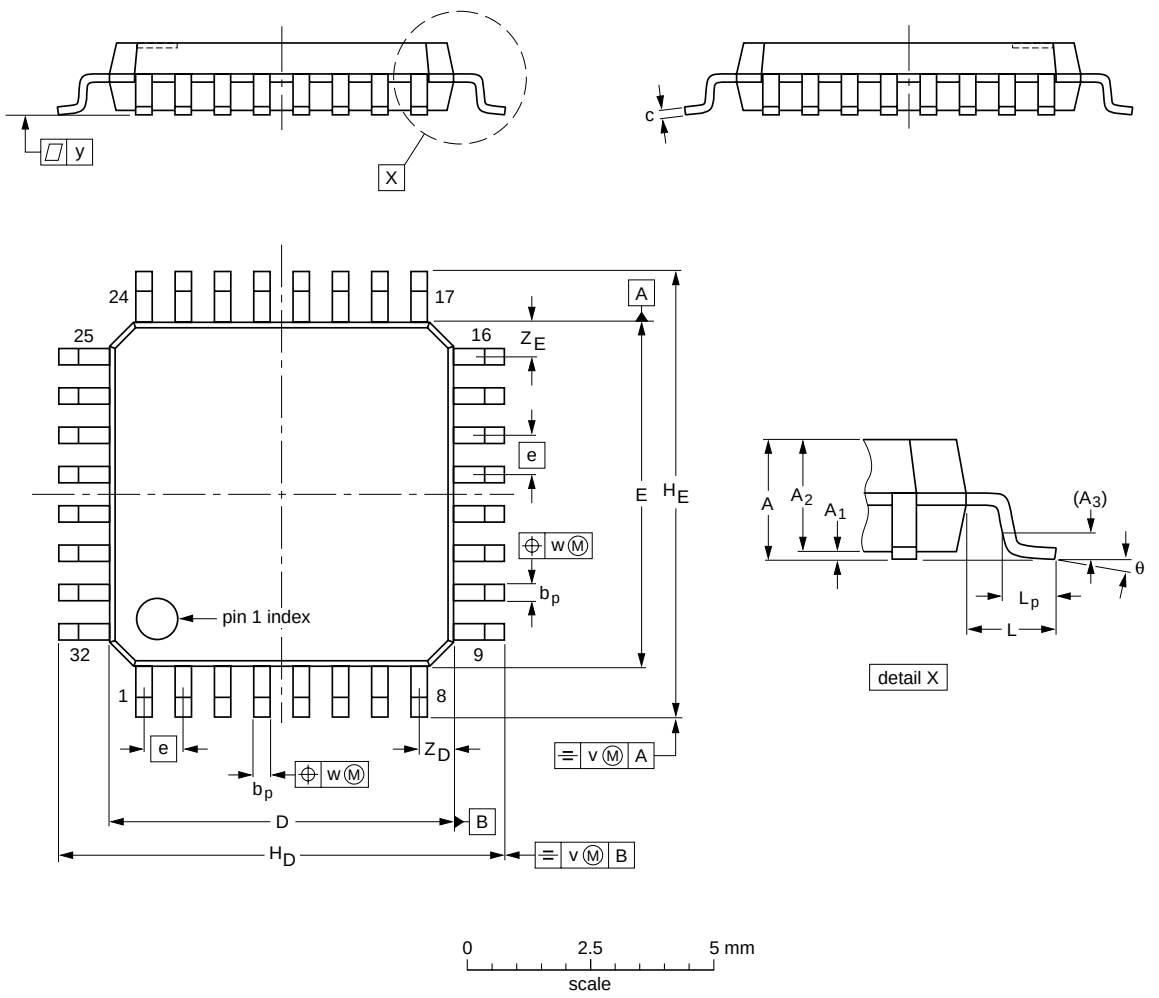
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{oper(max)}$	maximum operating frequency			-	-	250	MHz
t_{PLH}	LOW-to-HIGH propagation delay			1.5	-	3.2	ns
t_{PHL}	HIGH-to-LOW propagation delay			1.5	-	3.6	ns
$t_{sk(o)}$	output skew time	output-to-output		-	-	200	ps
$t_{sk(pr)}$	process skew time	part-to-part	[2]	-	-	1.7	ns
		part-to-part	[1]	-	-	1.0	ps
t_r	rise time	output		0.1	-	1.0	ns
t_f	fall time	output		0.1	-	1.0	ns

[1] For a specific temperature and voltage, includes output skew.

[2] Across temperature and voltage ranges, includes output skew.

10. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 3. Package outline SOT358-1 (LQFP32)

11. Soldering

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

11.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

12. Abbreviations

Table 10: Abbreviations

Acronym	Description
LVCMOS	Low Voltage Complementary Metal Oxide Silicon
LVPECL	Low Voltage Positive Emitter Coupled Logic

13. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCK942P_1	20060217	Product data sheet	-	9397 750 12261	-

14. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

15. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

16. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

17. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

Date of release: 17 February 2006
Document number: 9397 750 12261

Published in The Netherlands